Unit / Module Description:	Sundance Local Bus Specification
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SLB
(Sundance Local Bus)
Specification

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Revision History

Issue	Changes Made	Date	Initials
1.0	Revised Sundance LVDS Bus documentation.	21/8/07	GKP
1.1	Details added about alignment holes on SLB connectors.	29/01/08	PhSR
1.2	Updated External Links and added new Links	23/10/12	FC
1.2.1	Added optional outline cut-out detail.	14/11/12	GKP

Important comments or cautions are displayed next to this symbol.

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1 Introduction

1.1 Overview

Every application has varying input and output requirements. These can be simple USB interfaces, Camera-Link, or high-speed analog I/O. Utilising a standard base module, a flexible system can be tailored by attaching a wide variety of daughter modules. For this reason, the SLB mezzanine concept was introduced.

This concept consists of a carrier/base board which includes a high density connector. This connector accepts a daughter module (or mezzanine) which is mounted above the carrier (or in some case can be mounted separately and joined using a flexible cable).

The SLB connector is of a differential construction (based on a Samtec QSH/QTH-DP series 0.5 mm pitch connectors) and characterised for high-speed data of over 16Gbps (Gigabits per second) per pin pair.

The connector is split into three banks/sections, 2 for high-speed differential (LVDS) data transfer, and one for control. This is however, only examples. Some combination of Base Boards and SLB will use different pin-outs and total freedom is provide with the use of FPGAs on the Base Board.

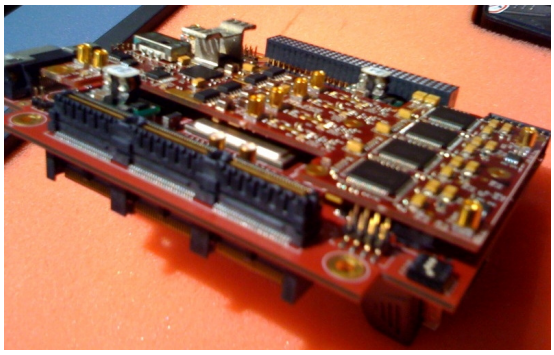
A separate connector provides power to the mezzanine board.

This document describes how the SLB works and specifies mechanical and electrical characteristics.

1.2 SLB Features

Below are listed the features of the SLB:

- Low Voltage Differential Signalling (LVDS), supported by FPGAs, EPLDs, etc.
- One control signal port, typical
- Two differential data ports, typical
- A set of power supplies: +3.3, +5, +12 and –12 Volts.
- Two-extra mounting holes to hold Main/Base and Daughter modules together.



SLB Module fitted onto Carrier Board

2 Related Documents

Samtec – QTH Specifications:

http://www.samtec.com/ProductInformation/TechnicalSpecifications/Overview.aspx?series=QTH

Samtec – QSH Specifications:

http://www.samtec.com/ProductInformation/TechnicalSpecifications/Overview.aspx?series=QSH

Samtec – BKS Specifications:

http://www.samtec.com/ProductInformation/TechnicalSpecifications/Overview.aspx?series=BKS

Samtec – BKT Specifications:

http://www.samtec.com/ProductInformation/TechnicalSpecifications/Overview.aspx?series=BKT

Samtec HQCD cable series:

http://www.samtec.com/ProductInformation/TechnicalSpecifications/Overview.aspx?series=HQCD

Samtec High Speed Connector Characterization Report:

http://www.samtec.com/ProductInformation/TechnicalSpecifications/High_Speed_Test_Reports.aspx?series=QSH&stack=5.00

Samtec High Speed Cable Characterization Report:

http://www.samtec.com/ProductInformation/TechnicalSpecifications/High_Speed_Test_Reports.aspx?series=HQCD&stack=1000.00

Sundance – SMT598:

http://www.sundance.com/prod_info.php?board=SMT598

Sundance Wiki Page about SLB

http://wiki.sundance.com/index.php/SLB_Mezzanine

Sundance YouTube Page about SLB

http://www.youtube.com/watch?v=Xz0LHFduK28&feature=plcp

3 Mechanical Specifications

3.1 Type of connector – Data and control signals

The SLB data/control connectors used to stack up modules, are manufactured by Samtec. They are 5mm-stack height, 0.5-mm pitch and specially made to carry differential pair signals. Both connectors on Main/Base and Daughter modules have 120 pins. The Samtec part numbers are as follows:

- ***QTH-060-01-F-D-DP-A*** for the base module.

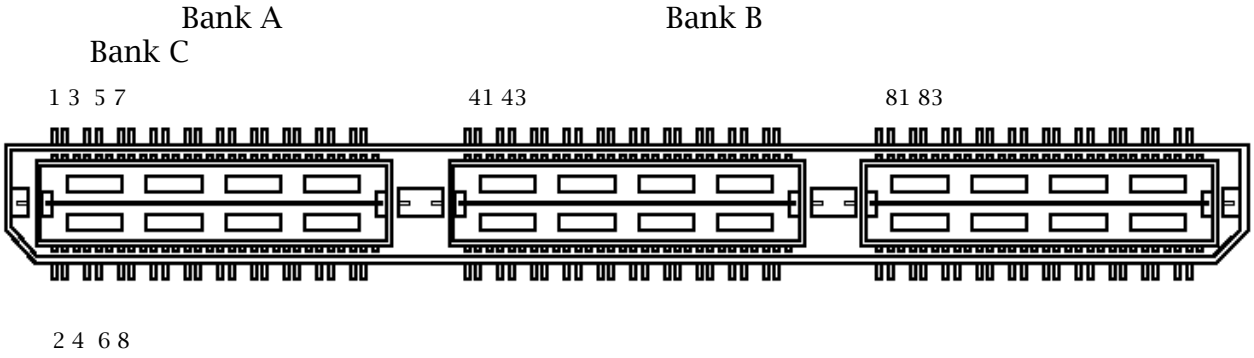


Figure 1 - QTH-060-01-F-D-DP-A (Top View)

- ***QSH-060-01-F-D-DP-A*** for the daughter module.

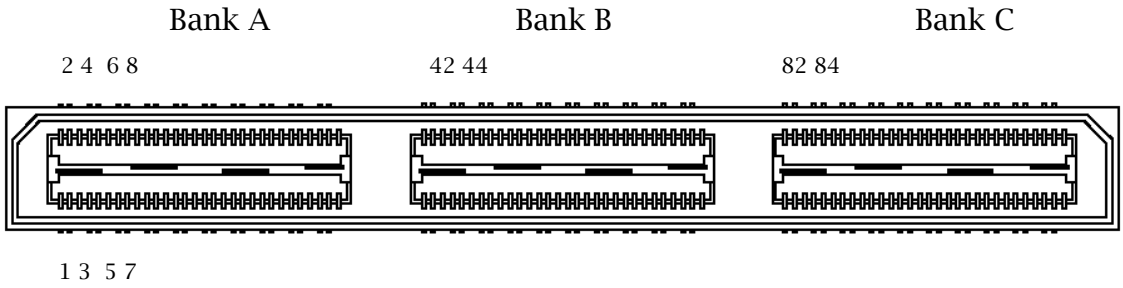


Figure 2 - QSH-060-01-F-D-DP-A (Top View)

Each of the two connectors shows 60 differential pairs, split into three Banks A, B and C. Banks A and C are ideally suited for data and Bank B for control signals. In addition to the shielding provided by the differentials pairs, connections to ground are added along the centre-line of the connectors.

3.2 Type of connector – Power Supplies

The SLB power supplies connectors used to stack up modules, are manufactured by Samtec. They are 5mm-stack height, 1-mm pitch and specially made to carry high currents. Both connectors on Main/Base and Daughter modules have 23 pins. The Samtec part numbers are as follows:

- ***BKS-133-01-F-V-A*** for the base module and

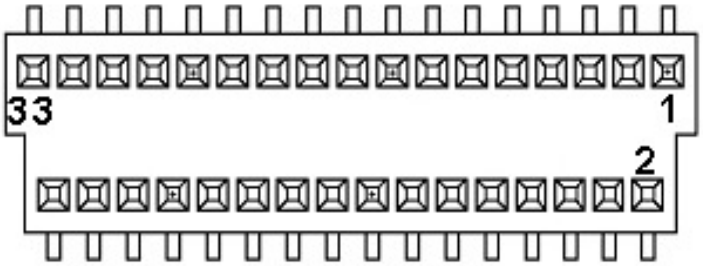


Figure 3 - BKS-133-01-F-V-A – Top View.

- ***BKT-133-03-F-V-A*** for the daughter module.

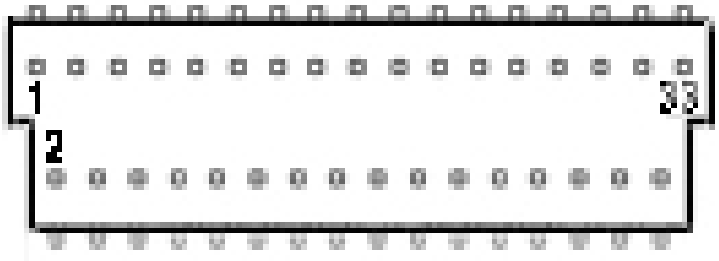
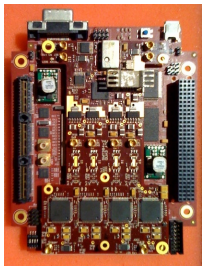


Figure 4 - BKT-133-03-F-V-A – Top View.

3.3 Mounting Hole Location

Note that Sundance can provide a gerber file of an existing board in order to check the right location of the connectors. It is an easy and quick test to make sure of the right location of the connectors and mounting holes.

To see an example of how both modules are interconnected, please go to Sundance's YouTube Page: http://www.youtube.com/watch?v=Xz0LHFduK28&feature=plcp



Top View of SLB

3.3.1 Main or Base Module

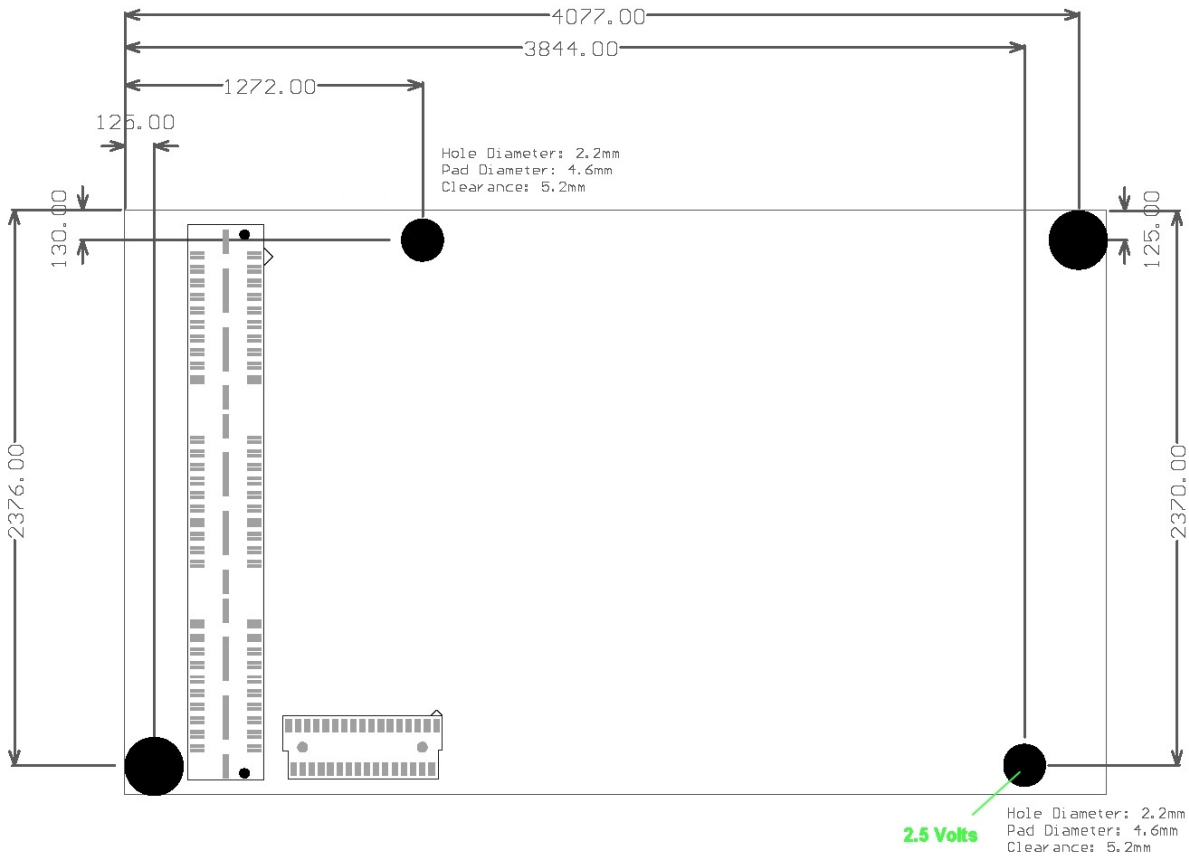


Figure 5 - Main/Base Module - Top View – Mounting Hole Location

3.3.2 Daughter Module

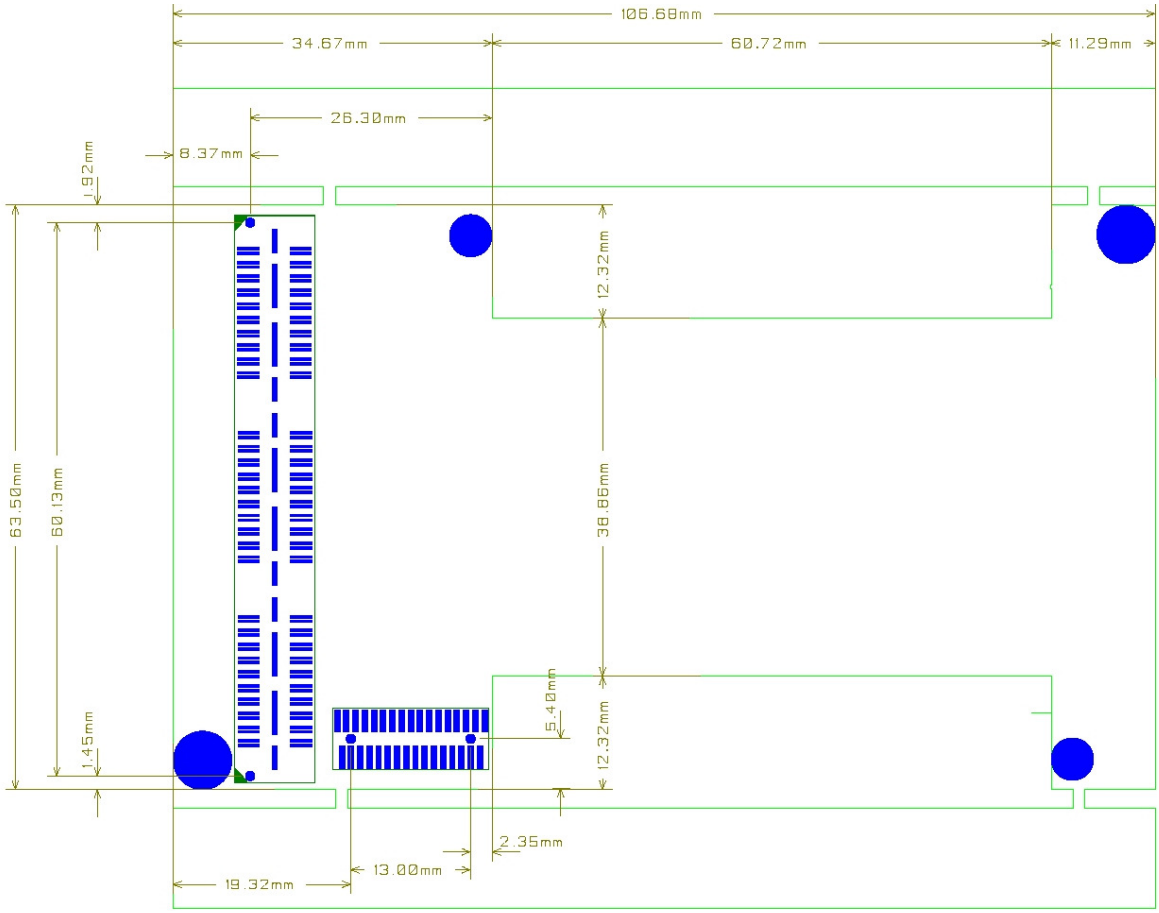


Figure 6 - Daughter Module - Top View - location of QSH and BKT connectors

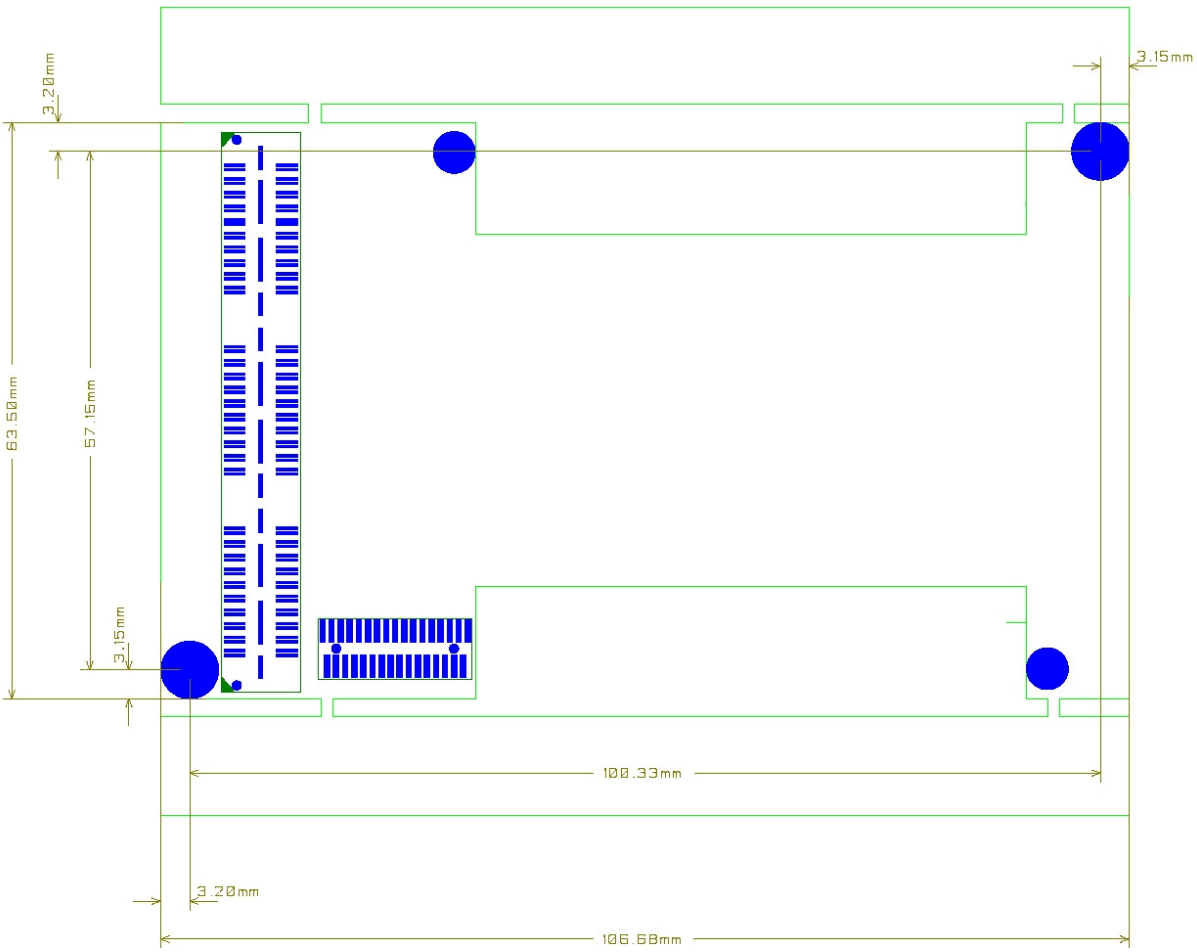


Figure 7 - Daughter Module - Top View – location of large mounting holes

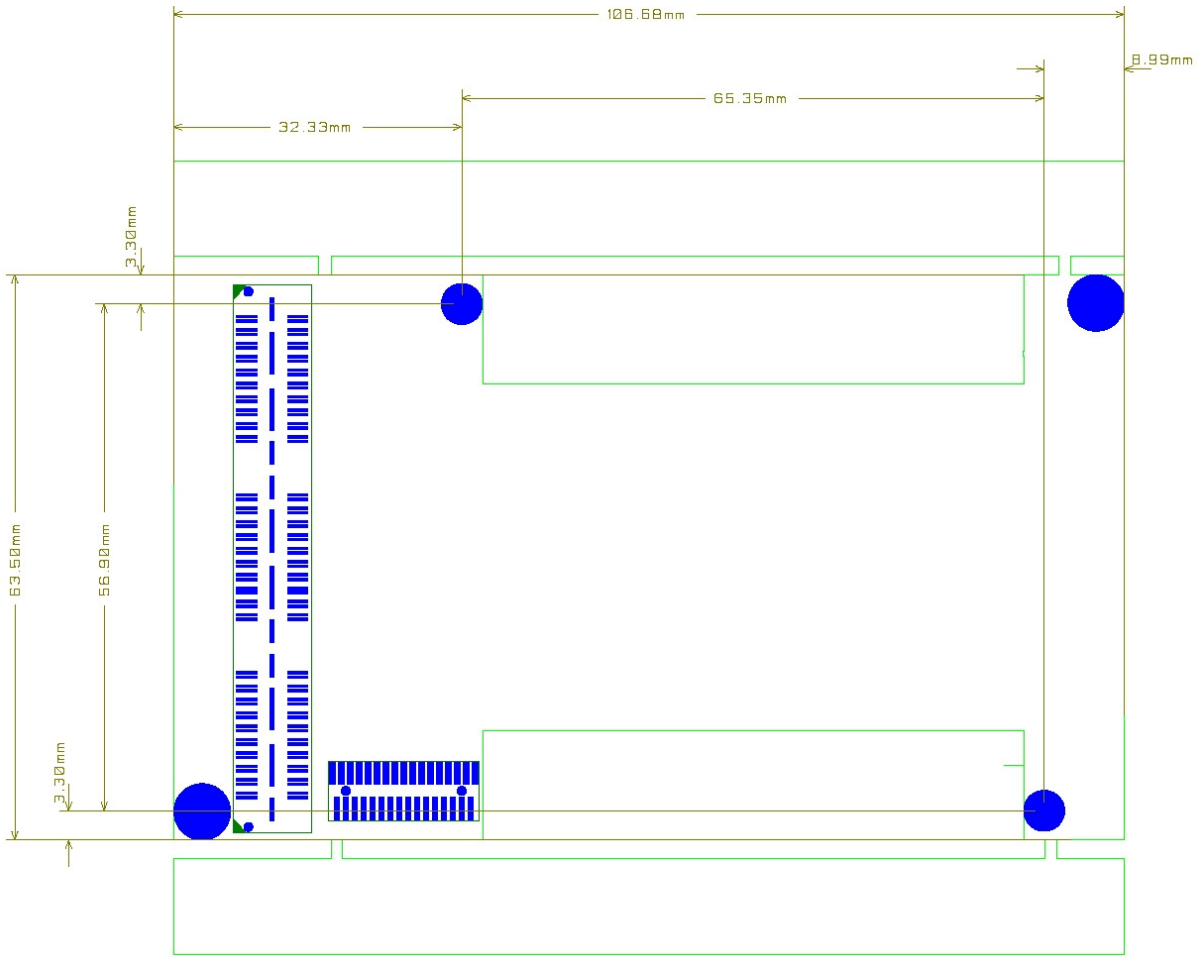


Figure 8 - Daughter Module - Top View - location of small mounting holes

3.4 Alignment holes

All connectors (Data/Controls and Power Supplies on Daughter and Base modules) have 2 alignment holes, which don't need to be platted as they are made of plastic. In order to ensure a good alignment of all Base and Daughter modules, it is recommended to verify the tolerance used by the PCB manufacturer on non-platted holes. They can be as big as +/-0.5mm. Some manufacturers can process non-platted holes using a lower tolerance.

In the above daughter module drawings (top views), the SLB data and power connectors are fitted on the underside of the board.

3.4.1 Notes

As you can see on the previous figures, modules don't only have the usual pair of 3.3 Volt mounting holes but they also have two smaller (in diameter) ones. They have been added to maintain both modules tight together and to provide the daughter module with a 2.5 Volt supply (note that the 2.5V supply has limited current). Note also that the 2.5V power to this mounting hole is options. Please verify your requirement with the appropriate carrier module/board documentation.

Location and dimensions of these extra mounting holes are shown on the above figures.

If none of the extra mounting holes are used, make sure that they are left unconnected as they are plated through.

As shown in the SLB drawing (dimensioned outline), the two long edges have cut-outs. These are useful in providing an access path to the carrier board's connectors (where fitted). These cut-outs are optional but recommended. Please check the compatibility of an SLB module with the target carrier board.

4 Electrical Specifications and Pin Assignment

4.1 Data and Control connectors (QSH and QTH)

The following table gathers the characteristics of both connectors provided by Samtec. Full details available from here.

Table 1 QSH/QTH Characteristics.

Maximum impedance Mismatch and Crosstalk	System Bandwidth	Signal Rise Time
5%	Up to 700MHz	No faster than 500ps.
10%	Up to 1.33GHz	No faster than 263ps
Data Valid up to	12GHz	30ps

4.2 Trace Routing Requirements

4.2.1 Data Routing

Below is some general guidance advice for high-speed PCB routing. It is strongly advised that further investigation be made on how to effectively ensure differential traces are routed correctly.

For the high-speed data ports the signals should be routed differentially and with each pair having closely matched lengths.

Separation of the LVDS pairs should be sufficient to reduce crosstalk.

Ideally, the differential impedance should be 100 Ohms, and the lengths matched to within 0.1".

Sundance can assist with impedance calculations for custom carriers or mezzanines if required.

De-skewing of data can be performed in most LVDS receiving/transmitting FPGA devices and therefore the length requirement can be less constraining.

4.2.2 Control Routing

The control signals have a more relaxed routing requirement. These are typically LVTTL (3.3V) signals that do not have any high-speed data present.

4.3 Connector (Bank A - data) Pin-out

This bank includes two 8-bit differential buses, a single differential clock (output ready) and an out-of-range signal.

Typically, the ClkOI pair will be connected to an FPGA clock capable input (contact Sundance for full details on existing SLB carriers and modules). The FPGASysClk pair can be used to transfer a clock from the carrier to the mezzanine.

Table 2 Pin Assignment - Data/Control Connector - Bank A.

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Bi-directional		Dir	Bi-directional	
1	DOAI0p	Data Out 0, Channel A (pos).	2	DOBI0p	Data Out 8, Channel A (pos).
3	DOAI0n	Data Out 0, Channel A (neg).	4	DOBI0n	Data Out 8, Channel A (neg).
Dir	Bi-directional		Dir	Bi-directional	
5	DOAI1p	Data Out 1, Channel A (pos).	6	DOBI1p	Data Out 9, Channel A (pos).
7	DOAI1n	Data Out 1, Channel A (neg).	8	DOBI1n	Data Out 9, Channel A (neg).
Dir	Bi-directional		Dir	Bi-directional	
9	DOAI2p	Data Out 2, Channel A (pos).	10	DOBI2p	Data Out 10, Channel A (pos).
11	DOAI2n	Data Out 2, Channel A (neg).	12	DOBI2n	Data Out 10, Channel A (neg).
Dir	Bi-directional		Dir	Bi-directional	
13	DOAI3p	Data Out 3, Channel A (pos).	14	DOBI3p	Data Out 11, Channel A (pos).
15	DOAI3n	Data Out 3, Channel A (neg).	16	DOBI3n	Data Out 11, Channel A (neg).
Dir	Bi-directional		Dir	Bi-directional	
17	DOAI4p	Data Out 4, Channel A (pos).	18	DOBI4p	Data Out 12, Channel A (pos).
19	DOAI4n	Data Out 4, Channel A (neg).	20	DOBI4n	Data Out 12, Channel A (neg).
Dir	Bi-directional		Dir	Bi-directional	
21	DOAI5p	Data Out 5, Channel A (pos).	22	DOBI5p	Data Out 13, Channel A (pos).
23	DOAI5n	Data Out 5, Channel A (neg).	24	DOBI5n	Data Out 13, Channel A (neg).
Dir	Bi-directional		Dir	Bi-directional	
25	DOAI6p	Data Out 6, Channel A (pos).	26	DOBI6p	Data Out 14, Channel A (pos).
27	DOAI6n	Data Out 6, Channel A (neg).	28	DOBI6n	Data Out 14, Channel A (neg).
Dir	Bi-directional		Dir	Bi-directional	
29	DOAI7p	Data Out 7, Channel A (pos).	30	DOBI7p	Data Out 15, Channel A (pos).
31	DOAI7n	Data Out 7, Channel A (neg).	32	DOBI7n	Data Out 15, Channel A (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
33	ClkOIp	Output Ready, Channel A (pos).	34	DOIRIp	Out of Range, Channel A (pos).
35	ClkOIn	Output Ready, Channel A (neg).	36	DOIRIn	Out of Range, Channel A (neg).
Dir	Main Module to Daughter Card.		Dir	Daughter Card to Main Module.	
37	FPGASysClkp	Clock Generated on Daughter module to FPGA (pos)	38	ExtTriggerI0	External Trigger from Daughter Module to FPGA (pos).
39	FPGASysClkn	Clock Generated on Daughter module to FPGA (neg)	40	ExtTriggerI1	External Trigger from Daughter Module to FPGA (neg).

4.4 Connector (Bank B - control) Pin-out

Bank B is dedicated for control signals. It includes an SMB interface, a serial number data line, control lines, power supply enable signals, mode lines, dedicated signals and control signals such as JTAG lines.

Table 3 Pin Assignment - Data/Control Connector - Bank B.

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Type	**System Signals**		**Type**	**System Signals**	
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
41	SMBClk	SMB Interface – Clock.	42	SMBData	SMB Interface – Data.
43	SMBnAlert	SMB Interface – Alerts Line	44	SerialNo	Serial Number Data Line.
Dir	Bi-directional		Dir	Bi-directional	
45	Cntrl0	Control Line 0	46	Cntrl2	Control Line 2
47	Cntrl1	Control Line 1	48	Cntrl3	Control Line 3
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
49	PSEnable0	Power Supply 0 Enable	50	PSEnable1	Power Supply 1 Enable
51	Mode0	Mode Line 0.	52	Mode1	Mode Line 1
Type	**Specific Signals**		**Type**	**Specific Signals**	
Dir	Bi-directional		Dir	Bi-directional	
53	Signal0	Signal 0	54	Signal6	Signal 6
55	Signal1	Signal 1	56	Signal7	Signal 7
Dir	Bi-directional		Dir	Bi-directional	
57	Signal2	Signal 2	58	Signal8	Signal 8
59	Signal3	Signal 3	60	Signal9	Signal 9
Dir	Bi-directional		Dir	Bi-directional	
61	Signal4	Signal 4	62	Signal10	Signal 10
63	Signal5	Signal 5	64	Signal11	Signal 11
Type	**Control Signals**		**Type**	**Control Signals**	
Dir	Bi-directional		Dir	Bi-directional	
65	Cntrl4	Control Line 4	66	Cntrl7	Control Line 7
67	Cntrl5	Control Line 5	68	Cntrl8	Control Line 8
Dir	Bi-directional		Dir	Reserved	
69	Cntrl6	Control Line 6	70	FpgaVRef	JTAG FPGA Vref.
71	FpgaTck	JTAG FPGA tck.	72	FpgaTms	JTAG FPGA tms.
Dir	Reserved		Dir	Reserved	
73	FpgaTdi	JTAG FPGA tdi.	74	FpgaTdo	JTAG FPGA tdo.
75	MspVRef	JTAG MSP430 Vref	76	MspTck	JTAG MSP430 tck.
Dir	Reserved		Dir	Reserved	
77	MspTms	JTAG MSP430 tms.	78	MspTdi	JTAG MSP430 tdi.
79	Msptdo	JTAG MSP430 tdo.	80	MspnTrst	JTAG MSP430 reset

Table 4 Optional SLB power pins

75	V33	+3.3V	76	V12	+12V
77	V33	+3.3V	78	V12	+12V
79	V33	+3.3V	80	V12	+12V

The MSP430 JTAG signals are only required to be connected to the SLB module if the MSP micro-controller (fitted on some TIM base modules) needs to be re-programmed or debugged with the SLB mezzanine present. Typically this is only used in such a manner during Sundance test and debug. These signals are not required for normal operation.

Some SLB carriers will provide power supplies to these pins. Please check with the respective user manuals.

4.5 Connector (Bank C - data) Pin-out

This bank includes two 8-bit differential buses, a single differential clock (output ready) and an out-of-range signal.

Typically, the ClkOI pair will be connected to an FPGA clock capable input (contact Sundance for full details on existing SLB carriers and modules). The FPGARslClk pair can be used to transfer a clock from the carrier to the mezzanine.

Table 5 Pin Assignment - Data/Control Connector - Bank C.

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Bi-directional		Dir	Bi-directional	
81	DOAQ0p	Data Out 0, Channel B (pos).	82	DOBQ0p	Data Out 8, Channel B (pos).
83	DOAQ0n	Data Out 0, Channel B (neg).	84	DOBQ0n	Data Out 8, Channel B (neg).
Dir	Bi-directional		Dir	Bi-directional	
85	DOAQ1p	Data Out 1, Channel B (pos).	86	DOBQ1p	Data Out 9, Channel B (pos).
87	DOAQ1n	Data Out 1, Channel B (neg).	88	DOBQ1n	Data Out 9, Channel B (neg).
Dir	Bi-directional		Dir	Bi-directional	
89	DOAQ2p	Data Out 2, Channel B (pos).	90	DOBQ2p	Data Out 10, Channel B (pos).
91	DOAQ2n	Data Out 2, Channel B (neg).	92	DOBQ2n	Data Out 10, Channel B (neg).
Dir	Bi-directional		Dir	Bi-directional	
93	DOAQ3p	Data Out 3, Channel B (pos).	94	DOBQ3p	Data Out 11, Channel B (pos).
95	DOAQ3n	Data Out 3, Channel B (neg).	96	DOBQ3n	Data Out 11, Channel B (neg).
Dir	Bi-directional		Dir	Bi-directional	
97	DOAQ4p	Data Out 4, Channel B (pos).	98	DOBQ4p	Data Out 12, Channel B (pos).
99	DOAQ4n	Data Out 4, Channel B (neg).	100	DOBQ4n	Data Out 12, Channel B (neg).
Dir	Bi-directional		Dir	Bi-directional	
101	DOAQ5p	Data Out 5, Channel B (pos).	102	DOBQ5p	Data Out 13, Channel B (pos).
103	DOAQ5n	Data Out 5, Channel B (neg).	104	DOBQ5n	Data Out 13, Channel B (neg).
Dir	Bi-directional		Dir	Bi-directional	
105	DOAQ6p	Data Out 6, Channel B (pos).	106	DOBQ6p	Data Out 14, Channel B (pos).
107	DOAQ6n	Data Out 6, Channel B (neg).	108	DOBQ6n	Data Out 14, Channel B (neg).
Dir	Bi-directional		Dir	Bi-directional	
109	DOAQ7p	Data Out 7, Channel B (pos).	110	DOBQ7p	Data Out 15, Channel B (pos).
111	DOAQ7n	Data Out 7, Channel B (neg).	112	DOBQ7n	Data Out 15, Channel B (neg).
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
113	ClkOQp	Output Ready, Channel B (pos).	114	DOIRQp	Out of Range, Channel B (pos).
115	ClkOQn	Output Ready, Channel B (neg).	116	DOIRQn	Out of Range, Channel B (neg).
Dir	Main Module to Daughter Card.		Dir	Daughter Card to Main Module.	
117	FPGARslClkp	Clock Generated on Mezzanine module to FPGA (pos)	118	ExtTriggerQ0	External Trigger from Daughter Module to FPGA (pos).
119	FPGARslClkn	Clock Generated on Mezzanine module to FPGA (neg)	120	ExtTriggerQ1	External Trigger from Daughter Module to FPGA (neg).

4.6 Power Supplies Connectors (BKS and BKT)

Each pin on the power connector (33 pins in total) can carry 1.5A. Digital 5V (D+5V0), digital 3V3 (D+3V3) and digital ground (DGND) is provided over this connector. D+3V3 and D+5V0 are assigned four pins each. The daughter card can thus draw a total of 6A from each of these two supplies. The integral ground plane on the differential connector provides additional grounding.

Some JTAG lines are also mapped onto this connector to be used in case the daughter module has a TI Processor. They would allow debugging and programming via JTAG. If not, leave them all unconnected.

The following table (next page) shows the pin assignment on the power connector:

Table 6 Pin Assignment - Power Supplies Connector.

Pin Number	Pin Name	Description of Signal
1	D+3V3	Digital 3.3 Volts
2	DGND	Digital Ground
3	D+3V3	Digital 3.3 Volts
4	DGND	Digital Ground
5	D+3V3	Digital 3.3 Volts
6	DGND	Digital Ground
7	D+3V3	Digital 3.3 Volts
8	DGND	Digital Ground
9	D+5V0	Digital 5.0 Volts
10	DGND	Digital Ground
11	D+5V0	Digital 5.0 Volts
12	DGND	Digital Ground
13	D+5V0	Digital 5.0 Volts
14	DGND	Digital Ground
15	D+5V0	Digital 5.0 Volts
16	DGND	Digital Ground
17	D+12V0	Digital +12.0 Volts – not used on the SMT390
18	DGND	Digital Ground
19	D+12V0	Digital +12.0 Volts – not used on the SMT390
20	DGND	Digital Ground
21	D-12V0	Digital –12.0 Volts – not used on the SMT390
22	DGND	Digital Ground
23	D-12V0	Digital –12.0 Volts – not used on the SM390
24	DGND	Digital Ground
25	DGND	Digital Ground
26	EMU0	Emulation Control 0
27	EMU1	Emulation Control 1
28	TMS	JTAG Mode Control
29	nTRST	JTAG Reset
30	TCK	JTAG Test Clock
31	TDI	JTAG Test Input
32	TDO	JTAG Test Output
33	DGND	Digital Ground

5 Probe Connector

In order to debug a specific system or to connect it to an external module, it might be useful to have access to signals carried by the QTH connector on the base module.

5.1 High Density Ribbon Cable

Figure 9 - High Density Ribbon cable.

Such cables are produced by Samtec (HQCD Series)

5.2 PCB for probing purpose – SMT598

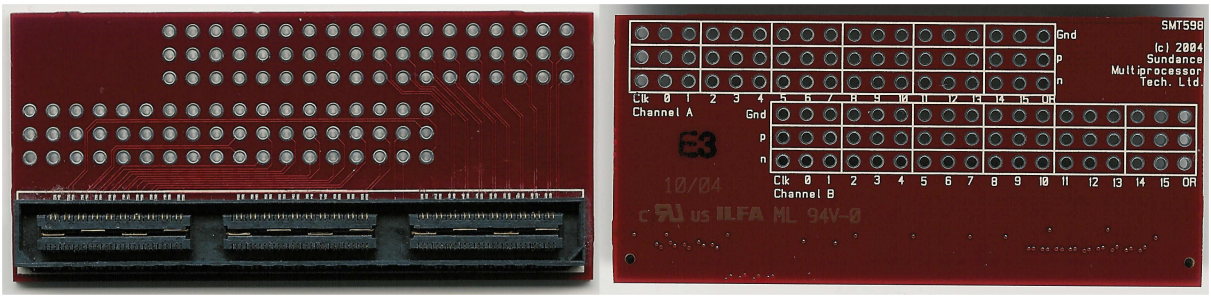


Figure 10 - SMT598.

Sundance produces the SMT598 that allow probing clock, data and over-range differential lines from Banks A and Bank C.

6 Typical SLB Daughter Module

This picture shows the underside of the SMT381 daughter board. The SLB data and power connectors are clearly visible here.