Unit / Module Description:	PCI/104-Express SLB carrier
Unit / Module Number:	SMT100
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Product Specification for SMT100

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Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	28/07/08	GKP
1.1	Major update.	29/08/08	GKP
1.2	Hyperlink update. Replaced CPLD by Spartan-3AN.	18/02/09	GKP
1.2.1	Added TTL I/O header.	18/02/09	GKP
1.2.2	Added external power connector. Added FX70T option.	19/02/09	GKP
1.2.2.1	Correction to V5 configuration method.		
1.2.2.2	Product name change.	4/03/09	GKP
1.3	Added SATA and user I/O connectors. Updated board layout.	4/03/09	GKP
1.4	Added FPGA configuration times.	11/6/09	GKP
1.5	Added 1.2V supply for Spartan3AN.	29/6/09	GKP
1.6	Updated board layout drawings.	7/7/09	GKP
1.7	Updated stack-up/down description.	12/10/09	GKP

Table of Contents

1 Introduction / Description

The SMT100 is an SLB carrier board in the PCI/104-Express (http://www.pc104.org/pci104_Express_specs.php) format.

The main features of the SMT100 are listed below:

- SLB Carrier.
- Virtex5 FX30T/FX70T FPGA (including integrated PowerPC™ core).
- 512Mbyte DDR2 memory.
- USB2 Interface to FPGA.
- RS232 interfaces.
- MicroSD/Transflash.
- 32-bit 33MHz PCI (http://www.pc104.org/pci_104_specs.php).
- 4-lane and 1-lane PCIe interfaces.
- Stack-up or stack-down configurations (automatic detection)

2 Related Documents (hyperlinks)

Sundance Local Bus (SLB) specification.

SMT118: Carrier with 3 Module sites and I/O facilities.

SMT144: Carrier with 4 Module sites.

SMT148FX: Carrier with 4 Module sites.

SMT6048: USB Driver.

SMT6002: Sundance Flash Programming Utility, FPGA.

PCI/104-Express specification.

PCI/104 specification.

PCIe External Cable specification.

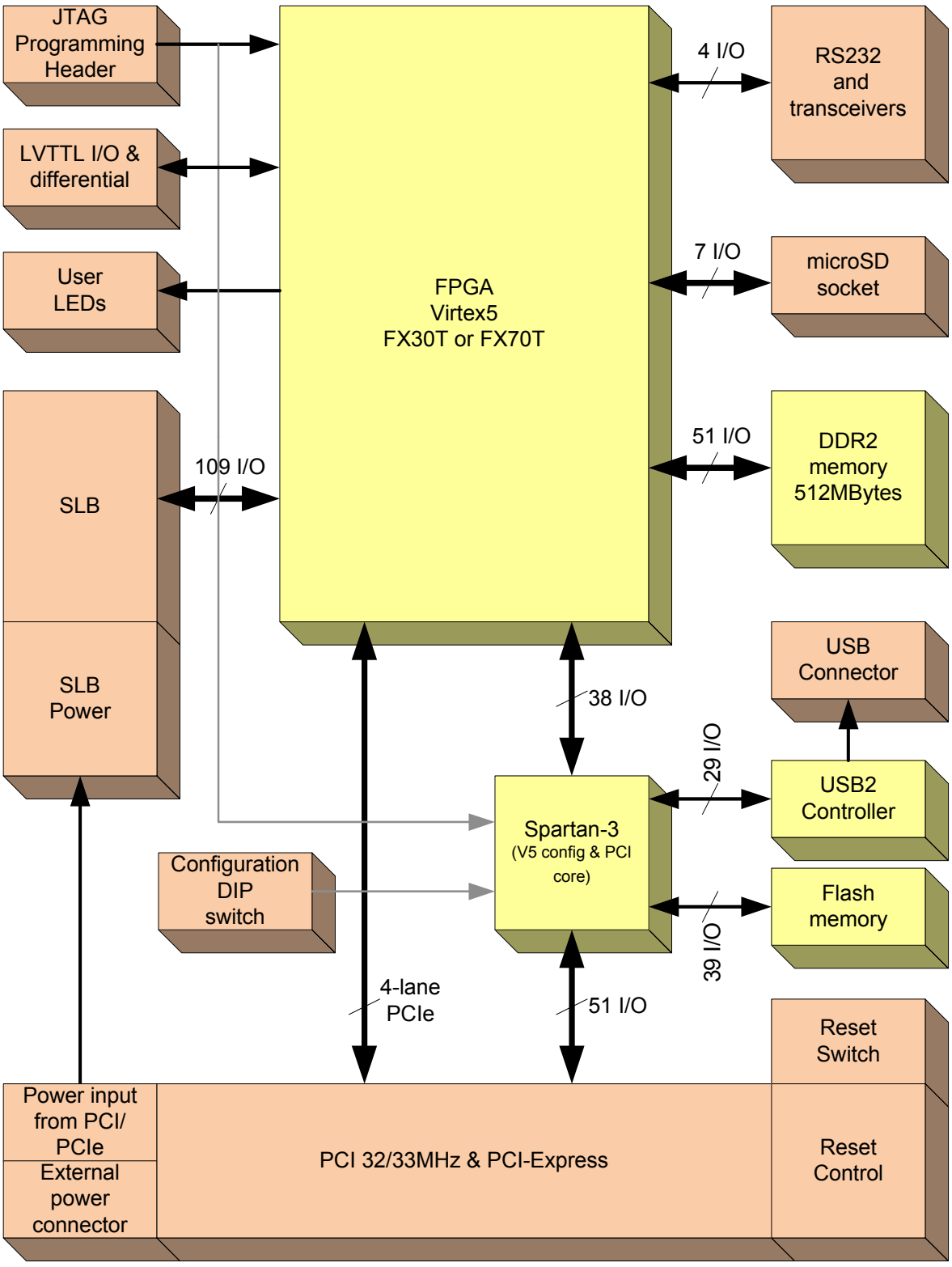
3 Acronyms, Abbreviations and Definitions

A list of acronyms etc:
http://www.sundance.com/web/files/static.asp?pagename=acc

4 Functional Description

The major elements of the SMT100 are shown in the block diagram below.

4.1 Block Diagram



4.2 Module Description

4.2.1 Xilinx Virtex 5 FPGA

A Xilinx Virtex-5 FX30T or FX70T FPGA is the primary FPGA resource on the SMT100.

This device is configured by the Spartan-3AN. Using a configuration clock of 66MHz, an FX70T would configure in 51ms.

1-lane and 4-lane PCIe interfaces are provided together with connections to user LEDs, RS232, microSD socket, DDR2 memory, SATA, and a full implementation of the Sundance SLB.

The configuration speed of both FPGAs is important as the PCIe core needs to be running within 100ms after system power up. Configuration time for the largest FPGA that the SMT100 supports is 75ms (51+24).

4.2.2 Xilinx Spartan 3 FPGA

This device (XC3S200AN) includes a 32-bit 33MHz PCI interface, and connections to the USB2 controller and flash memory.

Operating modes of this device are selected using a DIP switch bank.

This device configures itself using internal SPI flash memory. Configuration at 50MHz should take 24ms.

This device is used to configure the Virtex 5 FPGA.

Configuration data for the Virtex5 can be read from the flash, USB or PCI interfaces.

4.2.3 Cable PCIe

A single lane socket allows the connection to a host via cable PCIe. This connects directly to the Virtex 5's RSL pins.

4.2.4 SATA

Two sockets allow the connection of hard disks. These connect directly to the Virtex 5's RSL pins.

4.2.5 USB2

A Cypress CY7C68013A is used to implement a USB2 interface.

This interface can operate at up to 48MB/s, and is accessed via a mini-B type socket. This is a device only interface.

New FPGA configurations can be written to the flash via USB. Alternatively, the flash can be re-programmed by the host using PCI, PCIe or USB2.

4.2.6 Dual UART

Two RS232 channels comprising of Tx and Rx signals only are available on an 8-way header; Molex 87832-0820.

The corresponding transceivers are connected directly to the Virtex 5 FPGA, thus a UART core must be implemented to use these interfaces.

4.2.7 TTL I/O

A 4x2 0.1" pin header is provided that carries 4 LVTTL I/O signals (directly to the Virtex 5 with diode clamping to 3.3V and GND).

This header also contains 3.3V power and GND, together with a differential pair direct to a clock capable pair on the Virtex 5 FPGA.

4.2.8 SLB

All SLB signals are connected directly to the Virtex 5 FPGA. These include 4 8-bit differential buses and respective clocks.

All differential signals are impedance controlled.

4.2.9 LEDs

4 user LEDs are connected directly to the Virtex 5 FPGA.

4.2.10 Reset

Reset is asserted during power up, or by pressing the reset switch (of the SMT100 only).

4.2.11 DDR2 Memory

Two 128M x 16 devices (eg MT47H128M16HG) provide 512Mbytes of storage.

4.2.12 MicroSD / Transflash

A microSD socket is provided which is connected directly to the Virtex 5 FPGA.

4.2.13 Power Supplies

+3.3V is supplied via a total of 12 pins from both the PCI and PCIe connectors.

+5V and +12V have their major supply via the central conductors of the PCIe connector.

-12V is available from a single pin on the PCI connector.

An external 5-pin power socket can be used for stand-alone operation. The supplied voltages are +/-12V, 5V and 3.3V.

Local supplies are generated as follows:

Voltage	From	Max Current	Comment
1.0V	Switching controller.	10A	Virtex5 core.
1.8V	Switching controller.	10A	DDR2 and GTPs.
2.5V	Linear regulator from 3.3V.	1A	Virtex5 Vccaux.
1.0V	Linear regulator from 1.8V.	4A	Virtex5 Vccmgt.
1.2V	Linear regulator from 1.8V.	4A	Virtex5 Vccpll.
1.2V	Linear regulator from 1.8V.	4A	Virtex5 Vtt.
1.2V	Linear regulator from 1.8V	0.5A	Spartan3AN core.

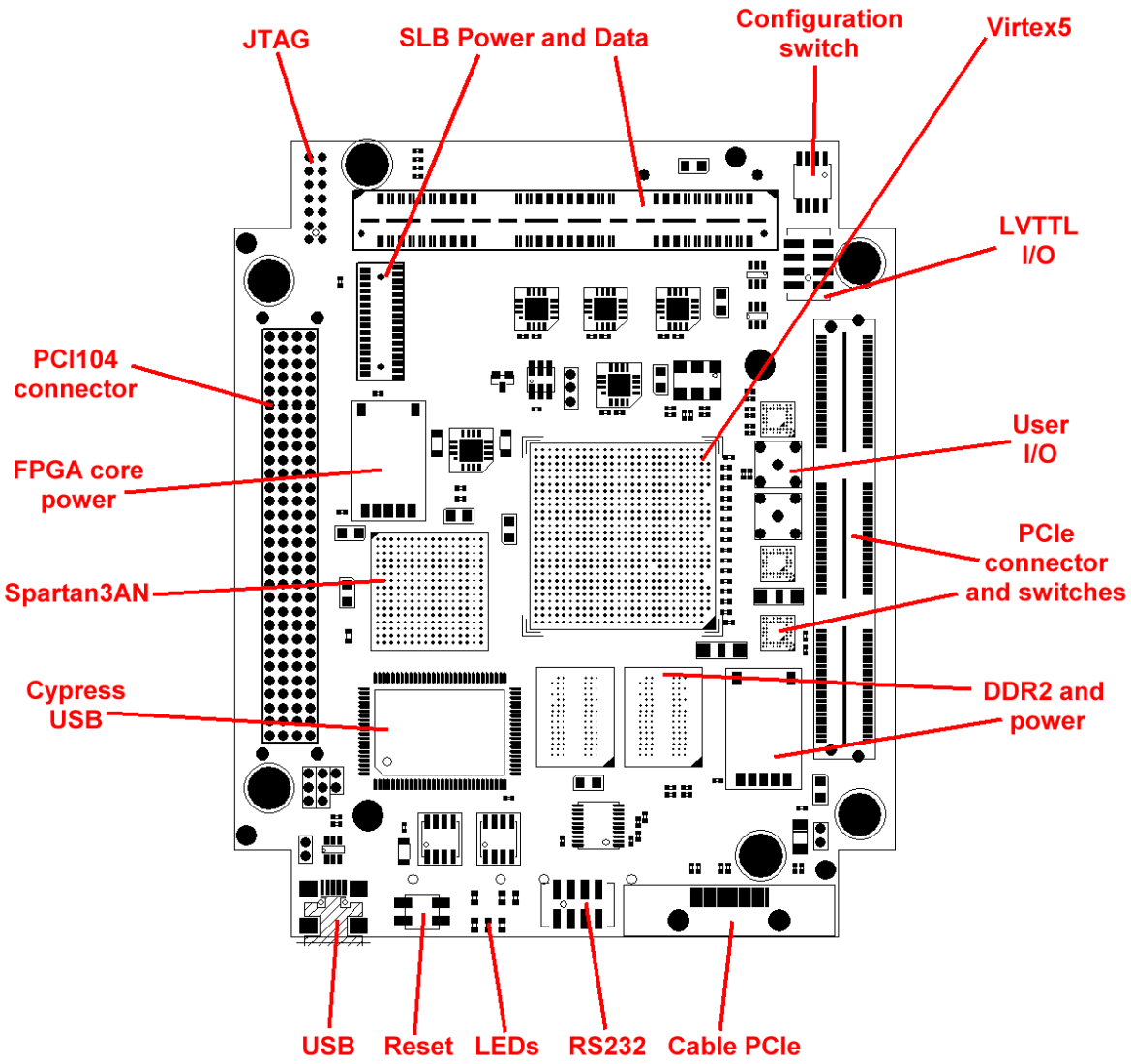
5 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

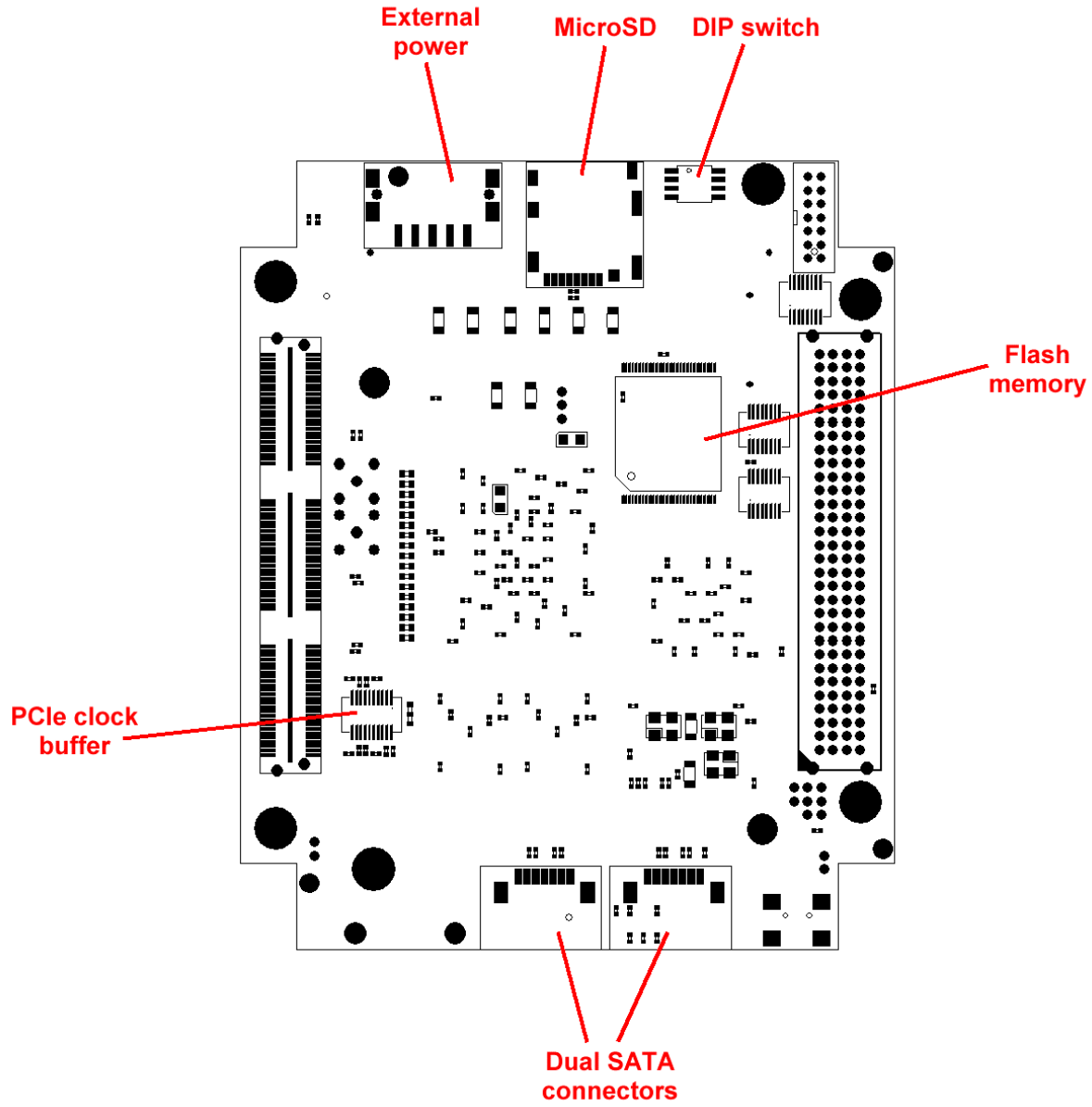
6 Circuit Description / Diagrams

7 Footprint

7.1 Top View



7.2 Bottom View



8 Support Packages

SMT6002 Sundance Flash Programming Utility.

SMT6048 Sundance USB Driver.

3L Diamond FPGA.

9 Physical Properties

Dimensions	95.9mm	115.6mm

Weight	

Voltage	Current (estimate)
+12V	100mA
+5V	1000mA
+3.3V	500mA
-5V	0
-12V	0

MTBF	

Note that the above current requirements are estimates and actual values depend entirely on Virtex 5 configuration, memory utilisation, and type of SLB fitted.

10 Safety

This module presents no hazard to the user when in normal use.

11 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

12 Ordering Information

Order number:

SMT100-30T

SMT100-70T