Unit / Module Description:	PCI/104-Express FFT & SLB carrier
Unit / Module Number:	SMT105
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Product Specification for SMT105

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Certificate Number FM 55022

Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	23/03/10	GKP
1.1	Increased detail.	24/03/10	GKP
1.2	Added fibre & SATA to blk diagram.	25/03/10	GKP
1.3	Corrected memory sizes	25/03/10	GKP
1.4	Added RS232 interfaces.	8/04/10	GKP
1.5	General tidy up. Specified 3 RS232 interfaces with Tx/Rx only. Added DIP switch configuration selection.	13/04/10	GKP
1.6	Moved the x1 PCIe interface to the top connector	16/04/10	GKP
1.7	Updated board layout drawings. Minor text updates.	16/06/10	GKP
1.8	Updated TTL header info. Added JP3, 6, 7, 9, 10 detail. Added BAT1 detail. Added LED detail.	15/12/14	GKP

Table of Contents

1 Introduction / Description

The SMT105 is an SLB carrier board in the PCI/104-Express format.

The main features of the SMT105 are listed below:

- SLB Carrier.
- Virtex5 FX100T FPGA (including integrated PowerPC™ core).
- 256Mbyte DDR2 memory.
- 3 x 72Mbit QDRII memory.
- USB2 Interface to FPGA.
- Dual 4-lane PCIe interfaces.
- 2 x Fibre interfaces.
- 2 x SATA interfaces.
- MicroSD/Transflash.
- 2 RS232 interfaces.

2 Related Documents (hyperlinks)

Sundance Local Bus (SLB) specification.

SMT6048: USB Driver.

SMT6002: Sundance Flash Programming Utility, FPGA.

PCI/104-Express specification.

PCI/104 specification.

Sundance SMT100 PCI104e SLB carrier.

Digital Logic MSM945 PCI104e controller.

Lippert GS45 PCI104e controller.

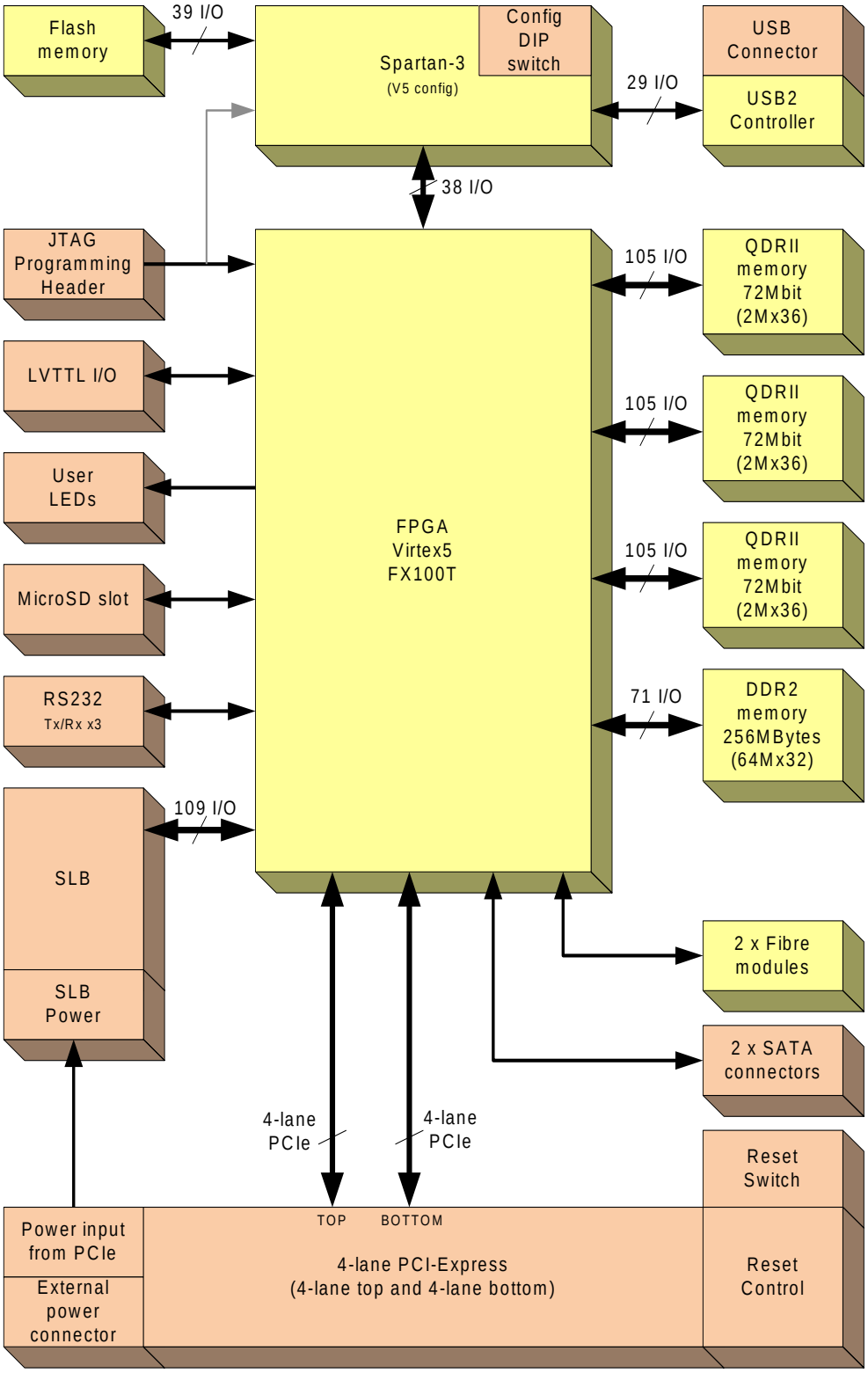
3 Acronyms, Abbreviations and Definitions

A list of acronyms etc:
http://www.sundance.com/web/files/static.asp?pagename=acc

4 Functional Description

The major elements of the SMT105 are shown in the block diagram below.

4.1 Block Diagram



4.2 Module Description

4.2.1 Xilinx Virtex 5 FPGA

A Xilinx Virtex-5 FX100T FPGA is the primary FPGA resource on the SMT105.

This device is configured by the Spartan-3AN. Using a configuration clock of 66MHz, an FX100T would configure in 75ms.

Two 4-lane PCIe and two 1-lane interfaces are provided together with connections to user LEDs, DDR2 memory, QDRII memory, SATA, and a full implementation of the Sundance SLB.

The configuration speed of both FPGAs is important as the PCIe core needs to be running within 200ms after system power up.

4.2.2 Xilinx Spartan 3 FPGA

This device (XC3S200AN) includes a connections to the USB2 controller, Virtex5 and flash memory.

Operating modes of this device are selected using a DIP switch bank.

This device configures itself using internal SPI flash memory. Configuration at 50MHz takes 24ms.

This device is used to configure the Virtex 5 FPGA.

Configuration data for the Virtex5 can be read from the flash or USB. Several Virtex 5 configurations can be stored within a 512Mbit flash device which is directly connected to the Spartan 3. A DIP switch allows for the selection of a particular configuration.

4.2.3 SATA

Two sockets allow the connection of hard disks. These connect directly to the Virtex 5's RSL pins. A single oscillator provides the GTX reference clock for SATA. Switching between SATA-I and II requires an oscillator change.

4.2.4 USB2

A Cypress CY7C68013A is used to implement a USB2 interface.

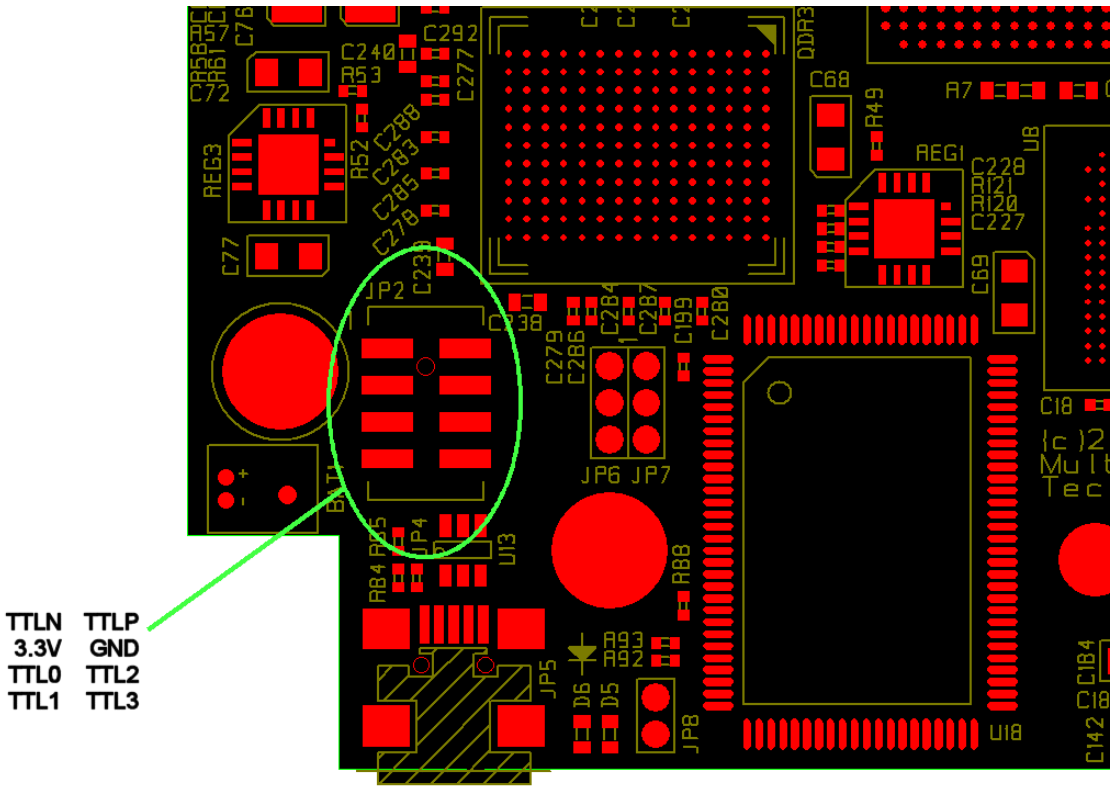
This interface can operate at up to 48MB/s, and is accessed via a mini-B type socket. This is a device only interface.

New FPGA configurations can be written to the flash via USB. Alternatively, the flash can be re-programmed by the host using PCIe.

4.2.5 TTL I/O

A 4x2 0.1" pin header is provided that carries 4 LVTTL I/O signals (directly to the Virtex 5 with diode clamping to 3.3V and GND).

This header also contains 3.3V power and GND, together with a differential pair direct to a clock capable pair on the Virtex 5 FPGA.



BGA pin	Signal
AH8	TTLN
NA	3.3V
AG20	TTL0
AE18	TTL1

Signal	BGA pin
TTLP	AG8
GND	NA
TTL2	AH15
TTL3	AF18

4.2.6 SLB

All SLB signals are connected directly to the Virtex 5 FPGA. These include 4 8-bit differential buses and respective clocks.

All differential signals are impedance controlled.

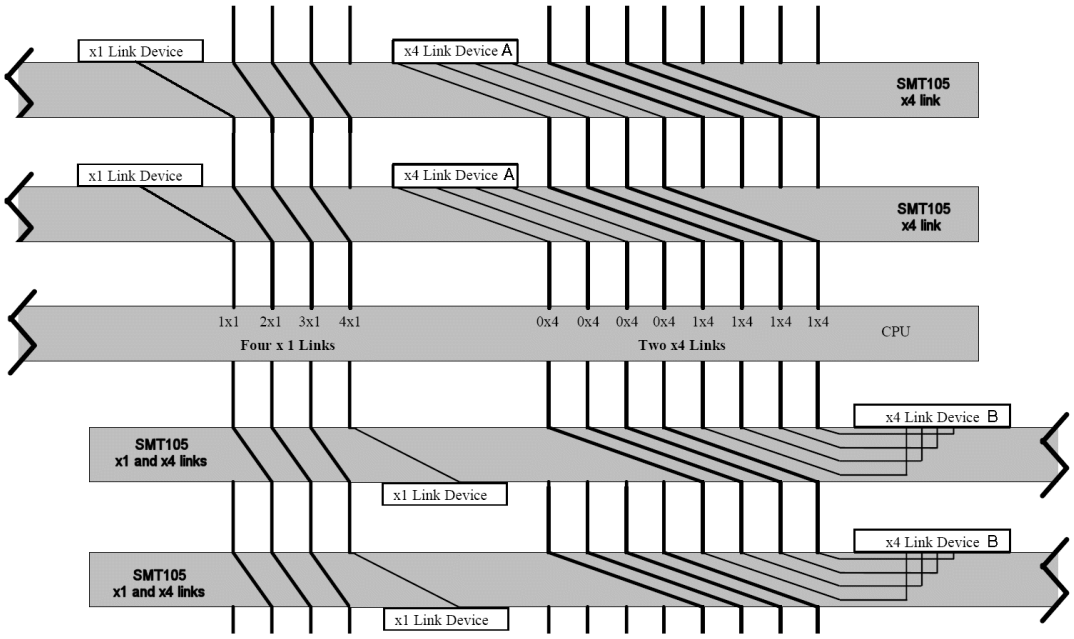
4.2.7 PCI Express (PCIe)

Two 4–lane interfaces are provided within the Virtex 5 (labelled A & B below). Only one interface is used at any one time. This is determined by the location of the SMT105 in the PCI/104e stack (stack–up or stack–down). Each 4–lane interface uses a different PCIe core within the FPGA, and separate GTX lanes.

Additionally a single 1–lane interface is provided within the Virtex 5. This interface can be connected in either the stack–up or stack–down configuration. Separate GTX lanes are used for this interface, but these are directed to a single PCIe core.

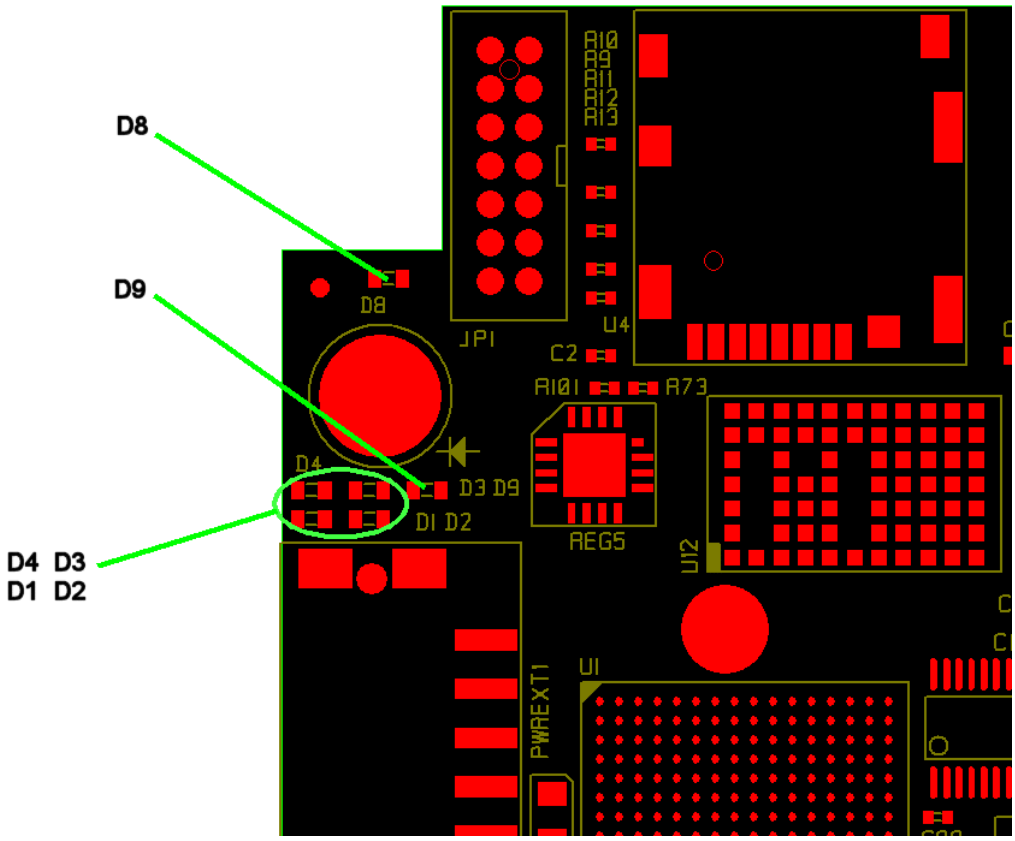
Thus all 3 of the PCIe cores are used. Note that the 1–lane interface can be used concurrently with the 4–lane interface; the host will recognise two devices.

Shown here are both the top and bottom stacks. Only one should be used at any given time.



4.2.8 LEDs

4 user LEDs are connected directly to the Virtex 5 FPGA.



LEDs D1 to D4 are connected directly to the FPGA using pins H20, H19, H13 and H14 respectively.

LED D9 will illuminate when the XC3S200A FPGA is configured.

LED D8 will illuminate when the Virtex 5 FPGA is configured.

4.2.9 Fibre

Two fibre modules (Stratos RJS_ST31) provide full–duplex links with data rates from 1 to 4Gbps over distances of 150 to 500m (typically) dependant on line speed.

Industry standard LC connectors allow the use of 50 or 62.5um fibres with an 850nm wavelength.

Provision of a dedicated oscillator allows for any data rate within the above limits to be set.

4.2.10 Reset

Reset is asserted during power up, PCI104e controller reset, or by pressing the reset switch on the SMT105.

The power up delay of the reset circuit is set to 21ms. This is in excess of the start–up times of the DCDC converters used, thus guaranteeing that all power supplies will be stable before the board is released from reset.

4.2.11 DDR2 Memory

Two 64M x 16 devices (eg MT47H64M16) provide 256Mbytes of storage. These have a maximum clock speed of 267MHz.

4.2.12 QDRII Memory

Three banks of QDRII memory are provided (eg CY7C15xxKV18). Each is 72Mbit in capacity and organised as 2M x 36. These devices have a maximum clock speed of 250MHz.

4.2.13 MicroSD / Transflash

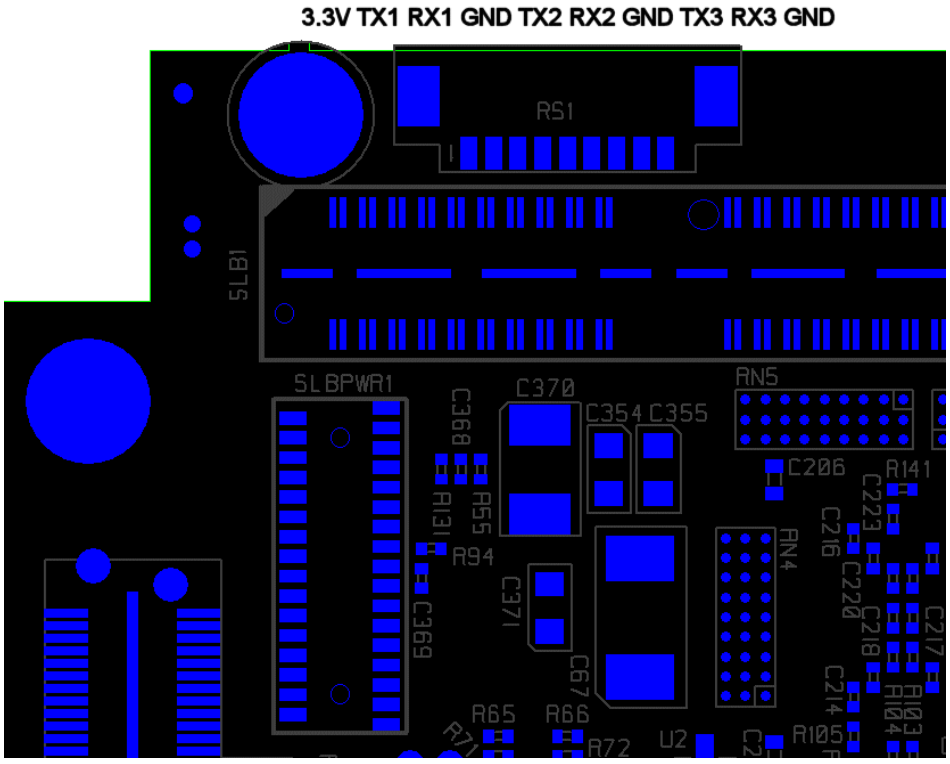
A microSD socket is provided which is connected directly to the Virtex 5 FPGA.

4.2.14 RS232

Three RS232 interfaces are provided and are connected to the Virtex 5 FPGA via a MAX3387E level translator.

Each interface consists of a Tx and Rx signal, and they are made available on a single board edge mounted 1.25mm 10-pin Molex PicoBlade connector (eg. Farnell 1125362).

The pin signal names are shown in the picture here:



See crimps and housings for details:

http://www.molex.com/molex/products/family?key=picoblade&channel=products&chanName=family&pageTitle=Introduction

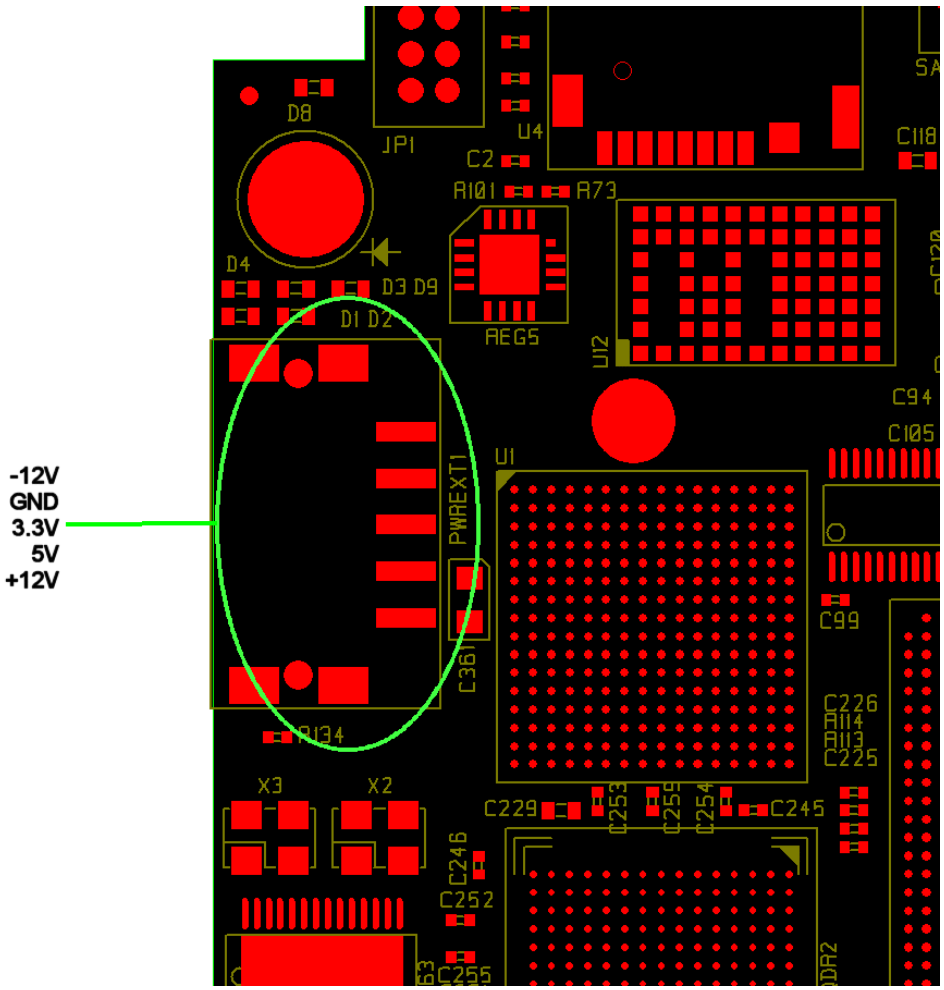
Mating part is Molex 0510211000 with 0500588000 crimp terminals.

4.2.15 Power Supplies

+3.3V is supplied via a total of 2 pins from the PCIe connector.

+5V and +12V have their major supply via the central conductors of the PCIe connector.

An external 5-pin power socket can be used for stand-alone operation. The supplied voltages are +/-12V, 5V and 3.3V. The housing is an ERNI MaxiBridge™ part #254823.



Various mating parts are available. E.g. ERNI 176040 (AWG26, 100mm, Blue).

Local supplies are generated as follows:

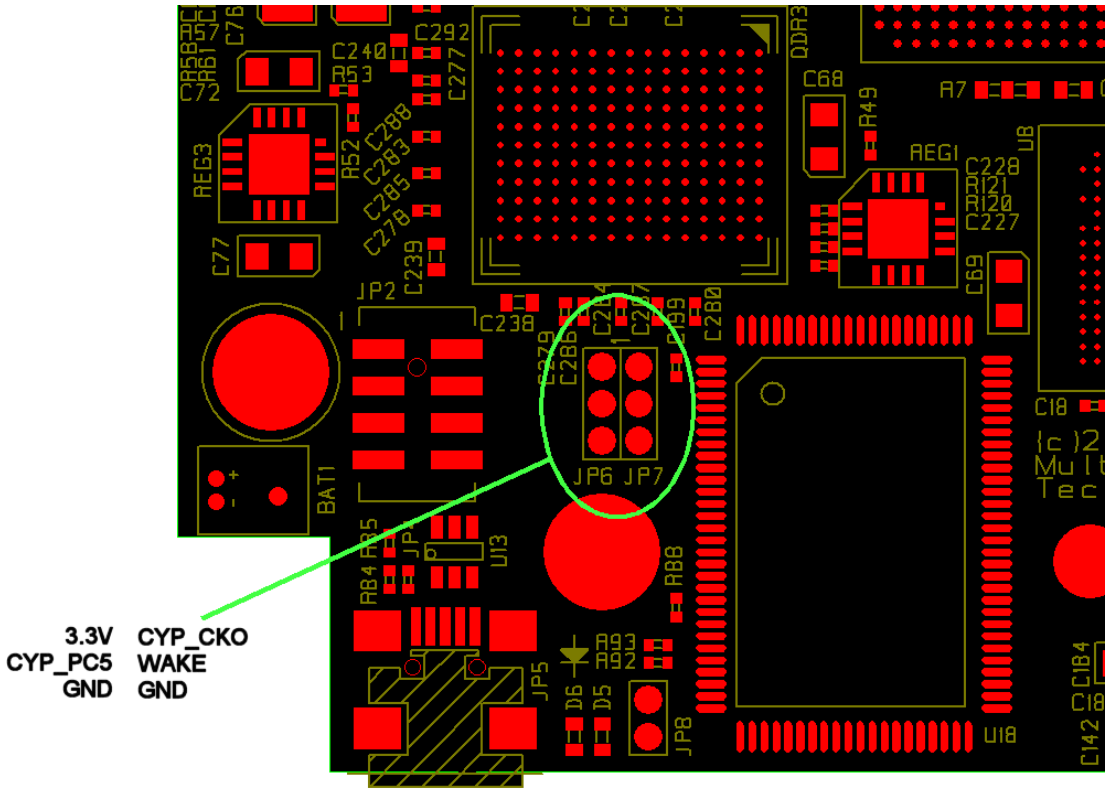
Voltage	From	Max Current	Comment
1.0V	Switching controller.	12A	Virtex5 core.
1.8V	Switching controller.	8A	DDR2, QDRII and GTPs.
2.5V	Linear regulator from 3.3V.	1A	Virtex5 Vccaux.
1.0V	Linear regulator from 1.8V.	4A	Virtex5 Vccmgt.
1.2V	Linear regulator from 1.8V.	4A	Virtex5 Vccpll.
1.2V	Linear regulator from 1.8V.	4A	Virtex5 Vtt.
1.2V	Linear regulator from 1.8V	0.5A	Spartan3AN core.
0.9V	Switching controller	6A	Memory termination.

4.2.16 Miscellaneous Jumpers

4.2.16.1 JP6 & JP7

Jumper JP6 (3-pin header) carries the signals 3.3V, CYP_PC5, and GND. This header is used for board debug.

JP7 carries the signals CYP_CKO (clkout), WAKE, and GND. This header is used for board testing.



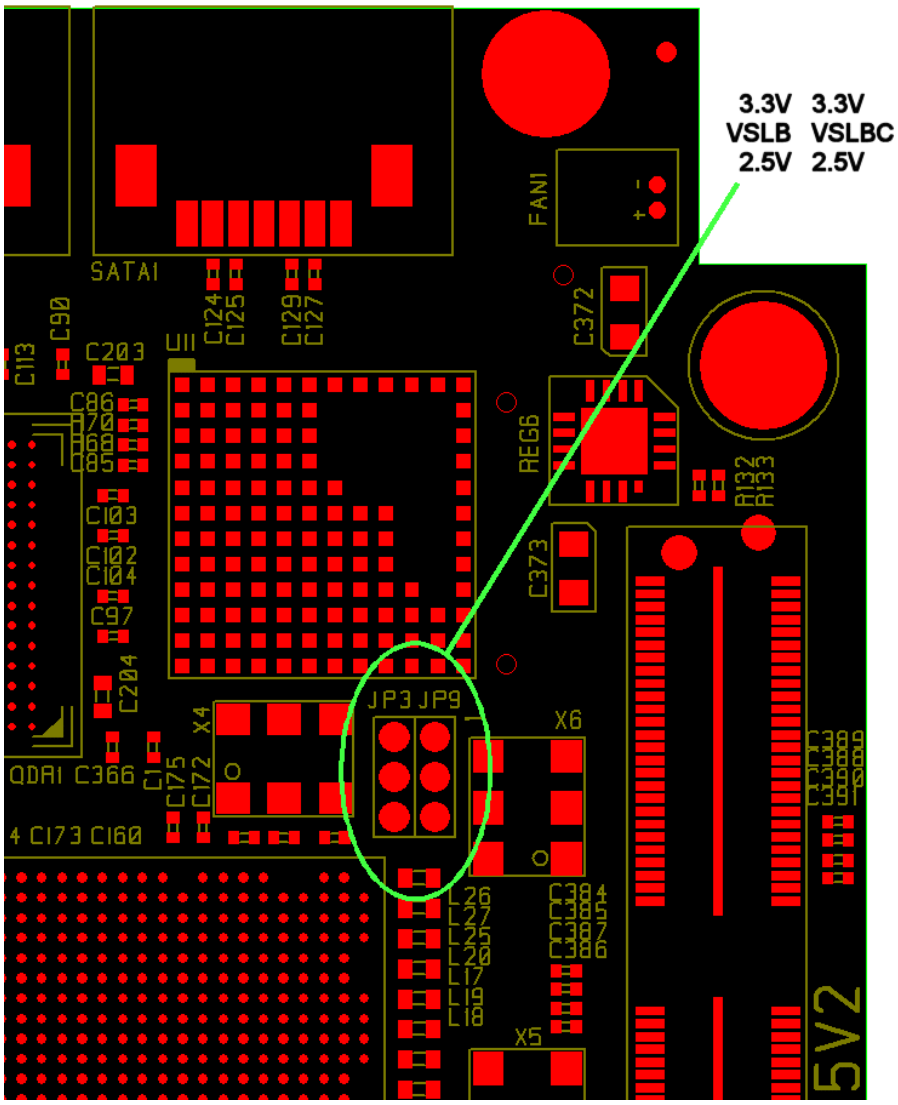
4.2.16.2 JP8

Insert JP8 to enable access to Cypress USB E²PROM.

4.2.16.3JP3 & JP9

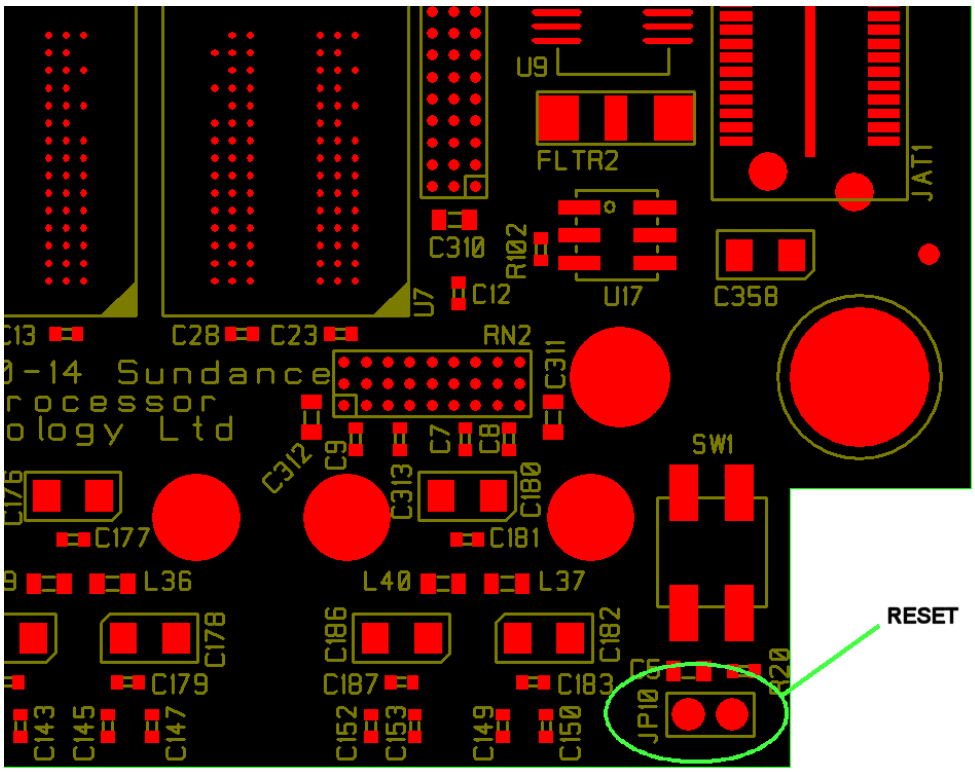
JP3 is used to select the FPGA SLB I/O voltage for the data pins (either 3.3 or 2.5).

JP9 is used to select the FPGA SLB I/O voltage for the control pins (either 3.3 or 2.5).



4.2.16.4JP10 & SW1

JP10 is used to inject an external reset (active low) signal. Left pin is GND, right pin is /RESET_IN.



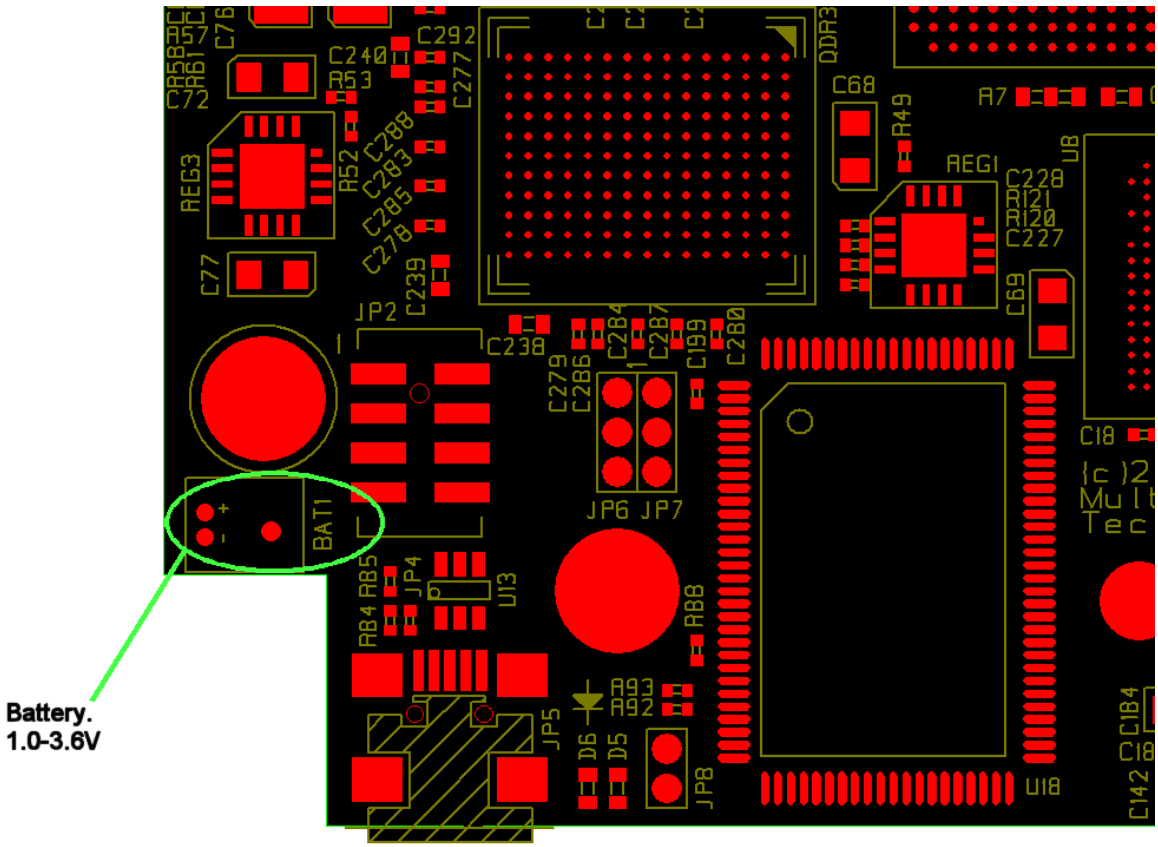
Either pressing SW1 or shorting JP10 will cause an active low reset to the FPGA pin AH17.

4.2.17 DIP Switch Function

Switch SW2	Function
1	Reset select. ON: hardware. OFF: software.
2	Bit file position. ON: default position 0. OFF: User position 1. See SMT6002.
3	ON: Erase/Program flash. OFF: Direct load FPGA via USB.
4	Link mode. ON: PCI/PCIe. OFF: USB.

Switch SW3	Function
1	BYTE_MODE. Do not alter.
2	SPROG. Do not alter.
3	unused
4	unused

4.2.18 BAT1 Connector



BAT1 is used to supply a 1.0 to 3.6V DC supply. It is only required if bitstream encryption is enabled. The security key is held within the FPGA in a battery backed location.

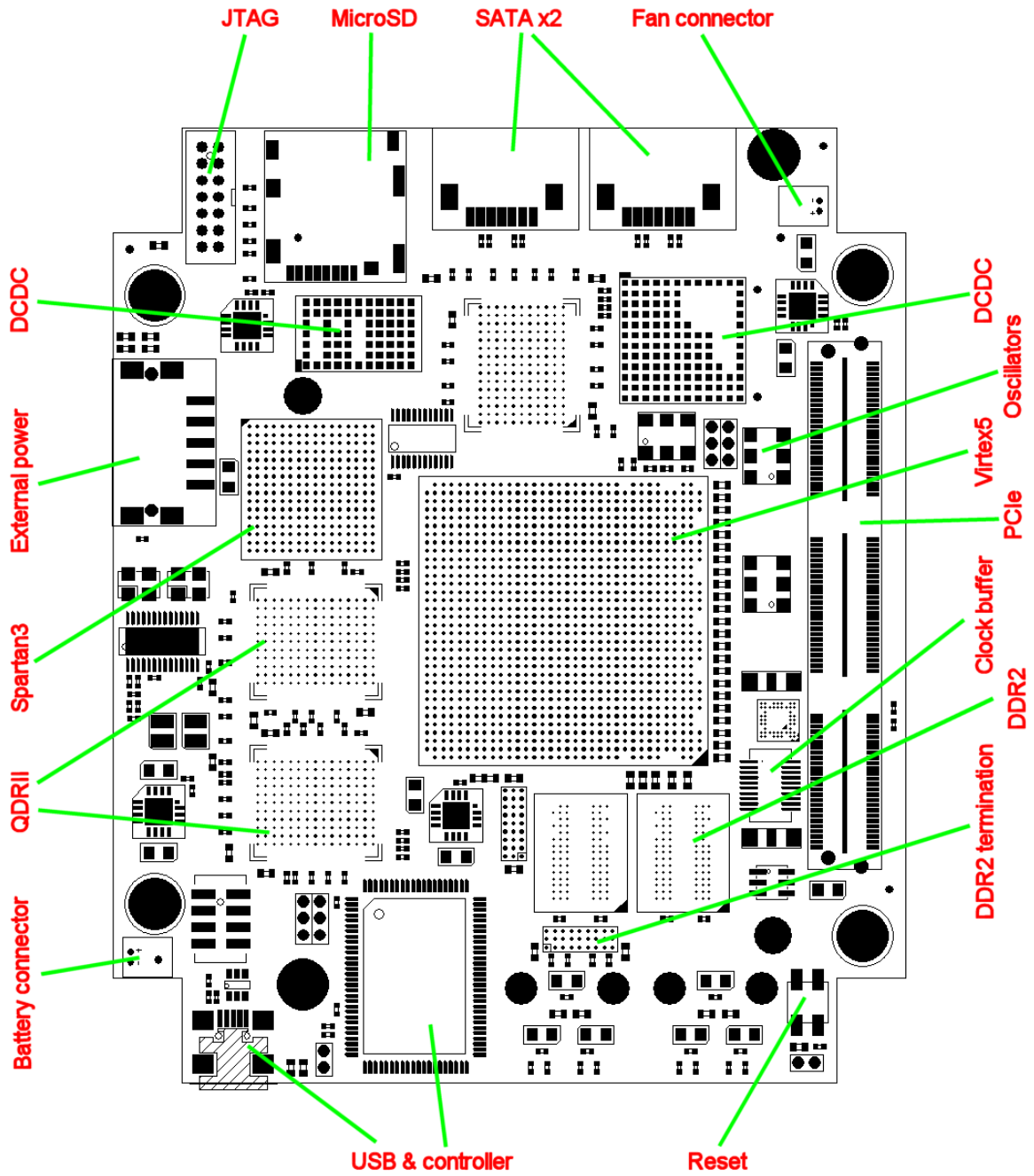
5 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

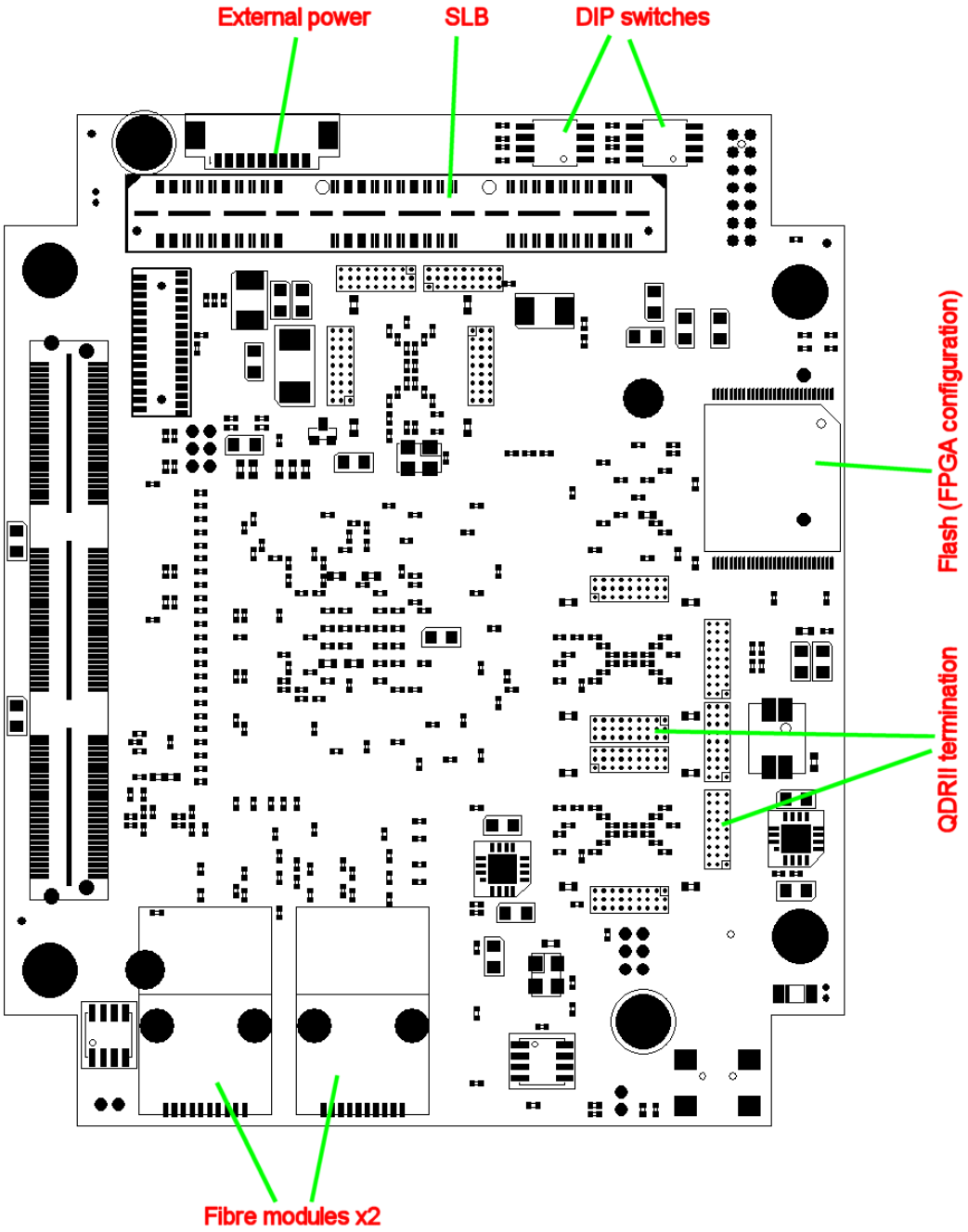
6 Circuit Description / Diagrams

7 Footprint

7.1 Top View



7.2 Bottom View



8 Support Packages

SMT6002 Sundance Flash Programming Utility.

SMT6048 Sundance USB Driver.

3L Diamond FPGA.

9 Physical Properties

Dimensions	95.9mm	115.6mm

Weight	

Voltage	Current (estimate)
+12V	100mA
+5V	1000mA
+3.3V	500mA
-5V	0
-12V	0

MTBF	

Note that the above current requirements are estimates and actual values depend entirely on Virtex 5 configuration, memory utilisation, and type of SLB fitted.

10 FPGA Pin Allocation

Sub-system	Pin name	Pin count	Instances	Total
SLB	All	109	1	109
LEDs & TTL	All	10	1	10
Configuration	Data	8	1	8
DDR2	Address	19	1	71
	Data (inc DQM)	40		
	Control (inc DM)	12		
QDRII	Address	20	3	315
	Data	72		
	Control	13		
Misc	Switch, RESET_IN	5	1	5
PCIe	All	8	1	8
Fibre	All	2	2	4
MicroSD	All	7	1	7
			TOTAL	**537**

11 Safety

This module presents no hazard to the user when in normal use.

12 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

13 Ordering Information

Order number:

SMT105