Sundance Multiprocessor Technology Limited **User Guide**	Form : QCF51 Dated : 20 December 2001 Revision : 5.1 Approved : Mark Ainsworth

Unit / Module Name:	SMT123-SHB
Unit / Module Number:	
Used On:	
Document Issue:	
Date:	

CONFIDENTIAL

Approvals		Date
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Revision History

	Changes Made	Issue	Initials
	First version	**1.0**	**AL**
11/06/04	**Added Weight, power consumption and MTBF**	**1.1**	**AL**

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1 Introduction

1.1 Overview

The SMT123-SHB is designed as a multi-purpose two-way Fibre-Channel interface. It is a stand-alone board with a Sundance SHB connector, that provides two separate 16-bit data channels, one each way, through the Fibre-Channel hardware. This allows rapid bi-directional transfer of Sundance SDB or Sundance SHB data between two systems over a distance of up to 500m. It also enables the communication with any other Fibre-Channel systems by giving a simple data interface between a Fibre-Channel device and any number of DSPs or FPGAs in the Sundance product range.

The Fibre Channel link operates at 2.125Gbits/s (or 1.0625), and allows a maximum data rate of 212.5MB/s in each direction.

The SMT123-SHB is powered by a PC floppy-drive power connector socket and is supplied with an adapter for a hard disk power connector, to allow the board to be run by an external power supply for stand-alone use.

1.2 Related Documents

- E2O Communications Inc EM212-L3Tz Datasheet
- Vitesse FibreChannel IC - VSC7146 Data Sheet
- SHB Technical Specification
- Virtex-II Data sheet

- Functional Description

1.3 Block Diagram

Figure 1 below shows the data-flow through the board. Serial data to and from the two Fibre Channel connectors is passed through a Vitesse Semiconductor VSC7146 Serialiser / Deserialiser IC, and then to or from the Xilinx Virtex-II FPGA, XC2V250–4) Virtex-II Data Sheets on a pair of 20-bit busses. The FPGA codes the data in a 10b/8b format for transmission through the fibre link and does the reverse on received data.

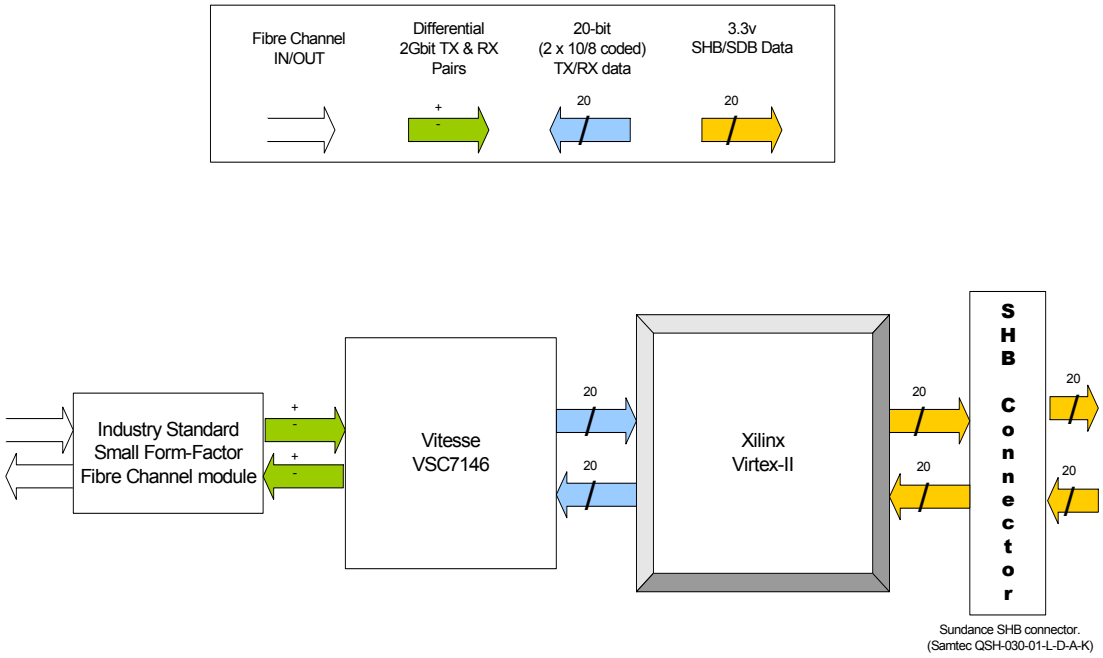

Figure 1 - Data Flow Diagram

1.4 Physical Description

The board is 100mm x 100.4mm. The shape of the board is designed to fit into a PCI slot although no physical connections to such bus are available. An industry standard “SFF” (Small Form-Factor) Fibre Channel module is fitted onto the board and protrudes from the front end for connection of the fibre cables. It uses the Industry Standard LC Optical Connector. The board requires only 5V supplied through a 4-pin 0.1” header compatible with standard floppy disk power connectors (J5). An on-board power conversion section derives the other voltages required on the board, i.e. 3.3v and 1.5v.

1.4.1 Board Layout

Figure 2 below shows the layout of the board. Throughout this document, wherever “left, right, top or bottom” are referred to in reference to the card, it is assumed that the card is in the orientation shown in this diagram.

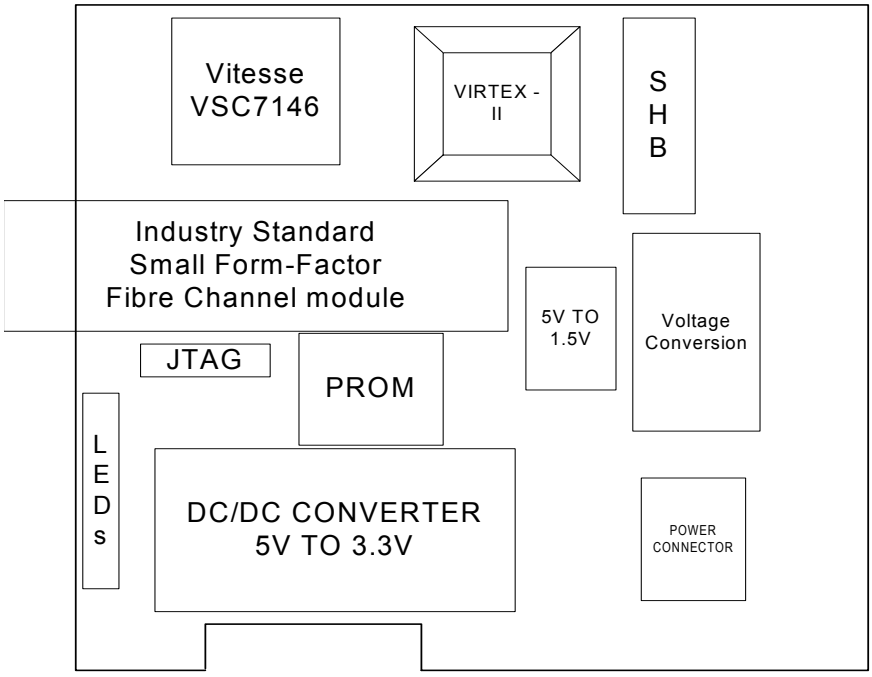

Figure 2 - Board Layout

1.5 Circuit Diagrams

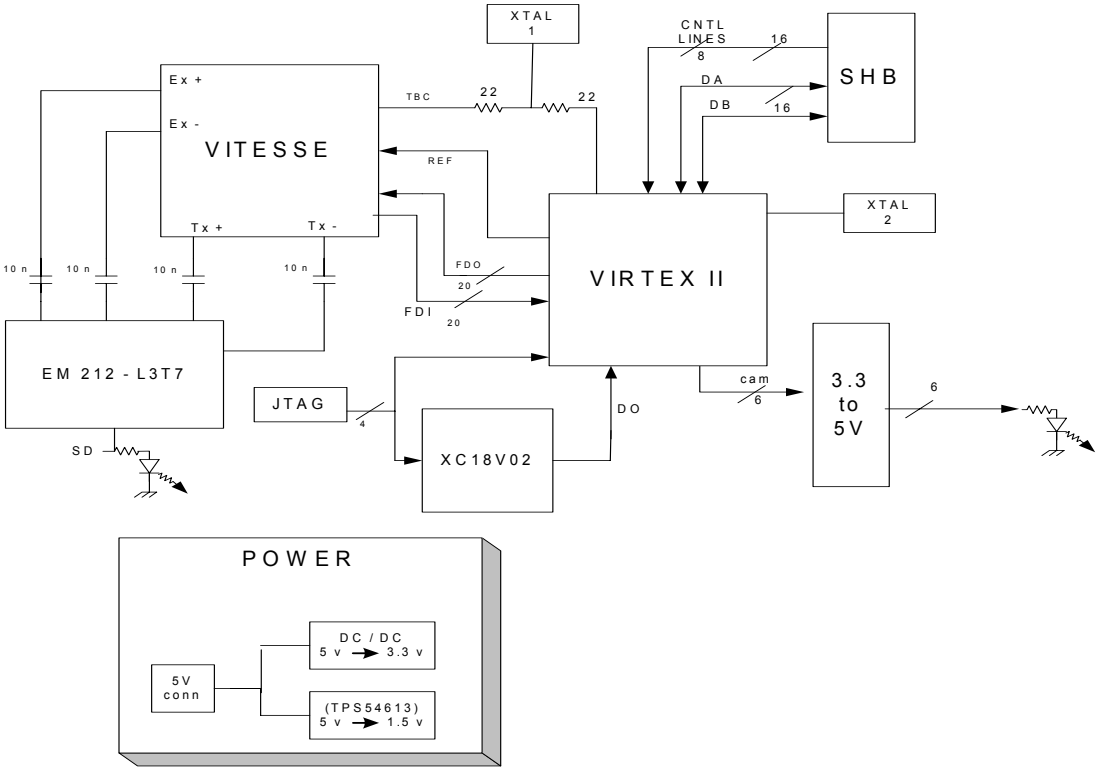

Figure 3 - Circuit Diagram

1.5.1 LED Indicators

A bank of 8 LEDs is situated on the left edge of the board (as shown on the left of **Figure 2**), which indicate that the board has power, and the status of the fibre link (blue LED).Table 1 below shows the arrangement of the LEDs, their meaning, and the FPGA pin with which they are driven. Most of them are meant to help the users to debug their applications.

Reference	Name	Meaning	FPGA pin that drives it
D4	Cam1	USER defined	T10
D5	Cam2	USER defined	R10
D6	Cam3	USER defined	T9
D7	Cam4	USER defined	R9
D8	Cam5	USER defined	P9
D9	Cam6	USER defined	N9
D10	SMURF	Link valid	T3
D11	RUDOLPH	FPGA not programmed	N/A

Table 1 LEDs (the background of each row indicates the colour of the LED)

2 Timing Diagrams

The VSC7146 needs to be provided with two separate clock signals: REF and TBC which must not have their opposing edges coincident within 2.0 ns of each other as illustrated in Figure 4. (T1 and T2 must be minimum 2ns). The REF signal comes straight to its corresponding pin of the Vitesse chip from the crystal though a small resistor, whereas TBC signal is the same clock passed through the Virtex II. It is connected to the pin N8 of the FPGA and the delay may be adjusted by using the DRC characteristics of this chip.

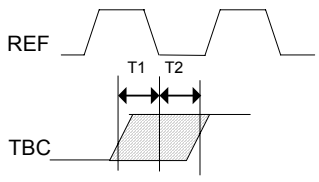

Figure 4 - TBC and REF Timing Waveforms

3 Electrical Interface

Table 2 below shows the pinout of the Sundance High Speed Bus board connector (SHB). For more information about the connector and its interface, please refer to SHB_Technical_Specification .

Hw	FPGA Pin	QSH Pin number	QSH Pin number	FPGA Pin	Hw
CLK	B8	1	31		
D0	D6	2	32		
D1	E7	3	33		
D2	C6	4	34		
D3	E6	5	35		
D4	B6	6	36		
D5	C7	7	37	A9	CLK
D6	A6	8	38	C12	D0
D7	D7	9	39	D9	D1
D8	B5	10	40	D12	D2
D9	A7	11	41	C9	D3
D10	A5	12	42	B13	D4
D11	B7	13	43	B9	D5
D12	C4	14	44	C13	D6
D13	F15	15	45	B10	D7
D14	B4	16	46	A12	D8
D15	C8	17	47	A10	D9
		18	48	B12	D10
		19	49	D10	D11
		20	50	A11	D12
		21	51	C10	D13
WEN	D5	22	52	B11	D14
REQ	D8	23	53	E11	D15
ACK	C5	24	54		
		25	55		
		26	56		
		27	57		
		28	58	C11	WEN
		29	59	E10	REQ
		30	60	D11	ACK

Table 2 - Sundance High Speed Bus connector pinout

4 CLOCKs

The board contains two crystals to allow data transfer through the fibre module and/or the SHB connector to other boards. The fibre module operates at 53.125MHz (half speed) or 106.25 MHZ (full speed). This corresponds to the REF signal mentioned in section 2 of this document. There are 3 resistors that play a key role to achieve proper operation of the VSC7146 according to the value of this crystal (X1 on the component side):

Resistor	Speed	Position
R19	HALF	0
	FULL	1
R20	HALF	0
	FULL	1
R25	HALF	1
	FULL	0

The SHB interface is usually clocked at 50 or 100 MHz (X2 on the bottom of the board) and it is connected to the FPGA pin **A8**.

5 PCB Layout Details

5.1 Component Side

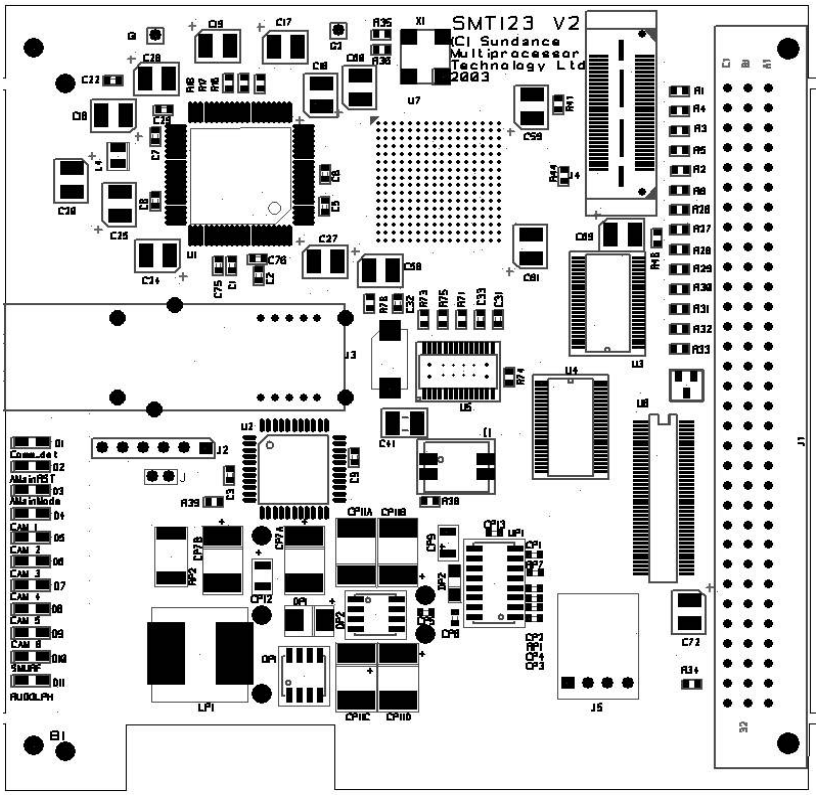

Figure 5 – PCB Layout, Top

5.2 Solder Side

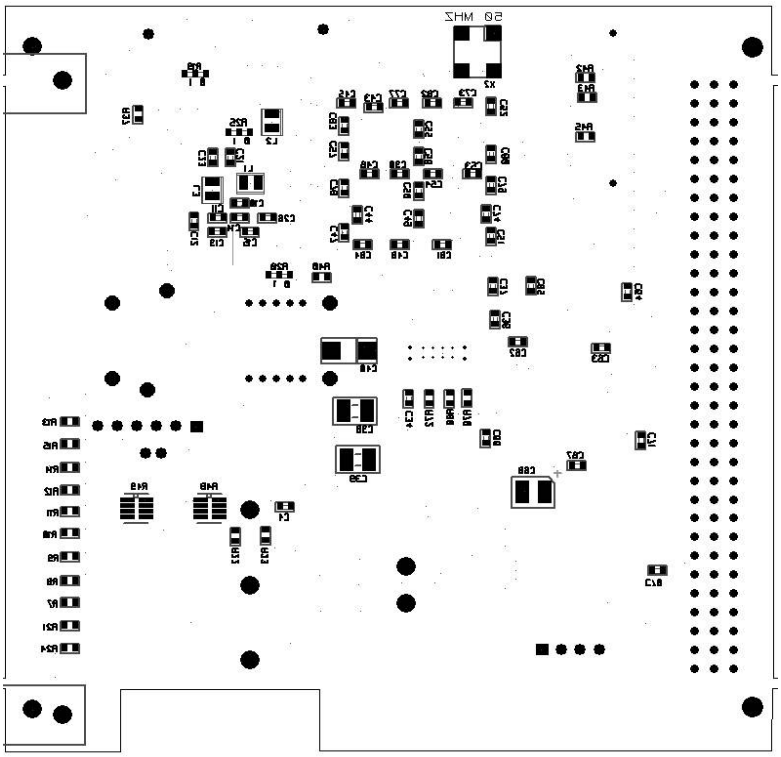

Figure 6 – PCB Layout, bottom

6 Pinout table

Table 3 shows the connections between the VSC7146 and the Virtex:

VSC7146	FPGA pin
T0	N3
T1	N2
T2	M4
T3	M3
T4	M2
T5	M1
T6	L4
T7	L3
T8	L2
T9	L1
T10	L5
T11	K5
T12	K4

T13	K3
T14	K2
T15	K1
T16	J4
T17	J3
T18	J2
T19	J1
R0	H3
R1	H4
R2	G1
R3	G2
R4	G3
R5	G4
R6	G5
R7	F5
R8	F1
R9	F2
R10	F3
R11	F4
R12	E1
R13	E2
R14	E3
R15	E4
R16	D2
R17	D3
R18	D1
R19	C1
RBC	T6
TBC	N8
REF	R8
EWRAP	P6
EN_CDET	N6

Table 3 – VSC7146 to FPGA connections

Additionally, the signal **SD** coming from the fibre module is connected to the pin **T4** of the FPGA and this signal will go high when the link is usable.

Pin 8 of the EM212 corresponds to TX_dis signal. It must be driven LOW from pin P1 of the FPGA in order to enable the fibre module.

7 JTAG

There is a 6-pin header (J2) to allow JTAG programming. Pin 1 of the header is on the right hand side (square pad).

6	5	4	3	2	1
TMS	TDI	TDO	TCK	GND	VCC

8 Weight

The board weights up to 70g (0.154 pounds)

9 Power Consumption

The board consumes approximately 3W during normal operation.

10 Safety

This module presents no hazard to the user.

11 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system that may be introduced through the output cables.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.