

# SMT145

## User Manual



Certificate Number FM 55022

## Revision History

<b>Date</b>	<b>Comments</b>	<b>Engineer</b>	<b>Version</b>
06/03/06	First revision	JPA	1.0
29/09/06	Corrected JP6 pinout	JPA	1.1

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## **Contacting Sundance**

You can contact Sundance for additional information by login onto the support system [support.sundance.com](https://support.sundance.com)

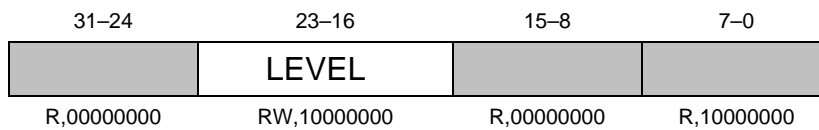
## Notational Conventions

### C60

The terms C60, C64xx and TMS320C64xx will be used interchangeably throughout this document.

### Register Descriptions

The format of registers is described using diagrams of the following form:



The digits at the top of the diagram indicate bit positions within the register and the central section names bits or bit fields. The bottom row describes what may be done to the field and its value after reset. Shaded fields are reserved and should only ever be written with zeroes.

- R            Readable by the CPU
  - W            Writeable by the CPU
  - RW          Readable and writeable by the CPU
- Binary digits indicate the value of the field after reset.

## Outline Description

The SMT145 is a single site TIM compatible PCI 64-bit carrier card. The card allows data transfer up to 533MB/s<sup>1</sup> between the host machine and the SMT145.

The TIM plugged on the SMT145 may use a comport (20MB/s) or an RSL (about 1GB/s) to communicate with the SMT145.

The SMT145 has JTAG connections for the carrier itself and for the TIM site.

## Features

- 66MHz/64bit PCI interface
- 1-2Gbit/s fibre interface with 8b/10b codec (optional)
- Input stream decoder and ZBTRAM manager (optional)
- Optional [PCI Express](#) interface
- Sundance [SHB](#) (2x16 bit, 1x32 bit) interface (optional)
- Sundance [RSL](#) (Rocket IO) interfaces
- Buffered external [ComPorts](#) (optional)
- Un-buffered internal [ComPorts](#)
- TIM Global Bus connector (optional)

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<sup>1</sup> The current implementation is 32-bits only and allows data rate of 230MB/s



## Block Diagram

The SMT145 has a PCI 64-bits 66MHz core that allows data transfer of 533 MHz between the host machine and the carrier board.

An RSL connection between the SMT145 and the TIM plugged onto it allows data transfer close to 1GB/s.

A comport connection between the SMT145 and the TIM plugged onto it allows the use of TIMs that don't have RSL and provides a data rate of about 20MB/s.

The picture is the block diagram of the SMT145. The features shown in yellow are supported by the standard SMT145. The features shown in blue are available only with the SMT145-FC. The features hatched are not available yet or available on request.

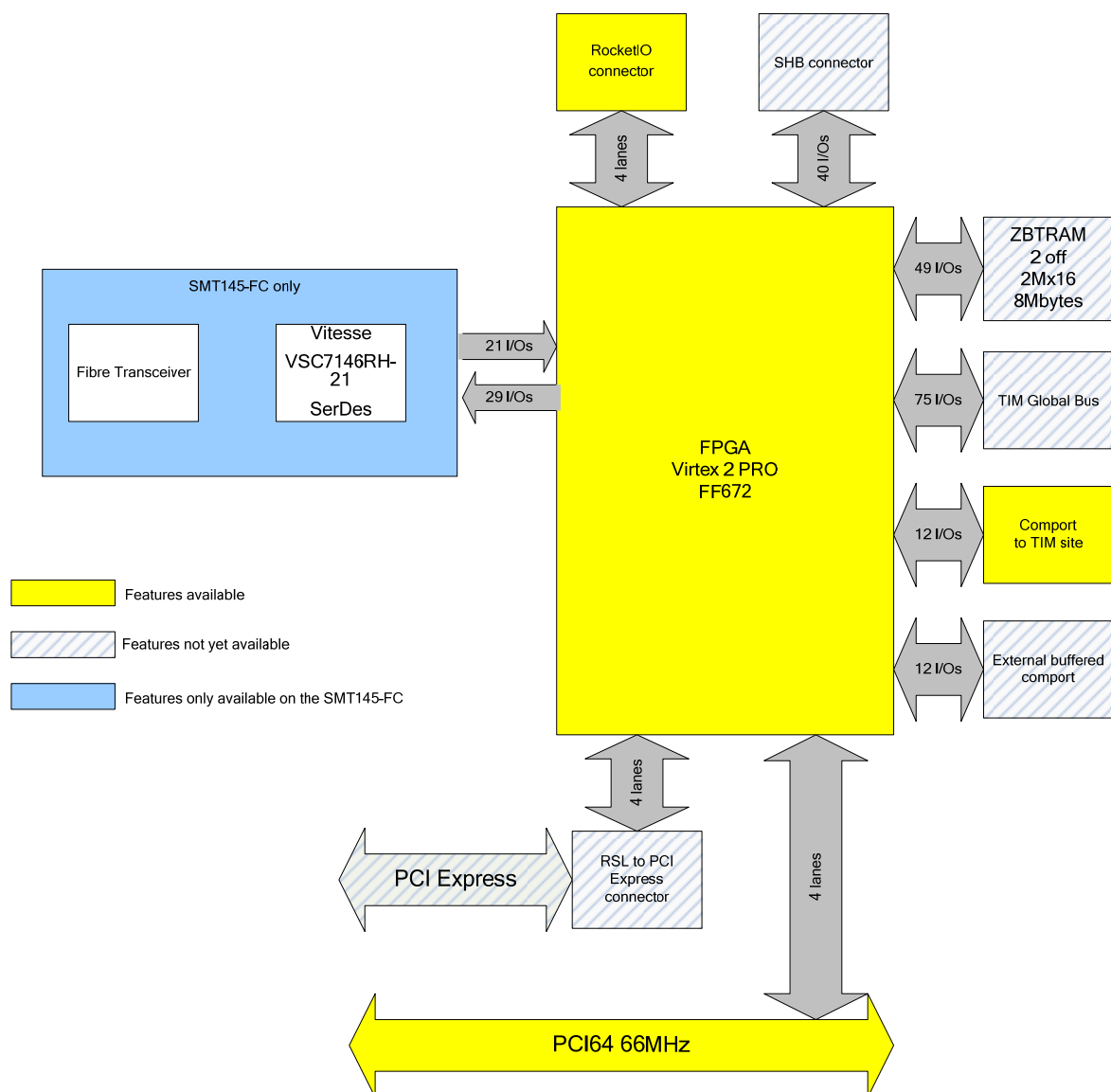


Figure 1: SMT145 block diagram

From the software point of view, the RSL and comport are accessible from the host machine via the X-Link interface.

### ***FPGA***

A Xilinx VirtexII-Pro VP7 FPGA is used for the control of the RSL, the comport and the PCI interface.

### ***PCI***

The PCI interface is provided by a PCI core within the FPGA. This is a 64-bit PCI device which runs at up to 66MHz allowing for transfer rates of about 533Mbytes/s between the SMT145 and the host machine.

### ***RSL***

One RSL connector is connected to the FPGA via four Rocket IO lanes. This connector allows data transfer close to 1GB/s with the TIM plugged on the SMT145.

The [RSL specification](#) gives more details.

### ***Comport***

A host comport allow data transfer between the host machine and the TIM. The data rate is about 20MB/s.

There are five comport connectors available on the SMT145. They are connected directly to the comport of the TIM. They are available through connectors JP1, JP2, JP4, JP5 and JP8.

JP1 connects to TIM comport 0.

JP2 connects to TIM comport 4.

JP4 connects to TIM comport 1.

JP5 connects to TIM comport 5.

JP8 connects to TIM comport 2.

### **JTAG**

The SMT145 provides JTAG connection for both the carrier itself and the TIM site.

There are three JTAG connectors available.

#### ***JTAG for the TIM***

The SMT145 doesn't have an on-board JTAG controller. To be able to access the TIM plugged on the SMT145 via JTAG, a JTAG emulator must be connected to the connector [JTAG1](#). Various emulators are available:

- XDS510
- XDS560

It is also possible to connect another Sundance carrier to this connector. For example you may connect the JTAG output of an SMT310Q to the connector JTAG1 of the SMT145. In that case the TIMs plugged on the carriers connected via JTAG are in the same JTAG chain.

The connector JTAG2 provides a JTAG output. It is used to connect different carrier boards in the same JTAG chain. For example you may connect the connector JTAG2 to the connector JTAG1 of another SMT145 or to the input JTAG connector of a SMT310Q.

Code Composer Studio drivers are available from Sundance, Part Number [SMT6012](#).

### ***JTAG for the SMT145***

The FPGA and the PROM of the SMT145 are in the same JTAG chain.

The connector [JP6](#) is used to access these components.

### **Configuration of the FPGA**

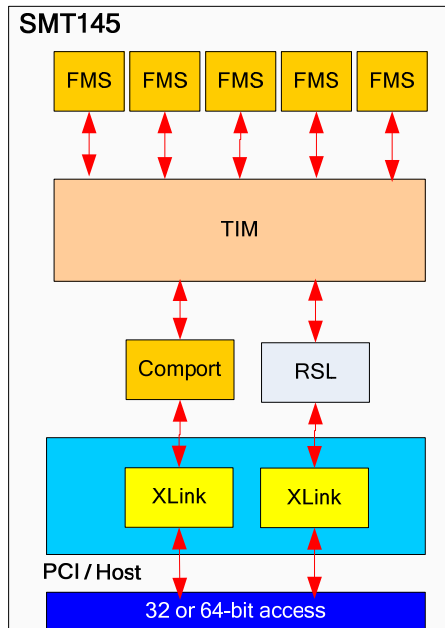
When the SMT145 is powered up the FPGA is configured with a bitstream stored inside the on-board PROM. The bitstream is loaded in the PROM via the JTAG header [JP6](#).

It is also possible to configure the FPGA directly using the JTAG header JP6.

Software Xilinx iMPACT is used for the configuration of both devices.

### **Software**

The diagram shows functionally how the SMT145 works. The host accesses a number of communication resources via the PCI bus. All communication resources are presented as X-Link software interfaces, and are memory mapped in the memory space of the host processor.



**Figure 2: software design**

### ***Driver***

The SMT145 is supported by the SMT6300 that provides the Windows driver for the board.

### ***Registers***

All the addressable resources are located in the BAR1.

The communication resources are presented to the host machine as X-Link interfaces. The addresses of the X-Link and the number of X-Link are available from the X-Link table of content.

Refer to the X-Link documentation for the description of the registers of the X-Link.

The other registers available in the firmware are the following:

#### Reset register (BAR1 – 0x00000000)

Writing '1' to the reset register will cause the SMT145 and the TIM plugged on it to be reset. The reset is de-asserted automatically after few milliseconds.

#### X-Link table of content (BAR1 – 0x00000400)

Refer to the X-Link documentation for the details of the table of content.

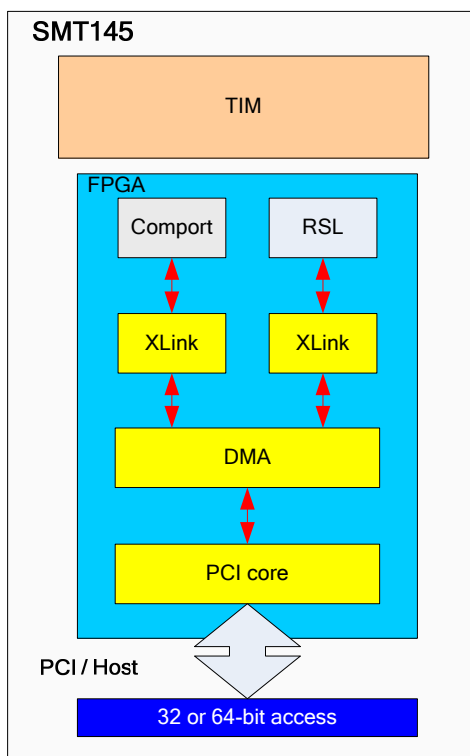
## Firmware

This section deals with the design of the FPGA available on-board the SMT145.

The firmware implements the communication interfaces required to allow the data transfer between the SMT145 and the TIM and the SMT145 and the PCI.

The host transfers data with the TIM using the X-Link. There is one X-Link instantiated per communication resource (SHB, RSL). All the X-link are connected to the PCI core and can be accessed from the host. The default firmware provides two communication resources: one comport and one RSL. Refer to the SMT6400 and SMT6500 for more information concerning the communication resources.

A PCI core is used to allow data transfer between the host machine and the X-Link.



**Figure 3: FPGA design**

The PCI core supports target accesses and initiator accesses. Data transfers are implemented using initiator accesses to ensure maximum bandwidth. For this purpose a DMA engine is connected to the X-Link and the PCI core to transfer the data.

## Operating Conditions

### **Safety**

The module presents no hazard to the user.

### **EMC**

The module is designed to operate within an enclosed host system that provides adequate EMC shielding. Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system.

The module is protected from damage by fast voltage transients introduced along output cables from outside the host system.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.

### **General Requirements**

The module must be fixed to a TIM40-compliant carrier board.

The SMT395 TIM is in a range of modules that must be supplied with a 3.3v power source. In addition to the 5v supply specified in the TIM specification, these new generation modules require an additional 3.3v supply to be presented on the two diagonally-opposite TIM mounting holes. The lack of this 3.3v power supply should not damage the module, although it will obviously be inoperable; prolonged operation under these circumstances is not recommended.

The SMT395 is compatible with all Sundance TIM carrier boards. It is a 5v tolerant module, and as such, it may be used in mixed systems with older TIM modules, carrier boards and I/O modules.

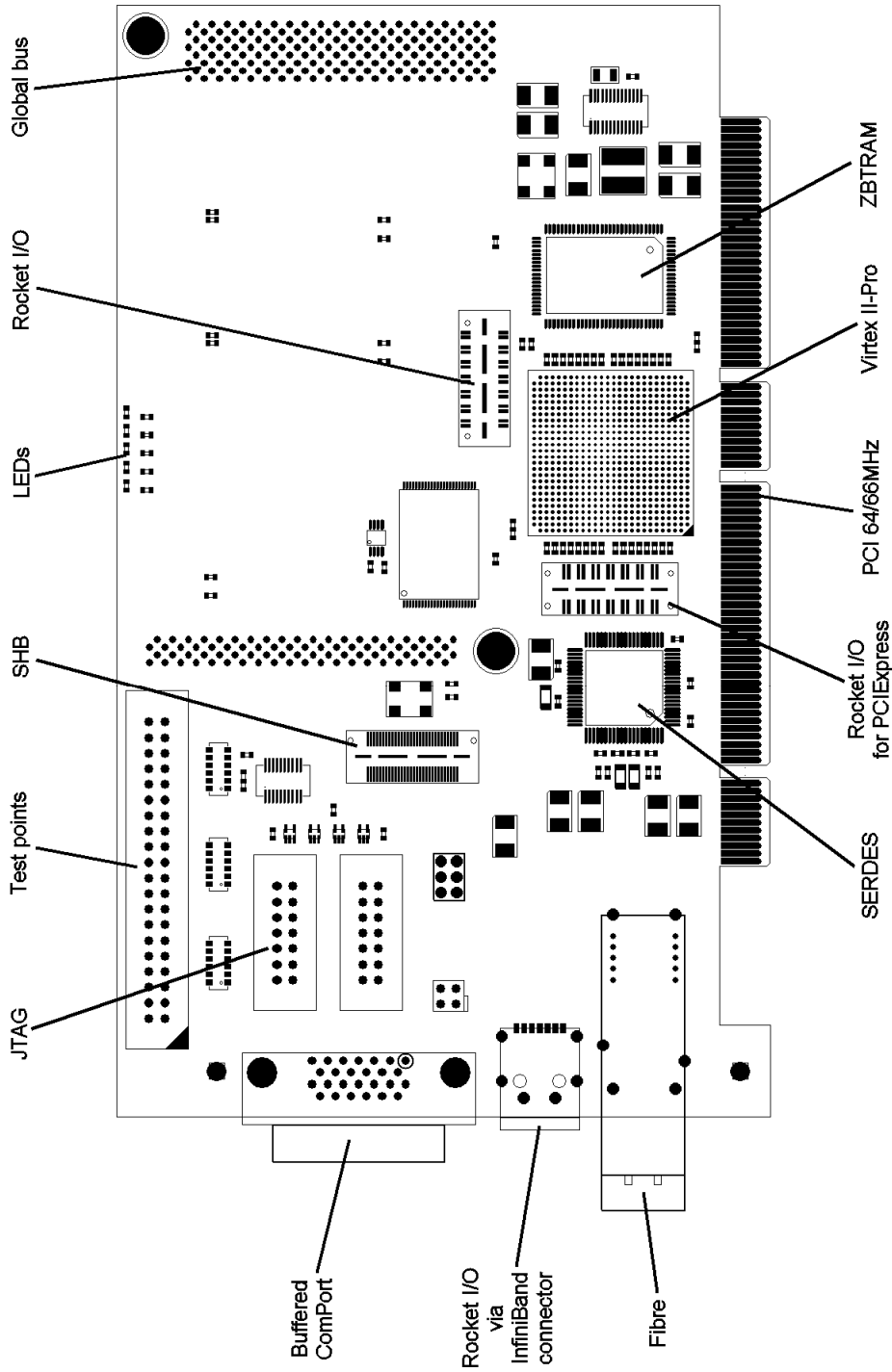
Use of the TIM on SMT327 (cPCI) motherboards may require a firmware upgrade. If the top right LED on the SMT395 remains illuminated once the TIM is plugged in and powered up, the SMT327 needs the upgrade. The latest firmware is supplied with all new boards shipped. Please contact Sundance directly if you have an older board and need the upgrade.

The external ambient temperature must remain between 0° C and 40° C, and the relative humidity must not exceed 95% (non-condensing).

### **Power Consumption**

The power consumption of this TIM is dependent on the operating conditions in terms of core activity and I/O activity.

# PCB description



## Connectors pinout

### **JP6**

3	2	1
TCK	GND	VCC
6	5	4
TDO	TDI	TMS

Pin Number	Function
1	Vcc (3.3v)
2	Gnd
3	TCK
4	TMS
5	TDI
6	TDO

### **JTAG1**

### **JTAG2**



## Bibliography

1. The X-Link:  
<http://support.sundance.com/Pub/documentation/pdf-files/X-Link.pdf>
2. TIM-40 MODULE SPECIFICATION Including TMS320C44 Addendum  
[http://support.sundance.com/Pub/documentation/pdf-files/tim\\_spec\\_v1.01.pdf](http://support.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf)
3. SDB Technical Specification  
[http://support.sundance.com/Pub/documentation/pdf-files/sdb\\_tech\\_spec.pdf](http://support.sundance.com/Pub/documentation/pdf-files/sdb_tech_spec.pdf)
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