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Product Specification for SMT148FX

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Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	14/9/06	GKP
1.0.1	Added FPGA pin allocation.	15/9/06	GKP
1.0.2	Added local clock description.	16/10/06	GKP
1.1.0	Minor clarifications.	2/11/06	GKP
1.2	Defined global bus as 16 bit data. Added OXUF922 for FPGA config and IEEE1394. Removed an external ComPort.	14/11/06	GKP
1.2.1	Added power supply capability in the physical properties section.	15/11/06	GKP
1.2.2	Changed FPGA config mode to CPLD select map. Removed OXUF922. Changed number of fan connectors to 4. Added thermal management section.	27/11/06	GKP
1.2.3	Added FPGA pinout drawing	29/11/06	GKP
1.3.0	Added USB connection to Spartan and CPLD. Removed a ComPort between Spartan and Virtex (now only 3).	4/12/06	GKP
1.3.1	Updated board layout.	6/2/07	GKP
1.3.1.1	Added EEPROM on board layout.	7/2/07	GKP
1.4	Added further detail on ComPort connectivity.	19/4/07	GKP
1.4.1	Clarified bullet points.	2/5/07	GKP

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1 Introduction

The SMT148FX is a four site stand-alone TIM carrier board with several external interfaces.

Connectors are provided to interface to:

- RS232 – From FPGA or USB controller
- LVDS (56 pairs)
- JTAG
- RSL
- SATA – Connectors carrying RSL signals only.
- SHB
- RS485 (16 pairs)
- USB2
- Firewire (1394) interface only (No IP core).
- Ethernet 10/100/1000
- LED (x32)
- ZBT memory
- Local clock buffer/generator output

2 Related Documents

2.1 Referenced Documents

Sundance SLB specification (hyperlink).

Sundance RSL specification (hyperlink).

Datasheets as specified above.

Texas Instruments Module specification.

SMT118: Carrier with 3 Module sites and I/O facilities.

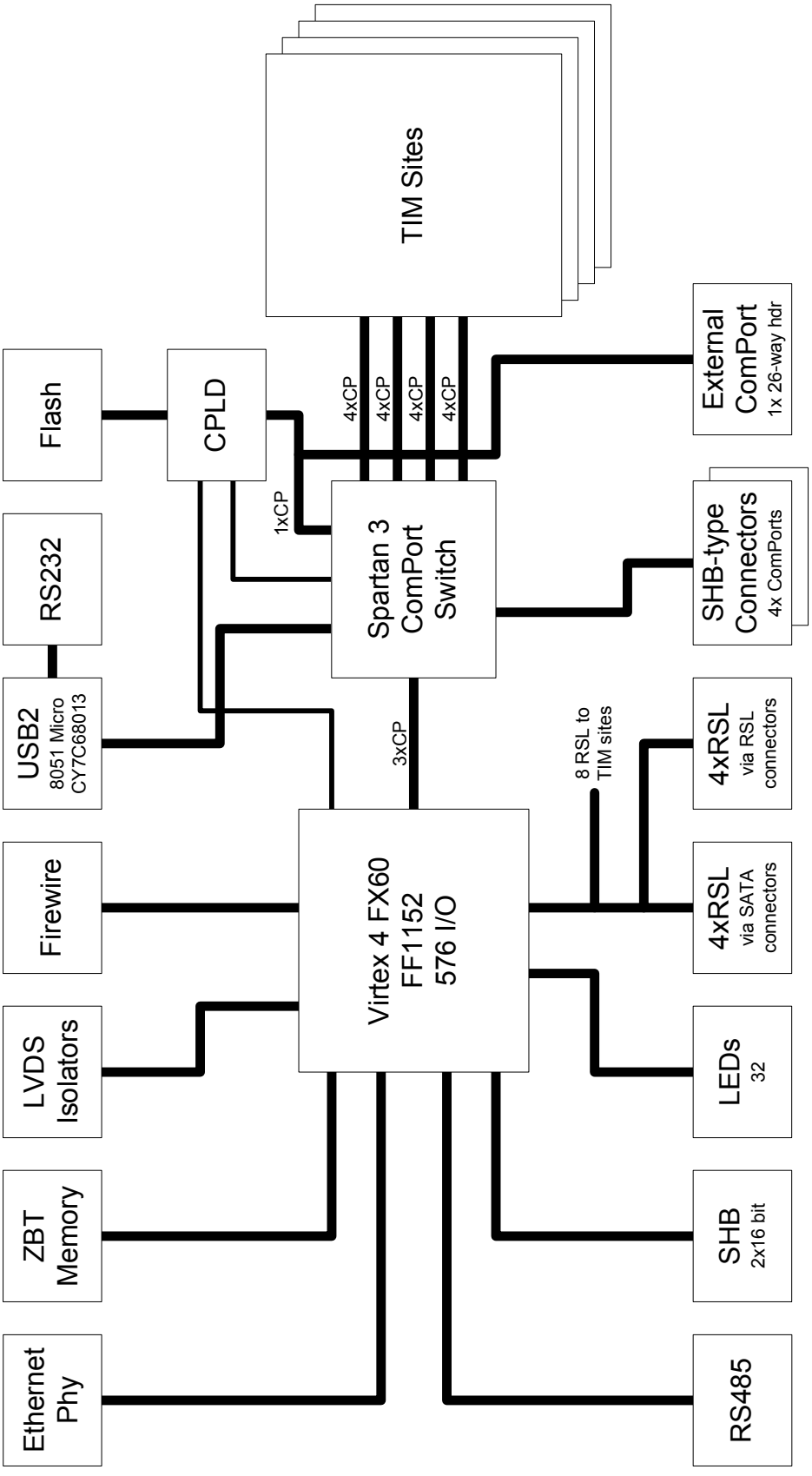
SMT180: Carrier with 8 Module sites.

3 Acronyms, Abbreviations and Definitions

A list of acronyms etc (hyperlink).

4 Functional Description

4.1 Block Diagram



4.2 Module Description

4.2.1 Virtex 4 FX

The primary controlling device on the 148FX is the Xilinx Virtex4 FX60 FPGA. This device is an FF1152 package which provides 16 MGTs (high speed serial I/O) and 576 normal I/O signals.

This device can be configured via a Xilinx compatible JTAG header.

In normal operation, this device is configured by CPLD (XC2C512). The configuration data is stored in flash memory, and is loaded using slave SelectMAP mode (8-bit parallel).

4.2.2 Spartan 3

The Xilinx Spartan 3 device is similar in nature to that employed on the SMT150Q and SMT329 carrier boards. It acts as a pre-configured ComPort routing switch. Different ComPort routing schemes are easy to implement using supplied tools (requires Xilinx ISE development software).

This device is also configured by the CPLD, and uses slave SelectMAP mode (8-bit parallel), but is also part of the Xilinx JTAG chain.

4.2.3 TIM Sites

The 148FX provides 4 TIM sites. In addition to the standard specification requirements, the 148FX also provides the 3.3V supply to the two TIM mounting holes.

Each TIM site has 4 ComPorts connected directly to the Spartan 3 device. The two remaining ComPorts are used to create a simple pipe, with each site connecting to its nearest neighbours.

The TIM site's interrupt, timer, config, and reset pins are all connected to the Virtex 4 FPGA. The reset signals are asserted during power-up, when pressing the on-board reset button, or when signalled to via one of the external ComPort connectors.

A global bus connection (16 bit data, 12 bit address) is also made from each site to the Virtex 4. The global bus connector normally contains one 16-bit SDB interface (this is unlike the TIM specification which describes the global bus as an Address, Data structure). These SDBs are the primary method of communication to the resources shared by the Virtex 4 (eg. USB, Firewire, etc).

4.2.4 10/100/1000 Ethernet Phy

A Marvell Ethernet PHY connects directly to the Virtex 4 FPGA. This interfaces to a 10/100/1000 network via a standard RJ45 socket. This socket has built-in magnetics to save board space.

The PHY is controlled by a MAC within the Virtex 4.

4.2.5 LVDS Isolators

48 single ended signals are connected from the Virtex 4 to LVDS drivers and receivers (SN65LVDS390/1) via galvanic isolators (type IL715-3). The transmitter part is enabled via control signals. The LVDS outputs are arranged in groups of 6., hence there are 8 control signals. The LVDS receivers are enabled continuously.

The isolation provided is up to 150V rms, whilst still enabling a baud rate of up to 100Mbps.

Typically. The TIMs are configured to route their McBSPs to the global bus connector pins, which, in turn, are routed to the LVDS I/O. The following table shows the pin-out for the 37-way D-type connectors.

1	GND	Input/Output	20	GND
2	McBSP_CLKR_Tx_0+	I	21	McBSP_CLKR_Tx_0-
3	McBSP_FSR_Tx_0+	I	22	McBSP_FSR_Tx_0-
4	McBSP_DR_Tx_0+	I	23	McBSP_DR_Tx_0-
5	GND		24	GND
6	McBSP_CLKX_Tx_0+	O	25	McBSP_CLKX_Tx_0-
7	McBSP_FSX_Tx_0+	O	26	McBSP_FSX_Tx_0-
8	McBSP_DX_Tx_0+	O	27	McBSP_DX_Tx_0-
9	GND		28	GND
10	GND			
11	GND		29	GND
12	McBSP_CLKR_Tx_1+	I	30	McBSP_CLKR_Tx_1-
13	McBSP_FSR_Tx_1+	I	31	McBSP_FSR_Tx_1-
14	McBSP_DR_Tx_1+	I	32	McBSP_DR_Tx_1-
15	GND		33	GND
16	McBSP_CLKX_Tx_1+	O	34	McBSP_CLKX_Tx_1-
17	McBSP_FSX_Tx_1+	O	35	McBSP_FSX_Tx_1-
18	McBSP_DX_Tx_1+	O	36	McBSP_DX_Tx_1-
19	GND		37	GND

4.2.6 Firewire

A single IEEE1394 interface is provided by an Agere FW801A PHY. The following table shows the pinout of the connector;

1	Cable Power
2	GND
3	TPB-
4	TPB+
5	TPA-
6	TPA+

This will allow high speed firewire data to be routed directly to the FPGA.

4.2.7 USB2

The USB2 interface is provided by the Cypress CY7C68013A device.

The Cypress part, in addition to providing USB functions with a FIFO type interface, also contains a USART, and an 8051 micro-controller.

The USB connector pin-out is shown here;

1	USB_ind
2	Data-
3	Data+
4	GND

The interface provided by this controller looks identical to a 16-bit SDB interface, and is routed directly to the Spartan FPGA and the CPLD.

The following table shows the Cypress pin connectivity to the Sundance SDB signal;

SDB Signal	Cypress Pin
CLK	IFCLK
D0	PB0
D1	PB1
D2	PB2
D3	PB3
D4	PB4
D5	PB5
D6	PB6
D7	PB7
D8	PD0
D9	PD1
D10	PD2
D11	PD3
D12	PD4
D13	PD5
D14	PD6
D15	PD7
WEN	RDY0
REQ	CTL2
ACK	RDY1
UD0	PA7
UD1	RDY3

4.2.8 RS232

Three devices generate RS232 data (simple TX and RX) from the FPGA and USB2 controller.

The Rx data pin from a 9-way D-type connector is connected to all three serial interfaces. The Tx data pin from each device is routed to a jumper block which allows the selection of one Tx data output. The RS232 levels are generated using a MAX3227 converter.

1	DCD
2	Rx
3	Tx
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

4.2.9 Flash

The flash memory connected to the CPLD and contains configuration data for the two FPGAs.

Any additional space within this device can be used to store application programs.

The flash can be directly programmed by the CPLD only.

The external ComPort is directly connected to the CPLD. This allows the reprogramming of the flash using an identical procedure as that employed on the SMT348. After configuration, the CPLD ComPort is tri-stated and the external ComPort functions as an input to the ComPort switch (Spartan 3).

4.2.10 RS485

Each of the 16 RS485 signal pairs is driven by an SN75HVD12. They are arranged into two groups of 8-bits each and have a single control signal which selects the group to be a transmitter or receiver.

Function	pin	pin	Function
S0-	1	2	S0+
S1-	3	4	S1+
S2-	5	6	S2+
S3-	7	8	S3+
S4-	9	10	S4+
S5-	11	12	S5+
S6-	13	14	S6+
S7-	15	16	S7+
GND	17	18	GND
GND	19	20	GND

Function	pin	pin	Function
GND	21	22	GND
GND	23	24	GND
S8-	25	26	S8+
S9-	27	28	S9+
S10-	29	30	S10+
S11-	31	32	S11+
S12-	33	34	S12+
S13-	35	36	S13+
S14-	37	38	S14+
S15-	39	40	S15+

4.2.11 SHB

A single SHB connector (Samtec QSH-030-01) provides two independent 16-bit SDBs, or a single 32-bit SDB interface. These signals are connected directly to the FX60.

4.2.12 LEDs

32 LEDs are connected to the Virtex 4 FPGA in a matrix of 8x4.

4.2.13 ZBT Memory

Two 16-bit wide ZBT memories are connected directly to the FPGA. This provides a memory bank of 2Mx16 bits (4Mbytes).

4.2.14 RSL

The Virtex 4 FX FPGA provides 16 RSL (Rocket Serial Link) interfaces. 8 of these are connected to the 4 TIM sites (2 per site).

Four RSLs are connected to 4 SATA style connectors thus allowing inter-board connectivity.

The remaining 4 are presented on a standard RSL connector. See the RSL specification for details on the connector type.

4.2.15 External ComPorts

Four ComPorts are connected to SHB style connectors. Two output-type ComPorts (0 and 1), and two input-type ComPorts (3 and 4) are provided. All 4 ComPorts are connected to both SHB-style connectors. Connector A is arranged 0, 1, 3 and 4, and connector B 3, 4, 0 and 1. With this scheme, a simple one-to-one SHB cable can be used to connect connector A on one 148FX to connector B on another 148FX.

Another ComPorts is available via a 26-way connector, where cable SMT502 can be used to connect to a SMT310Q and download applications from a PC. This connector has the following pin-out.

1	CSTRB	2	GND
3	CRDY	4	GND
5	CREQ	6	GND
7	CACK	8	GND
9	D0	10	D1
11	D2	12	D3
13	D4	14	D5
15	D6	16	D7
17	3.3V	18	GND
19	/RESETOUT	20	GND
21	/RESETIN	22	GND
23	NC	24	NC

External Comports 0, 1, 3 and 4 are routed to two SHB connectors (Samtec QSH-030-01) to allow connection to another SMT148FX carrier and its ComPorts. The pin-out is as follow:

1	STRB_0	2	RDY_0	3	REQ_0	4	ACK_0
5	D0_0	6	D1_0	7	D2_0	8	D3_0
9	D4_0	10	D5_0	11	D6_0	12	D7_0
13		14		15	STRB_1	16	RDY_1
17	REQ_1	18	ACK_1	19	D0_1	20	D1_1
21	D2_1	22	D3_1	23	D4_1	24	D5_1
25	D6_1	26	D7_1	27		28	
29	STRB_3	30	RDY_3	31	REQ_3	32	ACK_3
33	D0_3	34	D1_3	35	D2_3	36	D3_3
37	D4_3	38	D5_3	39	D6_3	40	D7_3
41		42		43	STRB_4	44	RDY_4
45	REQ_4	46	ACK_4	47	D0_4	48	D1_4
49	D2_4	50	D3_4	51	D4_4	52	D5_4
53	D6_4	54	D7_4	55		56	
57		58		59		60	RESET

Compatible with the 148 and 148LT, an active low RESET signal is provided. When two 148FX boards are interconnected with a 60 way cable assembly, the RESET is propagated from one 148FX to the other.

4.2.16 Internal ComPorts

Each TIM site has 6 ComPorts.

Four of these are connected directly to the Spartan 3 FPGA. These are ComPorts 0, 1, 3 & 4.

ComPorts 2 & 5 are connected between TIM sites in a pipe configuration as follows;

TIM1 ComPort 2 connects to TIM2 ComPort 5

TIM2 ComPort 2 connects to TIM3 ComPort 5

TIM3 ComPort 2 connects to TIM4 ComPort 5

TIM4 ComPort 2 connects to TIM1 ComPort 5

4.2.17 Power input

Power is supplied from an external source. The voltage of the external source needs to be in the range +18V to 30V. This enters the board via an 8-pin connector (Receptacle, mini fit 8 Way, Molex)

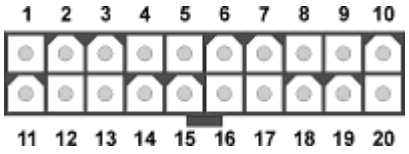
+18-30V	1
+18-30V	2
+18-30V	3
+18-30V	4
GND	5
GND	6
GND	7
GND	8

Table 1 : Power in pinout

The external source is input to a DC-DC converter module, which produces +/-12V to the TIM sites. It is also used as an input to two DC-DC converters that produce the +5V, +3.3V, +2.5V and 1.5V supply to the TIM sites, carrier FPGA and other devices.

Alternatively, the input power can be provided at +9 to 18V (using an alternative DCDC part), or from an ATX style power supply. Please consult Sundance regarding these options.

4.2.18 ATX Power Connector Pin-Out



Main 20 pin connector:

Name	Pin	Pin	Name
+3.3V	1	11	+3.3V
+3.3V	2	12	-12V
GND	3	13	GND
+5V	4	14	ON (input)
GND	5	15	GND
+5V	6	16	GND
GND	7	17	GND
-	8	18	-
-	9	19	+5V
+12V	10	20	+5V

Extension for BTX:

+12V			+5V
+3.3V			GND

4.2.19 Power output

Power can be supplied to external devices or modules. The 8-pin connector (Receptacle, mini fit 8 Way, Molex) providing different voltages has the following pinout:

	Pin number
-12V	1
+12V	2
+5V	3
+3.3V	4
GND	5
GND	6
GND	7
GND	8

Table 2 : Power out pinout

4.2.20 JTAG

A single JTAG chain connects all 4 TIM sites and the JTAG in & out connectors. This chain is used with the TI Code Composer Studio software suite. Although in essence it is a chain, the chain exists internally to a Xilinx CPLD. The CPLD drives and receives signals to the 4 TIM sites independently. This allows JTAG clock frequencies in excess of 30MHz to work reliably.

The JTAG-out (JTAG2) connector can be connected to the JTAG-in (JTAG1) connector of other SMT148FX, thus extending the chain (see cable SMT503).

All JTAG chaining and TIM bypass is performed within the CPLD.

4.2.21 Local Clock for ADCs etc.

The full functionality of the SMT399-F is also included. This comprises an external clock input, phase shifter, local OCXO, and 4-way power splitter.

4.2.22 Fan Power

Four two-pin connectors are provided to supply fans using power directly from the power input connector.

Note that if power is provided via an ATX type supply, then these fan connectors will be unpowered.

4.2.23 Reset Scheme

A power rail monitor observes the state of the 3.3V supply. This device will generate a reset to the SMT148FX (RESET148) during power-up or if the 3.3V supply drops below 3V. This signal is an open-collector output and is also driven to the inter-card ComPort connector, and thus to another SMT148FX.

The POR (power on reset) signal is driven to the RESETOUT pin on the external ComPort1 connector. The RESETIN pin on the above connector is buffered by an open-collector device which in turn can also drive the RESET148 signal. An additional 4 pin header is provided to allow other devices to share the open-collector RESET148 signal.

The TIM reset pins are connected to the FPGA and will be reset when RESET148 is active as well as when some firmware conditions trigger a reset to the different TIMs (see Firmware description for more details about TIM reset).

4.2.24 FPGA configuration

In the default configuration the FPGA is configured by the OXUF922 micro-controller that fetches the configuration from the flash device. However it is possible to download a new configuration to the FPGA using the Xilinx JTAG cable connected to a PC and to JP5 on the SMT148FX carrier. The pinout is as follows:

1	3.3V
2	GND
3	TMS
4	TCK
5	TDO
6	TDI

5 Verification, Review and Validation Procedures

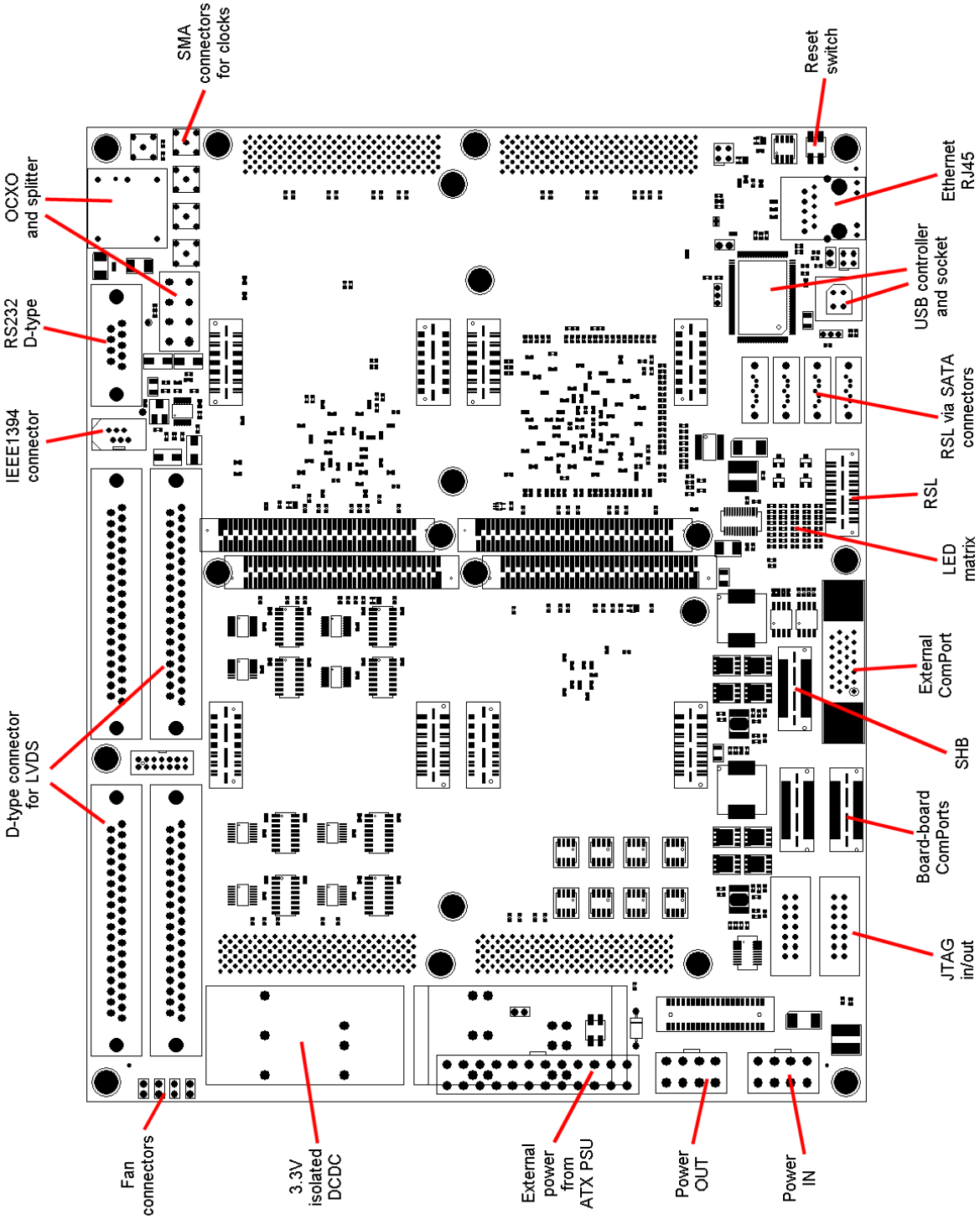
To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

6 Timing Diagrams

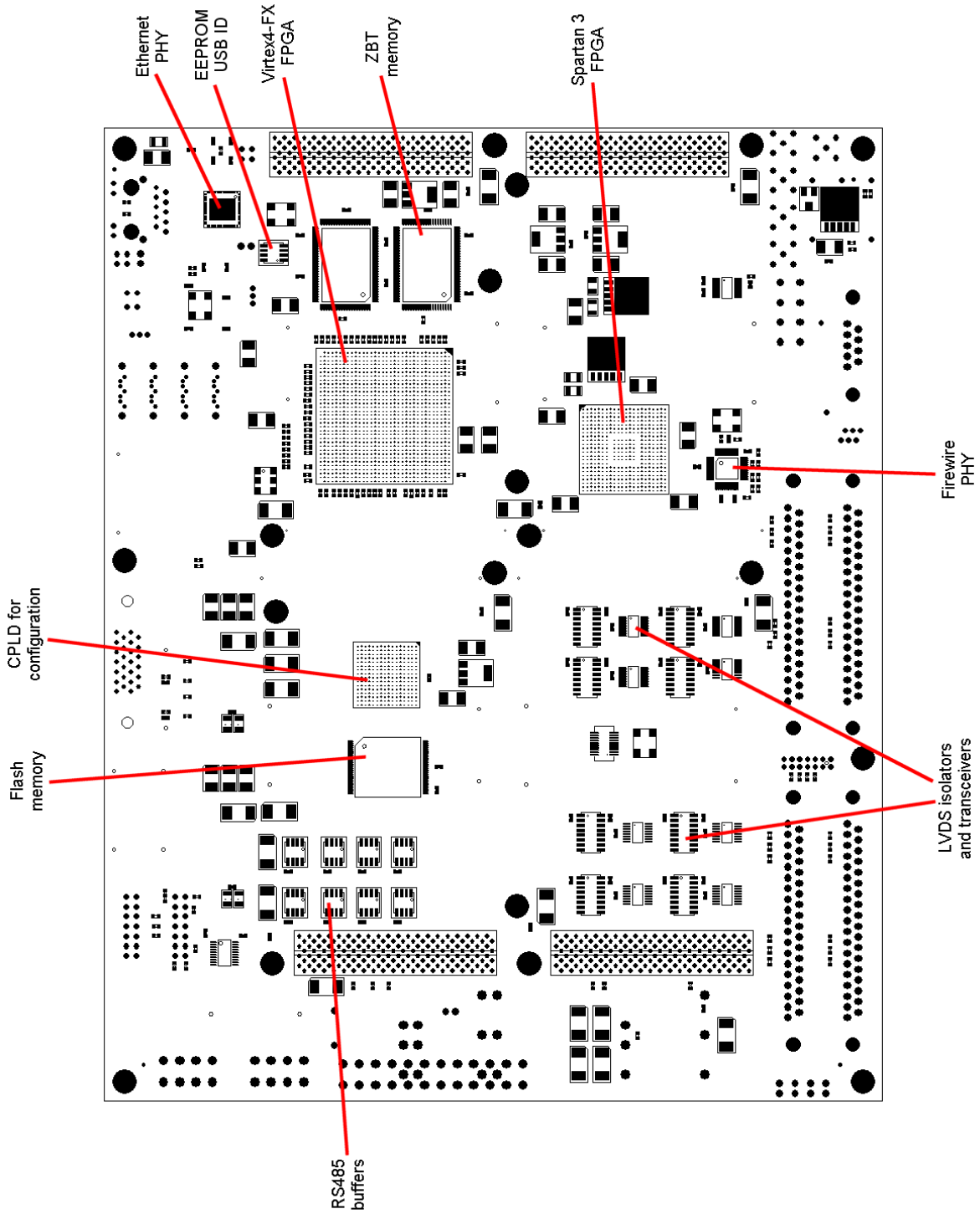
7 Circuit Description / Diagrams

8 Footprint

8.1 Top View



8.2 Bottom View



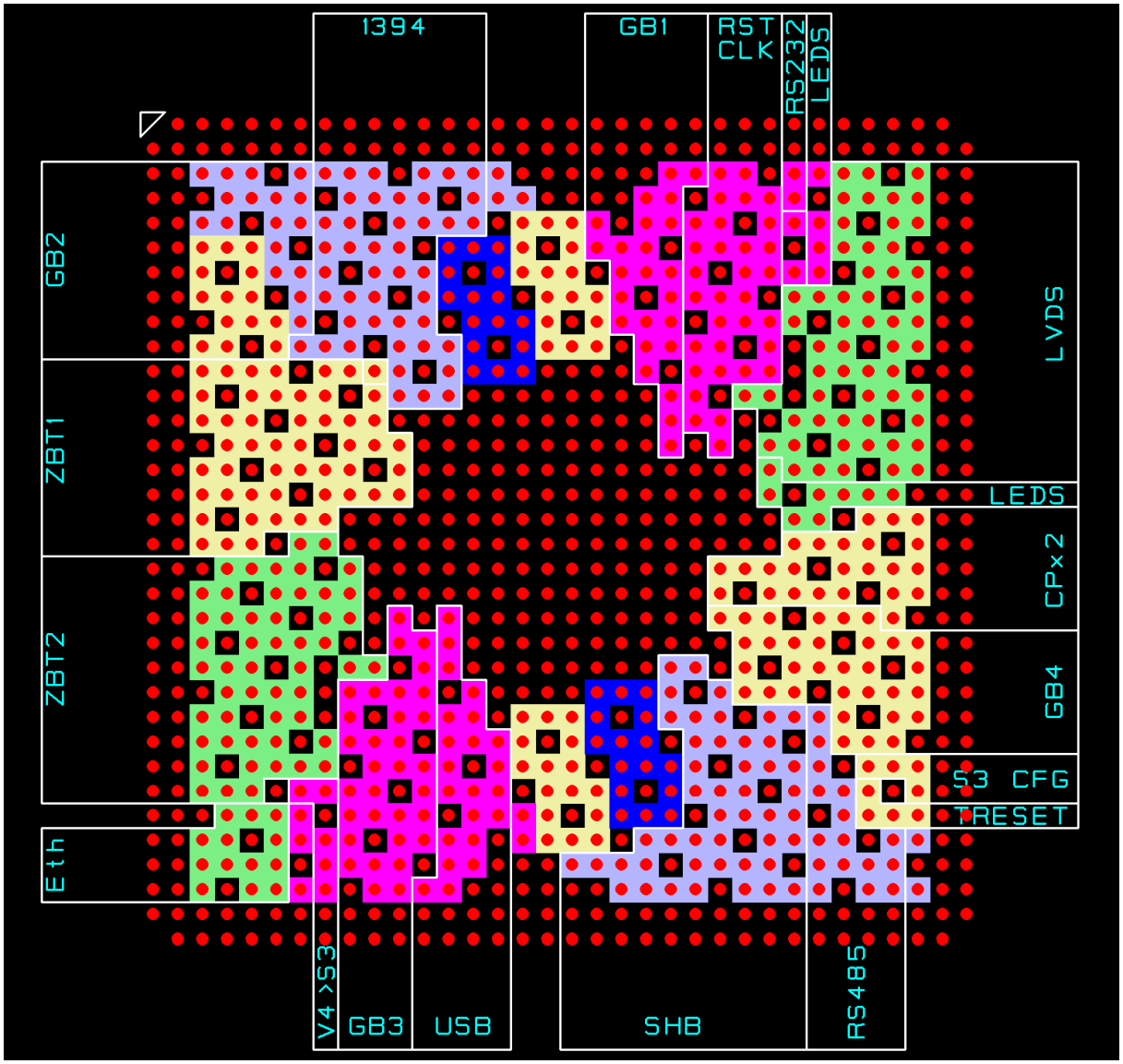
9 FPGA Pin Allocation

USB2 controller	CLK	1		22	SDB type interface
	Data	16			
	Control	3			
	User Def	2			
Firewire / OXUF922	All			29	IDE interface to OXUF922
	Address	12		23	From OXUF922
	Data	8			V4 Configuration data
	Control	3			
SHB/SDB	Data	16	2	48	2 x 16-bit data.
	Control	3			WEN, REQ, ACK.
	User	4			USER0-3
	Clock	1			
RS485	All			18	16 data and two control.
LVDS	All			56	8 groups of 7, normally routed to McBSPs via FPGA.
ComPorts	All	12	4	48	To Spartan3.
LEDs	All			12	8 x 4 matrix.
Ethernet PHY	All			12	4-bit data + 2 control for each direction.
				4	RST, COMA, MDC and MDIO.
Global Bus	Address	12	4	128	
	Data	16			
	Control	4			STRB, RW, PAGE, RDY
TIM misc	TCLK	2	4	48	
	Config	1			
	IIOF,NMI	4			
	IACK	1			
	Reset	1			Individual resets to TIM sites.
	Clock	3			CLKIN, H1 and H3.
RS232	All			2	Tx + Rx.
ZBT	Address	20	1	62	
	Data	32			
	Control+Clk	10			
Spartan3	FPGA config			3	PROG, CCLK, DIN
	Data Interface			4	CLK25, PXCLK, PXDATA, PXLOAD
	Reset			1	From V4
Other				2	BDRESET, CLK50

10 FPGA Bank Allocation

Interface	Bank	Comment
Global Bus A	5	12 Address, 16 Data, 4 Control (STRB, RDY, WR, PAGE)
Global Bus B	6+10	12 Address, 16 Data, 4 Control (STRB, RDY, WR, PAGE)
Global Bus C	8	12 Address, 16 Data, 4 Control (STRB, RDY, WR, PAGE)
Global Bus D	11	12 Address, 16 Data, 4 Control (STRB, RDY, WR, PAGE)
ZBT Bank 1	10	Clock uses GCK on bank
ZBT Bank 2	12	Clock uses GCK on bank
Ethernet	12	
SHB	7	
RS485	7+8	Direction control is on bank 8.
ComPorts	11+5	2 ports per bank used.
LVDS	9	
USB	8	Appears as a 16 bit SDB.
LEDs	5+9	
Misc, TIM	1+3+4	
RS232	5	Tx, Rx.
RST, Clock	5	
IEEE1394	6	
TIM reset	11	
V4 to S3 interface	8	CLK, DATA, LOAD, RESET

This is shown graphically here,



11 Support Packages

12 Physical Properties

The following table indicates the power capabilities of the on-board supplies;

Dimensions	
Weight	

Option		A	B	C
Supply Current	+12V	1.67A	0.83A	*
	+5V	10A	10A	*
	+3.3V	10A	10A	*
	-5V	0A	0A	*
	-12V	0A	0.83A	*

*Option C is with the use of an external ATX power supply. Refer to the relevant power supply specification in this case.

MTBF	

13 Thermal Management

Although provision is made to attach DC fans to the SMT148FX (powered directly from the input voltage), correct enclosure air flow should be ensured.

Sundance are able to provide a heat-pipe type thermal management solution for two TIM sites (sites 2 and 3). This involves increased height TIM and RSL connectors for these sites, the fixing of the heat-pipe system direct to the TIMs' components, and the addition of an off-board heatsink and fan. Please consult Sundance for pricing and availability for this option.

Several components in both the onboard 3.3V and 5.0V supplies are rated at 125°C maximum. Without adequate cooling, the inductors in this circuit can reach in excess of 170°C when running at full rated load.

14 Safety

This module presents no hazard to the user when in normal use.

15 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

16 Ordering Information

Two variations of this product are available.

SMT148-FX	Standard product.
SMT148-FX-Fxxx	With additional local ADC oscillator. xxx refers to the oscillator frequency.