HARDWARE SPECIFICATION

FOR

SMT150Q

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APPROVAL PAGE

Name	Signature	Date

AUTHOR/S

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DOCUMENT HISTORY

Date	Initials	Revision	Description of change
22/11/04	GKP	1.0	First draft. (based on the 145Q)
23/11/04	GKP	1.1	Board layout updated.
24/6/05	GKP	1.2	Changed to Virtex4 and included a ComPort switch
2/8/05	GKP	1.3	Updated board layout and com port drawing.
3/4/06	GKP	2.0	Major revision
22/6/06	GKP	2.1	Removed references to SHB and SRAM.
17/8/06	GKP	2.2	Added FPGA configuration section.

TABLE OF CONTENTS

1. SCOPE

This document specifies the requirements for The SMT150Q PCI express TIM carrier board.

1.1. INTRODUCTION

The SMT150Q is a PCIe 4-Site TIM carrier

- PCI Express interface (4 lanes)
- Sundance RSL (Rocket IO) interfaces

1.2. PURPOSE

The SMT150Q must:

- Provide high-speed RSL interfaces to Sundance TIM modules
- Provide ComPort interfaces for low speed communications.

1.3. APPLICABILITY

Interface to other FPGA, DSP, ADC/DAC modules and in stand alone systems.

2. APPLICABLE DOCUMENTS AND REFERENCES

2.1. APPLICABLE DOCUMENTS

2.1.1. External Documents

TI TIM specification & user's guide.

Samtec QSH Catalogue page

Virtex 4 Datasheet

PCI Express Overview

2.1.2. Internal documents

None.

2.1.3. Project Documents

Smt150Q QCF14.mpp Project Planning Document.

2.2. REFERENCES

2.2.1. External documents

N.A

2.2.2. Internal documents

N.A

2.2.3. Project documents

N.A

2.3. PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

3. ACRONYMS, ABBREVIATIONS AND DEFINITIONS

3.1. ACRONYMS AND ABBREVIATIONS

TIM	Texas Instruments Module
SLB	Sundance LVDS Bus
RSL	Rocket Serial Link (Xilinx MGT)
MGT	Multi-Gigabit Transceiver

3.2. DEFINITIONS

TIM carrier	A circuit board which contains TIM site(s). Typically these also contain an interface to a host (PCI, VME), or various interfaces for standalone operation.

4. REQUIREMENTS

4.1. PRIME ITEM DEFINITION

This carrier board conforms to the TIM standard (**T**exas **I**nstrument **M**odule, See TI TIM specification & user's guide).

The carrier board provides power, ground, RSL, Comport, and a JTAG chain between all the modules fitted and a pathway to the host, for a non stand-alone system.

The SMT150Q provides the additional 3.3V power supply to the two diagonally opposite TIM mounting holes.

4.2. PRIME ITEM DIAGRAMS

4.2.1. PCI-e Interface and RSL Connections

The Virtex4-FX series devices include high speed serial IO (Rocket IO).

16 differential pairs are available on the XC4VFX60 FPGA used on the SMT150Q.

The Sundance implementation of Xilinx's Rocket IO is called RSL.

Note that all RSL connections are full-duplex and can therefore send and receive data at 250Mbytes/s simultaneously (when used at 2.5Gb/s data rate).

Notes on RSLs:

TIMs with RSL connectivity can have up to 4 RSL connectors; two mounted on the top of the module, and two underneath.

When viewed from the TOP with the primary TIM connector on the left, the RSL connector at the bottom and underneath the module MUST be present on all TIM designs. This connector will have ALL 4 RSLs connected to logic (FPGA or DSP) on the module.

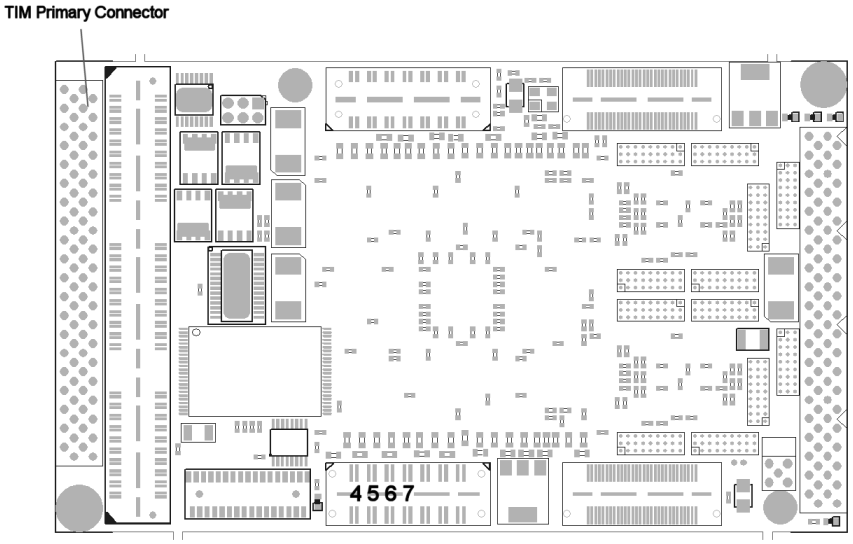
Under normal circumstances, only 4 of the 7 differential pairs available on the RSL connector will be used for RSL signals. This allows 16 RSL connections per TIM module.

Unused differential pairs of the RSL connector may be used for other interfaces such as Ethernet. They may also be used for extra RSL connections, but only after the other available connections have been used.

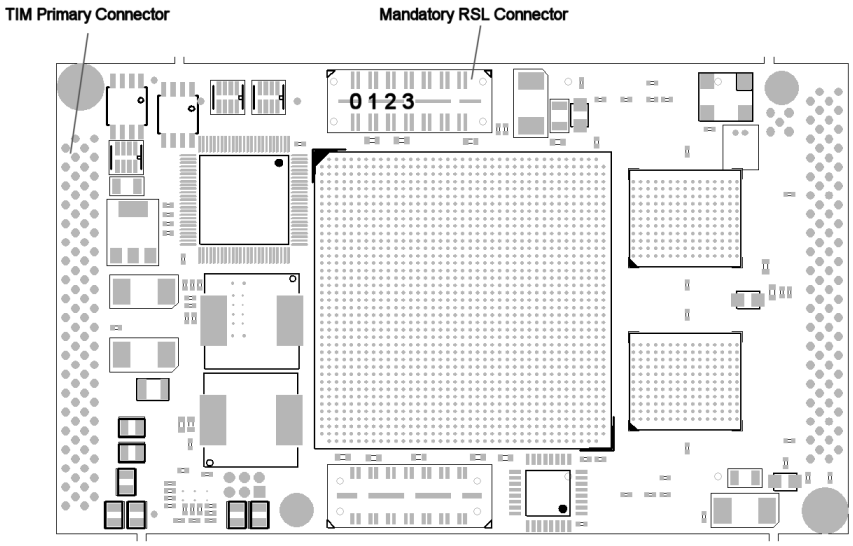
After the mandatory TIM RSL connector has been allocated connections to the RSL interface device, the connector mounted above this on the top side must then be connected to on-board devices. Only after all 8 RSL signals have been allocated on these two RSL connectors, may signals be allocated to the two remaining RSL connectors. Note, however, that this connector is optional.

The following pictures show priority for allocating RSL signals to connectors (0 to 7, with 0 being of highest priority).

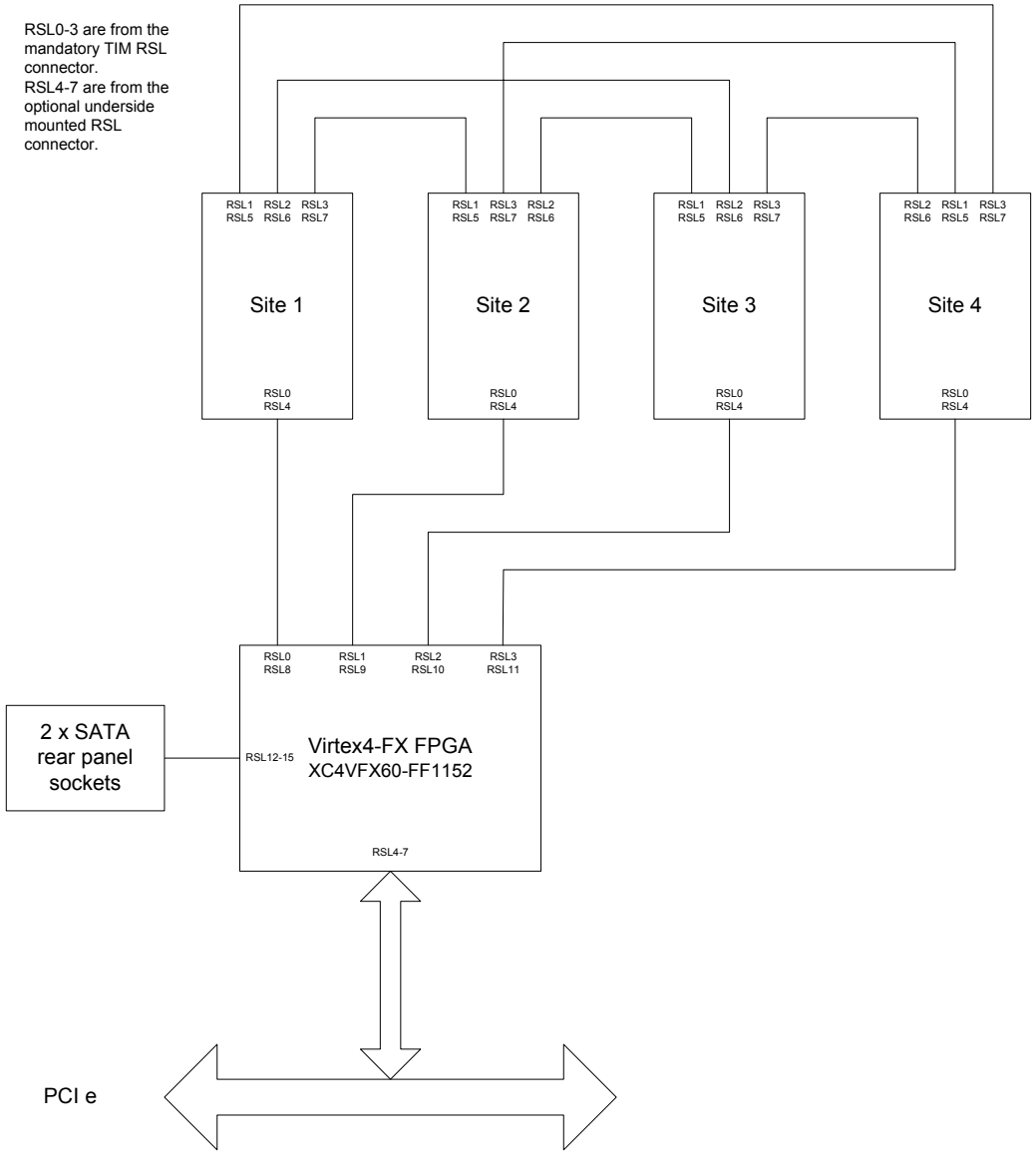
All connectors not labelled may be allocated at designer's discretion.



Top View



Bottom View

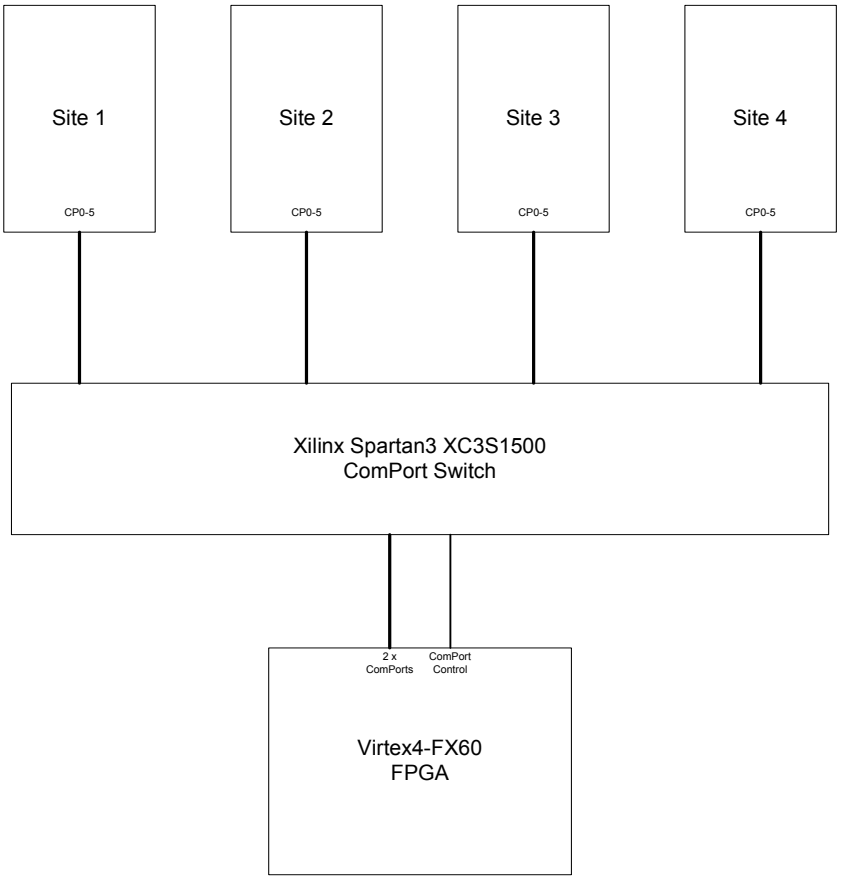


The above diagram shows the RSL connectivity between sites, PCI-express and off-board.

4.2.2. ComPort Connections

ComPort connections are provided for backwards compatibility with earlier generations of TIMs and carriers, but fast data transfer should be accomplished using RSL (where available).

All TIMs' ComPorts (6 each) are connected to a ComPort switch implemented using a Xilinx Spartan3 device (XC3S1500-4FGG456). Two additional ComPorts from the Virtex4-FX device are also connected to this switch.



4.3. PRIME ITEM CHARACTERISTICS

4.3.1. PCIe Interface

The PCIe interface is provided by a Xilinx PCIe core within the FPGA. This is, internally, a 64-bit PCI device

4.3.2. PCI memory map

In target mode, a host device accesses the SMT150Q across the PCI bus, which gives access to the target mode registers. The operating system or BIOS will normally allocate a base address for the target mode registers of each SMT150Q. Access to each register within the SMT150Q is then made at offsets from this base address as shown in the tables below.

4.3.3. JTAG Connector

Debugging via JTAG (Code Composer) is performed by connecting an external debugger to the 14-pin JTAG header.

Cascading of multiple JTAG systems is possible due to the provision of a JTAG-OUT connector.

The TIM JTAG signals are also connected to the Virtex4. This could allow debugging using Code Composer Studio without the need for an external XDS510/560 type debugger, but this will depend on the availability of the TI TBC (test bus controller) internal workings to be made available.

4.3.4. Global Bus

TIM sites1 1 and 3 have the optional global bus connector. These global buses are completely isolated and are connected to the Virtex4 FPGA.

4.3.5. FPGA Configuration

The FPGA can be configured in 2 different ways.

- Using the on-board Flash PROM.
- Using the on-board JTAG header and Xilinx JTAG programming tools.
    - The JTAG header is compatible with the Parallel-IV signals.

The flash PROM is a 32Mx8 device and has its address and control signals connected to a CPLD. The data bus is connected to the Virtex FPGA and the CPLD.

Upon power up (or board reset), the CPLD will check the start of the flash to see if it has valid Virtex FPGA configuration data. If such data exists, then the CPLD will incrementally access the flash (using an internal address counter) and send this 8-bit data to the Virtex FPGA, thus configuring the FPGA. When the Virtex is configured, the flash is further read (via the CPLD) by the Virtex FPGA in order to extract data to program the Spartan FPGA.

If no configuration data is present in the flash, then the CPLD will enter a flash programming mode. Here, a 4-bit command bus (and 50MHz clock) is used between the Virtex FPGA and the CPLD to initiate the programming of the flash. It is envisaged that when the board is first powered up (with an empty flash), then the Virtex FPGA will be configured using the Xilinx JTAG programming header. This will then allow system (PC) access to the afore mentioned command bus.

The following table shows the currently specified commands;

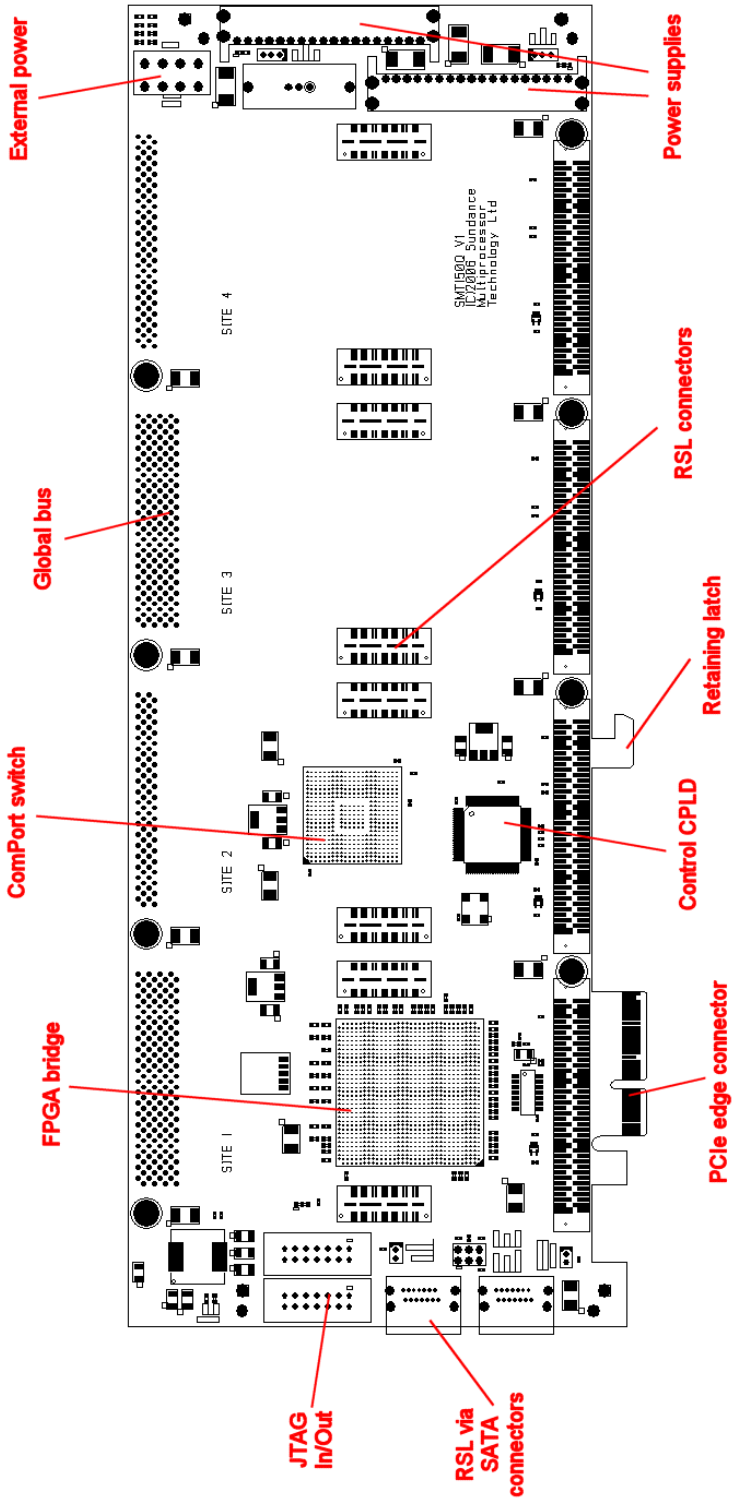
4-Bit command	Function	Description
0000	NOP	
0001	WRITE	Informs the CPLD to assert flash CS and WE
0101	WRITE+INC	As WRITE but also increments the address counter
0010	READ	Informs the CPLD to assert flash CS and OE
0110	READ+INC	As READ but also increments the address counter
1000	LOAD A0	Sets the flash address counter bits 7-0
1001	LOAD A1	Sets the flash address counter bits 15-8
1010	LOAD A2	Sets the flash address counter bits 23-16
1011	LOAD A3	Sets the flash address counter bit 24
1100	WRITE AAA	Bypasses the address counter and uses address AAA
1101	WRITE 555	Bypasses the address counter and uses address 555
1111	NOP	

The CPLD is further connected to a 2-pin jumper which is used to select what configuration data to use to program the FPGAs. Essentially, this will alter the most significant address bit from the address counter during configuration. In this way, it will be possible to have a default configuration (jumper inserted) which can be reverted to if the secondary configuration (jumper not inserted) is corrupted.

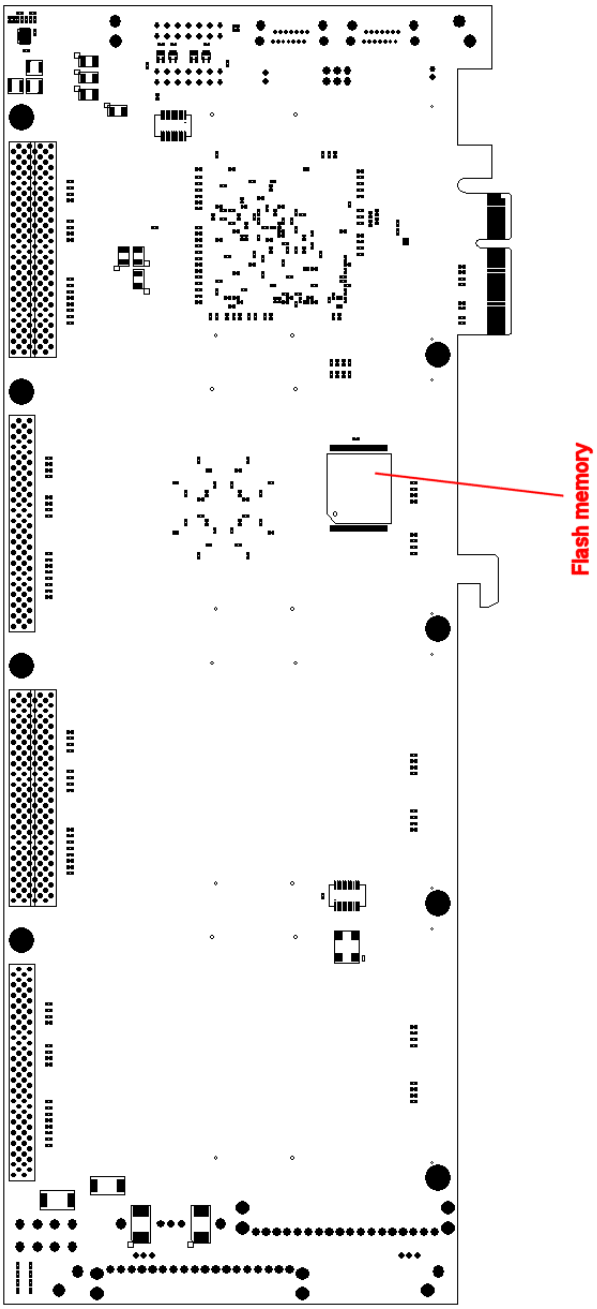
The commands are sent to the CPLD by the FPGA asserting the correct code for one clock cycle only. Commands may not be sent to the CPLD at a rate greater than the speed of the flash. This would indicate that commands cannot be sent at a rate greater than 1 every 8 clock period.

5. FOOTPRINT

5.1. TOP VIEW



5.2. BOTTOM VIEW



6. QUALIFICATION REQUIREMENTS

6.1. QUALIFICATION TESTS

6.1.1. Meet Sundance standard specifications

- Meet the TIM standard specifications
- Meet the RSL specifications.

6.1.2. Speed qualification tests

- Provide PCIe maximum throughput on 4 lanes.

6.1.3. Integration qualification tests

- Must work on ALL Sundance platforms.
- Must be able to work stand-alone.

7. PCB LAYOUT DETAILS

7.1. BOARD LAYOUT GUIDELINES:TBD

- Decoupling guidelines.

8. PINOUT AND PACKAGE REQUIREMENTS

8.1. FPGA PINOUT: TBD

8.2. 2 RSL CONNECTORS

See SUNDANCE RSL specification

8.3. 4 LEDS:TBD

9. SAFETY

This module presents no hazard to the user.

10. EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

11. REVIEW PROCEDURES

Reviews will be carried out as indicated in design quality document QCF14 and in accordance with Sundance's ISO9000 procedures.

12. ORDERING INFORMATION
