

Sundance Multiprocessor Technology Limited
SMT300- NI Front Panel
Connector

Form : QCF51
Date : 11 February 2009

Unit / Module Description:	NI RDIO Connector for SMT300
Unit / Module Number:	SMT300- NI
Document Issue Number:	1.1
Issue Date:	21 st April 2009
Original Author:	G K Parker

SMT300- NI Front Panel Connector

Sundance Multiprocessor Technology Ltd, Chiltern House,
Waterside, Chesham, Bucks. HP5 1PS.

This document is the property of Sundance and may not be copied
nor communicated to a third party without prior written
permission.

© Sundance Multiprocessor Technology Limited 2009



Certificate Number FM 55022

Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	23/03/09	GKP
1.1	Added BGA ref for 351T FPGA.	21/4/09	GKP

Table of Contents

1	Introduction.....	4
2	Related Documents.....	4
3	Verification, Review & Validation Procedures	5
4	Circuit Description / Diagrams	6
5	Footprint.....	6
6	Pinout	7
7	Safety.....	8
8	EMC	8



1 Introduction

This product incorporates a double-width replacement front panel for the SMT300. The extra space to the right of the standard SMT300 connectors contains a 68-pin Tyco d-style connector that can receive a National Instruments SHC68-68 RDIO cable.

Fixed to the Tyco connector is a small PCB which holds a Sundance SHB connector.

This product therefore allows the connection of NI cards to Sundance systems.

2 Related Documents

Tyco 68-way connector:

<http://catalog.tycoelectronics.com/TE/bin/TE.Connect?C=1&M=BYPN&TCPN=5174225-1&RQPN=5174225-1>

National Instruments NI PXI-7833R:

<http://www.ni.com/pdf/products/us/2005-5528-301-101-D.pdf>

<http://www.ni.com/pdf/manuals/372492b.pdf>

Sundance SHB Cable:

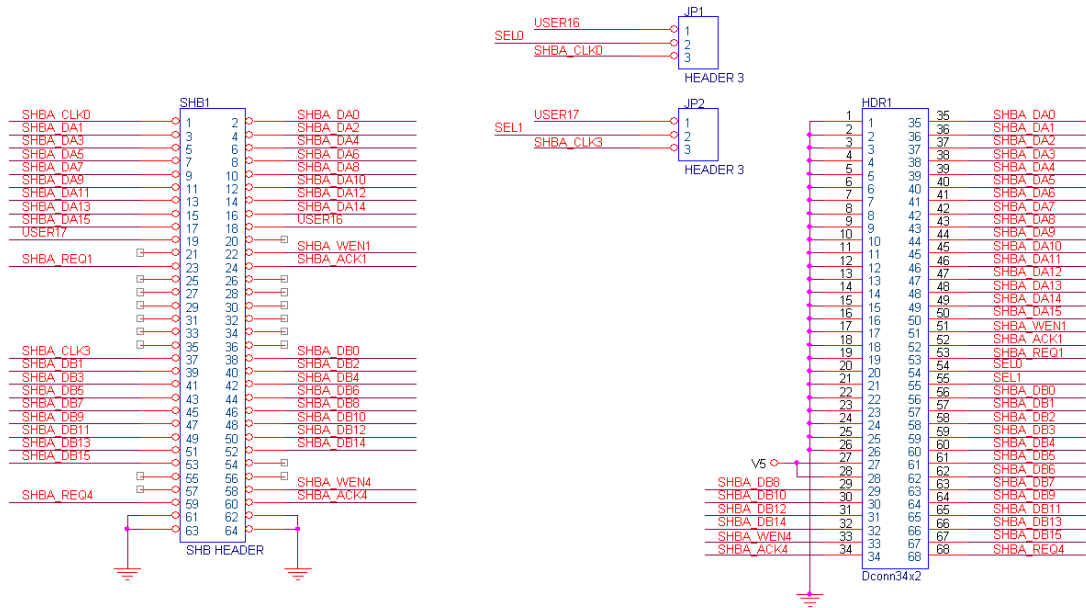
<http://www.sundance.com/web/files/productpage.asp?STRFilter=SMT511-320>

3 Verification, Review & Validation Procedures

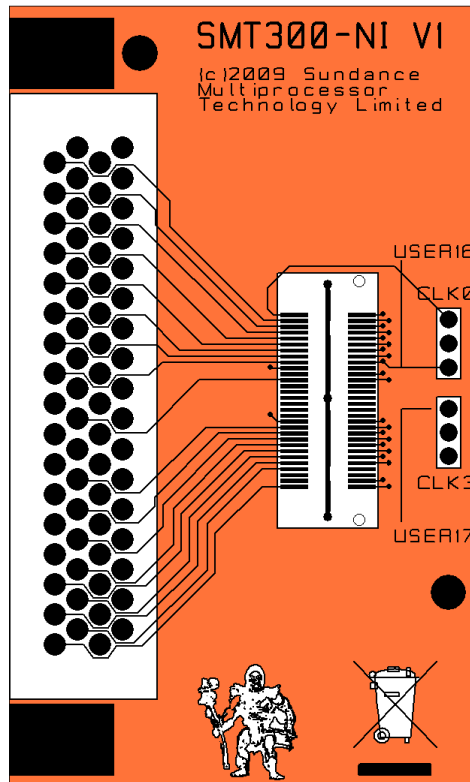
To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

A continuity test will be carried out using a suitable TIM, the SMT300- NI (this card), and an NI SHC68- 68 cable.

4 Circuit Description / Diagrams



5 Footprint



6 Pinout

Signal	SHB	BGA	RDIO
CLK0	1	G8	54
DA1	3	G6	36
DA3	5	G7	38
DA5	7	H7	40
DA7	9	J7	42
DA9	11	K7	44
DA11	13	K6	46
DA13	15	L4	48
DA15	17	L5	50
USER17	19	D11	55
	21		
REQ1	23	J5	53
	25		
	27		
	29		
	31		
	33		
	35		
CLK3	37	T9	55
DB1	39	N8	57
DB3	41	N7	59
DB5	43	P7	61
DB7	45	P6	63
DB9	47	R9	64
DB11	49	P9	65
DB13	51	R6	66
DB15	53	T6	67
	55		
	57		
REQ4	59	U10	68
	61		
	63		
	65		
	67		

RDIO	BGA	SHB	Signal
35	E6	2	DA0
37	E7	4	DA2
39	F5	6	DA4
41	F6	8	DA6
43	H5	10	DA8
45	G5	12	DA10
47	M7	14	DA12
49	L6	16	DA14
54	D12	18	USER16
		20	
51	T10	22	WEN1
52	T11	24	ACK1
		26	
		28	
		30	
		32	
		34	
		36	
56	M6	38	DB0
58	M5	40	DB2
60	N5	42	DB4
62	P5	44	DB6
29	R11	46	DB8
30	P10	48	DB10
31	R7	50	DB12
32	R8	52	DB14
		54	
		56	
33	T8	58	WEN4
34	U7	60	ACK4
		62	
		64	
		66	
		68	

Notes:

RDIO pins 1- 26 are connected to GND.

RDIO pin 54 (SEL0) can connect to either SHB pin 18 (USER16) or SHB pin 1 (CLK0). This is determined by a jumper.

RDIO pin 55 (SEL1) can connect to either SHB pin 17 (USER17) or SHB pin 37 (CLK3). This is determined by a jumper.

BGA column refers to the pin number of the FPGA on an SMT351T.

7 Safety

This module presents no hazard to the user when in normal use.

8 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.