SUNDANCE

SMT300

User Manual V1.9

Certificate Number FM 55022

Revision History

Date	Comments	Engineer	Version
30/11/01	Initial SMT300 Draft	AJP	0.5
16/01/02	Re-editing	SP	1.0
20/02/02		SP	1.1
06/03/02	ComPort Mirrors	SP	1.2
29/05/02	Installation Procedure	SP	1.3
16/07/03	PLL registers	SP	1.4
21/07/03	Reformat	SP	1.5
23/04/04	PLL register changes	SP	1.6
21/05/04	Power connector part number correction	TJW	1.7
03/10/06	Corrected Typo	SP	1.8
19/03/10	Corrected Reset IN/Out error	AJP	1.9

Table of Contents

1 Introduction

The SMT300 is a 3U size CompactPCI board that can carry an industry-standard, TIM format processor modules. Sundance provides a large range of these TIMs.

Features:

- Processor interconnection using comports. Direct comport and SDB access to the host is also provided;
- 1MB of shared SRAM between the host and TIM site 1 (the Master TIM site);
- On-board JTAG controller to allow debugging using Code Composer. The board can also be used as a JTAG master for debugging remote systems;
- On-board CompactPCI Bridge chip to provide DMA, mailbox events, and interrupts;
- CompactPCI access between the host and the Master TIM site at burst speeds in the range 60–100MB/s;

2 Installing the SMT300

2.1 Software installation

You should install the SMT6300 software package before plugging the hardware into your PC. The SMT6300 sets up device drivers and test utilities for the Sundance range of carrier boards.

2.2 Hardware installation

1. Plug your TIM into the SMT300 TIM Site. Note that many TIMs require a 3.3v supply. This is taken from the mounting pillars, so it is important you bolt down the modules securely;
2. Power-down the PC;
3. Insert the SMT300 into a spare CompactPCI slot;
4. Power-up your PC. If you are using[1] Windows 2000 or Windows XP, the hardware wizard should appear (Figure 1);
5. Click "Next >". The wizard should indicate that the SMT300 has been installed successfully (Figure 2);
6. Click "Finish";

2.3 Testing the hardware

The SMT6300 comes with a utility called SmtBoardInfo.exe. You should start this and run its confidence test, found under "Tools".

[1] Windows NT users: No hardware wizard will appear, but you should ensure there are no resource conflicts. See Checking for hardware resource conflicts

Figure 1 - Hardware wizard

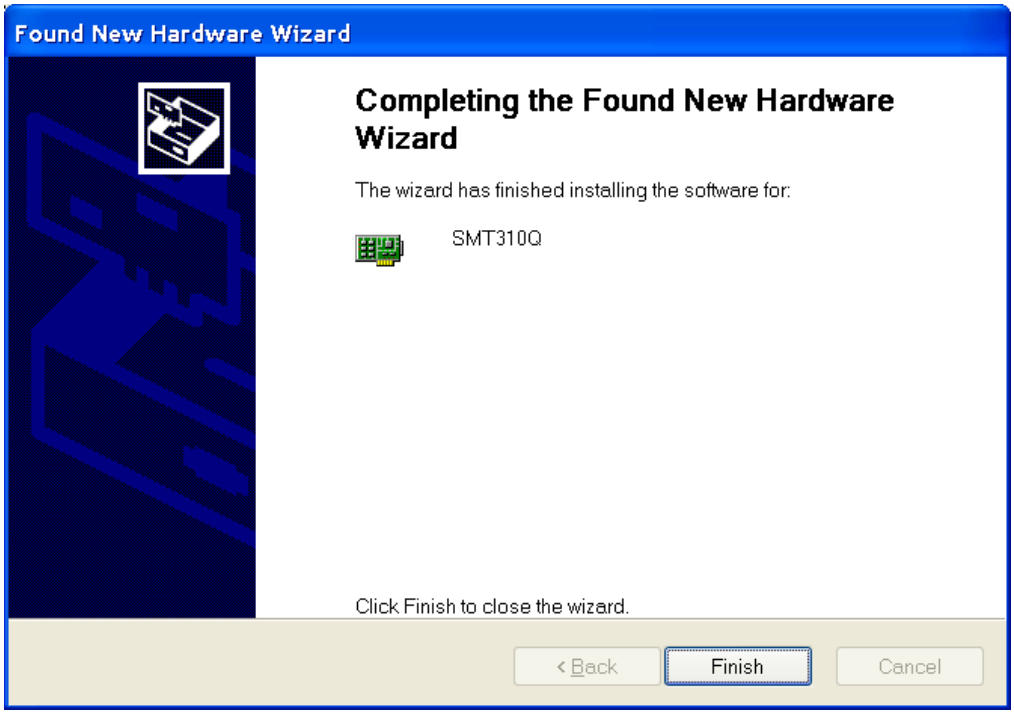
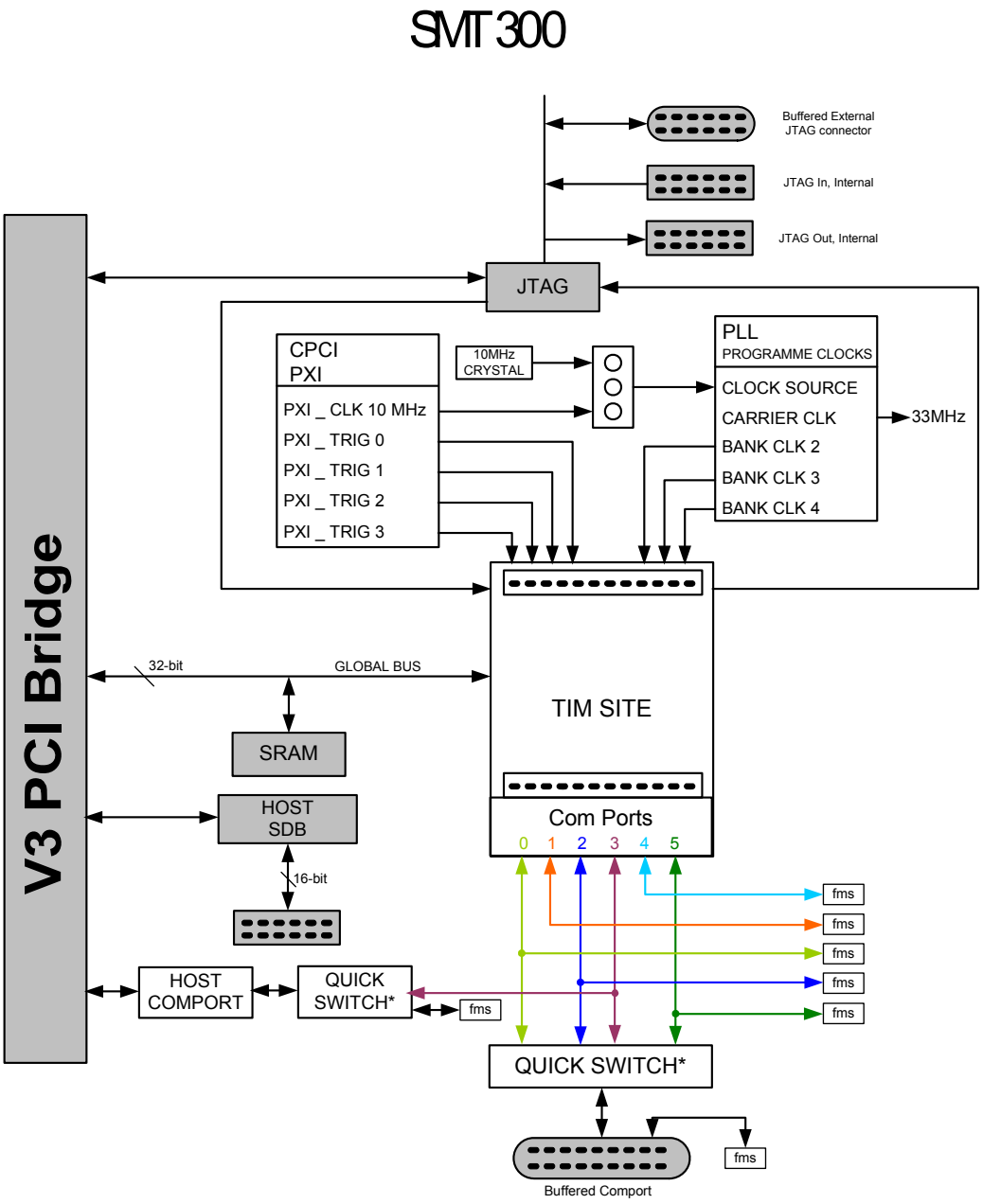


Figure 2 - Hardware wizard detected the Sundance hardware

3 Hardware Overview



*Quick Switches set up using the comport configuration register (bar 1, offset 20_{16})

Figure 3 - SMT300 Block Diagram

3.1 Local Bus

The SMT300 uses a *Local Bus*[2] to control transfers amongst the various resources. The bus has a 33MHz clock that is available on the CLKIN pin of the Master TIM site. The TIM in this site should be set to select the local bus clock in preference to its own oscillator to allow it to synchronise accesses across the CompactPCI Bridge. Details of this can usually be found in the TIM documentation under "Global Bus Control Register".

3.2 V363EPC CompactPCI Bridge Chip

The CompactPCI Bridge connects the host CompactPCI bus to various devices on the local bus:

- **Quick Logic EPC363 Bridge chip**. This has a 32-bit, 33MHz CompactPCI interface that supports I^2C control, mailbox register access, and direct memory reads and writes;
- **Input and output FIFO.** This is capable of transferring 256 32-bit words of data to and from the DSP at 33MHz, bursting at a maximum local bus transfer rate of 132MB/s;
- **Address apertures.** These provide access to the V363EPC Bridge chip configuration registers or bridging functions. The apertures respond to addresses on both the CompactPCI and Local buses. The following apertures are available on the SMT300:
    - Four data transfer apertures to transfer data across the bridge. Two apertures are for CompactPCI to local transfers (BAR1 and BAR2) and two are for local to CompactPCI transfers (Local-to-CompactPCI Aperture 0 and Local-to-CompactPCI Aperture 1).
    - Two apertures to access the bridge chip's internal registers: one aperture for Local Bus (CompactPCI Bridge Register) accesses and one for CompactPCI bus (BAR0) accesses.

3.3 JTAG controller

The JTAG controller is based on the TI 8990 device; Code Composer Studio drivers are available from Sundance, Part Number SMT6012. The presence of a TIM in a module site causes its SENSE pin to switch the module into the JTAG chain.

3.4 Shared SRAM

The Master TIM can access the SRAM over the Local Bus at transfer rates up to 100MB/s. The number of wait-states required by the Master TIM varies

[2] The Local Bus is not shown explicitly in the SMT300 block diagram.

depending on the speed of the module. Maximum access rates use a 20ns strobe cycle.

3.5 Control EPLD

The EPLD acts as an on-board arbitration unit that controls which device has access to the Local Bus resources.

3.6 Onboard resources

3.6.1 SDB

The on-board SDB connector is accessible via the Host CompactPCI interface. It can be configured with a jumper (J9) to be either an input port or an output port. It is not intended as a high-speed link as it only has a single 16-bit data register. You can join this connector with an SDB cable to one of the SDB connectors on any TIM plugged into the board.

3.6.2 Host ComPort link

The normal means of communication between the host PC and the Master TIM on an SMT300 is through the host ComPort. A programmable switch selects how this ComPort is connected.

4 ComPorts

The SMT300 gives access to all six TIM site ComPorts. One of four of these ComPorts can be connected through a high drive buffer to a connector on the rear panel of the card. This connection and switching is achieved using *Quick switches* alleviating the need for patch cables.

Five of the TIM site ComPorts are connected straight to 14-way surface-mount FMS connectors for connection to other ComPort compatible devices within the same chassis.

There is a connection from the CompactPCI interface to ComPort 3 for booting the TIM. This connection can be severed with a quick switch (clear *CENc*) allowing ComPort 3 to be used for other purposes. This also allows the CompactPCI interface ComPort to be used independently of the TIM as it is also wired to a 14-way surface-mount FMS connector.

The configuration of the ComPorts on the SMT300 can be set using the ComPort configuration register (I/O Offset 20_{16}).

Default = $2C_{16}$ (Assuming no FMS cables connected)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	CENc	CENb	SELC	SELB	SEL1	SEL0

Table 1 : ComPort configuration register

The table below illustrates the different setting of the register.

CENc	CENb	SEL1	SEL0	Function
1	X	X	X	Connects DSP ComPort 3 to CompactPCI Host[1]
0	X	X	X	Disconnects DSP ComPort 3 to CompactPCI Host
X	0	X	X	Disables all DSP connections to Buffered ComPort
X	1	0	0	Connect DSP ComPort 0 to Buffered ComPort[2]
X	1	0	1	Connect DSP ComPort 2 to Buffered ComPort[2]
X	1	1	0	Connect DSP ComPort 3 to Buffered ComPort[2]
X	1	1	1	Connect DSP ComPort 5 to Buffered ComPort[2]

Table 2 : ComPort selection

[1] **If SELC is read as 0 then CENc is overridden as DSP ComPort 3 is now being driven by the external FMS connector J2.**

[2]**If SELB is read as 0 then CENb is overridden as buffered ComPort is now connected to external FMS connector J1.**

BUF_COM_DIR : Selects the direction of the buffered ComPort = SEL1

4.1 Buffered External ComPort

The buffer consists of an FCT245AT type device with 64mA pull-down ability. All signals are pulled up to +3.3 volts with 330-ohm resistors and the active devices are mounted as closely as possible to the connector they serve. The back panel connector is a 26 pin 3M type (3M part number 10226-5212JL).

As well as ground signals and the 12 C4x ComPort signals, there are 6 additional signals. These signals are NOT essential for communications:

Name	Description
I/O_OUT	Output high when port is outputting, output low when port is receiving.
I/O_IN	Input which prevents bus contention if connected to I/O_OUT
/RST_OUT	Active low open collector copy of the board reset drive.
/RST_IN	Active low board reset input, pulled up to 3.3V by 330 ohms.
VCC	1 AMP +5 Volt supply, with reset-able 1 Amp fuse, to power a remote buffer, if required.
SHIELD	Overall cable shield, connected to plug shells and chassis.

Table 3: Buffered ComPort Additional Signals

You can synchronise resetting a number of boards by chaining them together with /RST_OUT of one driving /RST_IN of the next.

The SMT502-Buffer is the recommended cable assembly for the buffered ComPort and can be purchased separately.

4.2 ComPort to CompactPCI Interface

The ComPort interface is memory-mapped to the CompactPCI Bridge as illustrated in Table 9. The ComPort uses the control and data registers to detect the state of the input and output FIFOs. The following section describes the bit definitions for these registers.

4.2.1 ComPort Registers (BAR1, Offset 10_{16})

The host can be connected to TIM site 1 using ComPort 3 (T1C3). This port is bi-directional and will automatically switch direction to meet a request from either the host or the DSP. Both input and output registers are 32 bits wide. Data can only be written to COMPORT_OUT when STATUS [OBF] is 0. When

a word is received from the DSP, it is stored in COMPORT_IN and STATUS [IBF] is set to 1. Reading COMPORT_IN will clear STATUS [IBF] and allow another word to be received from the DSP.

4.2.2 Control Register (BAR1, Offset 14_{16}, WRITE-ONLY)

The CONTROL register contains various control flags:

7-4	3	2	1	0
	IIOF2	IIFO1	IIOF0	RESET

RESET	Write a 1 to this bit to assert the reset signal to all the TIM modules on the SMT300.
IIOF0 IIOF1 IIOF2	These bits connect to the corresponding pins on the TIM in module site 1. Writing 0 causes the corresponding IIOF line to go low.

Table 4: Control Register

Note. On CompactPCI system reset, RESET is asserted to all TIM sites.

4.2.3 Status Register (BAR1, Offset 14_{16}, Read-Only)

31-22	21	20	19	18	17	16	15-12	11	10	9	8
	CONFIG_L	TBC RDY	0	MASTER	IBF	OBF		IM2	IM1	IM0	INTD

7	6	5	4	3	2	1	0
C40 INT	TBC INT	IBF INT	OBE INT	C40 IE	TBC IE	IBF IE	OBE IE

OBE IE	Set if ComPort output buffer empty interrupts enabled.
IBF IE	Set if ComPort input buffer full interrupts enabled
TBC IE	Set if JTAG interrupts enabled
C40 IE	Set if interrupt from TIM DSP enabled
OBE INT	Set if the ComPort output buffer becomes empty. Cleared by writing a 1 to the corresponding bit in the interrupt control register.
IBF INT	Set if the ComPort input buffer receives a word. Cleared by writing a 1to the corresponding bit in the interrupt control register
TBC INT	Set when the TBC asserts its interrupt. Cleared by removing the source of the interrupt in the TBC.
C40 INT	Set when the TIM DSP sets its host interrupt bit. Cleared by writing a 1 to the corresponding bit in the interrupt control register.
INTD	The logical OR of bits 7—4 in this register gated with each one's enable bit.
OBF	Set when a word has been written to the ComPort output register. Cleared when the word has been transmitted to the DSP.
IM0	Interrupt mask 0. Returns Interrupt Control Register Bit 8.
IM1	Interrupt mask 1. Returns Interrupt Control Register Bit 9.
IM2	Interrupt mask 2. Returns Interrupt Control Register Bit 10.
IBF	Set when a word has been received into the ComPort input register.
MASTER	Set when the SMT300 bridge owns the ComPort interface token.
TBC RDY	Reflects the current state of the TBC RDY pin. This bit is active high and therefore is an inversion of the TBC pin.
CONFIG_L	Reflects the state of the TIMs' CONFIG signal. Active low.

Table 5: Status Register

INTD is the input interrupt into the CompactPCI Bridge from the SMT300; this can be routed to INTA, INTB, or INTC using the CompactPCI Interrupt Configuration Register (BAR0, offset $4C_{16}$).

4.2.4 Interrupt Control Register (BAR1, Offset 18_{16})

This write-only register controls the generation of interrupts on the CompactPCI bus. Each interrupt source has an associated enable and clear flag. This register can be written with the contents of bits 7:0 of the Status Register. The JTAG controller generates TBC INT and must be cleared of all interrupt sources in order to clear the interrupt.

10	9
DSP-PC IIOF2 En	DSP-PC IIOF1 En

8	7	6	5	4	3	2	1	0
DSP-PC IIOF0 En	CLEAR C40 INT	0	CLEAR IBF INT	CLEAR OBE INT	C40 IE	TBC IE	IBF IE	OBE IE

DSP-PC IIOF2 En	Enables DSP-PC interrupts on IIOF2
DSP-PC IIOF1 En	Enables DSP-PC interrupts on IIOF1
DSP-PC IIOF0 En	Enables DSP-PC interrupts on IIOF0
IBF IE	ComPort Input Buffer Full Interrupt Enable. Allows an interrupt to be generated when the host ComPort input register is loaded with data from the C40.
OBE IE	ComPort Output Buffer Empty Interrupt. Allows an interrupt to be generated when the host ComPort register has transmitted its contents.
TBC IE	Test Bus Controller Interrupt Enable. Interrupts from the Texas JTAG controller are enabled when set.
C40 IE	C40 Interrupt Enable. Allows a programmed interrupt to be generated by the C40 when set.
CLEAR OBE INT	Write a one to this bit to clear the interrupt resulting from a ComPort output event.
CLEAR IBF INT	Write a one to this bit to clear the interrupt event resulting from ComPort input.
CLEAR C40 INT	Write a one to this bit to clear down the C40 INT event.

Table 6: Interrupt Control Register

4.3 ComPort Direction

ComPorts will automatically switch direction during the execution of a program, but when they come out of reset, they will be set to an initial direction: input or output. You should always ensure that you only ever connect pairs of ComPorts that reset to opposite initial directions.

ComPorts resetting as inputs	3, 4, 5
ComPorts resetting as outputs	0, 1, 2

5 Sundance Digital Bus (SDB)

A growing number of Sundance's Modules have an on-board SDB. A description of the SDB interface may be found on the Sundance web site at ftp://ftp2.sundance.com/Pub/documentation/pdf-files/sdb_tech_spec.pdf.

The following register controls the carrier's SDB.

D7	D6	D5	D4	D3	D2	D1	D0
X	X	OFFF	IPFF	RW	RW	RW	RXNTX

Table 7: SDB Control Register

The SDB control and status register is located at BAR2 offset 00200260_{16}. The bit definitions are shown below:

RXNTX	SDB Direction. The SDB direction is set using Jumper J9 (Where's that Jumper?) on the SMT300, When the jumper is removed the SDB is set for receive mode; when the jumper is present the SDB is set for transmit mode. This bit indicates the direction set: 0=Receive, 1=Transmit.
RW	General scratch bits
IPFF	Input FIFO full: When set, a 16-bit value has been latched in the data register ready for reading. This bit is automatically cleared on a read from the data register.
OPFF	Output FIFO full: This bit is set when a 16-bit value is written to the FIFO and is automatically cleared when it has been sent out of the SDB.

The SDB data register is located at BAR2 offset 00200240_{16}. You can write 16-bit values to this location to transfer them over the SDB interface as long as the OPFF flag in the status register is clear and the J9 jumper is present.

6 JTAG Controller

The SMT300 has an on board Test Bus Controller (TBC), an SN74ACT8990 from Texas Instruments. The TBC is controlled from the CompactPCI bus giving access to the on-site TIM and any number of external TIMs. Please refer to the Texas Instruments data sheet for details of this controller. The TBC is accessed in I/O space BAR1 offset 80_{16}.

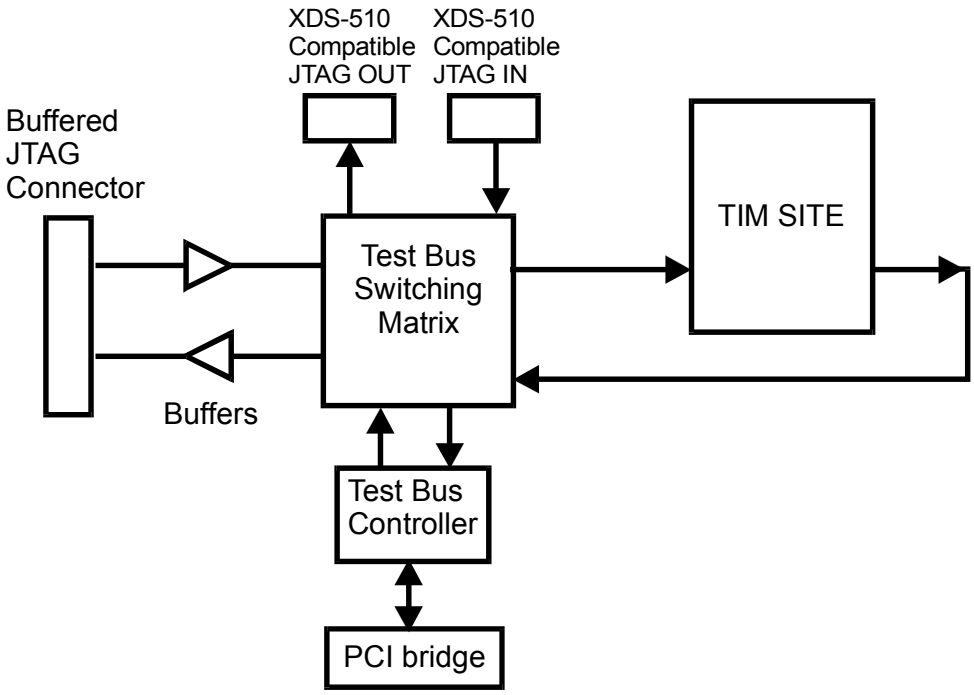


Figure 4: TBC Data Routing

The SMT300 can operate in two TBC modes; Master mode and Slave mode. In Master mode, the Test Bus Controller on the SMT300 drives the JTAG scan chain through the TIM site on the SMT300. If the site is not populated with a TIM then the module's SENSE signal is used to enable a tri-state buffer connecting TDI and TDO (JTAG Data In and Data Out) on the specific site, maintaining the integrity of the JTAG data path. This switching is automatic. The Buffered External JTAG Connector J11 is intended to connect to a JTAG device external to the system chassis. When the SMT300 is in master mode, the buffered JTAG connector acts as a master and is to be connected to JTAG slaves. The un-buffered JTAG out (XDS-510) Header J27 is for use with JTAG slaves within the system chassis. When either of these connectors is connected to a JTAG slave device, the SMT300 automatically detects the device and routes the test data accordingly. Master mode is selected with a jumper in location A on J5.

When the SMT300 is configured in Slave mode, the TBC on the SMT300 is disabled, as the TBC is assumed to be on another device connected to the SMT300. If using a TBC device within the same system chassis, the connection can be made using the XDS-510 compatible connector J28.

In this case, the XDS-510 compatible connector must be selected as the JTAG source by fitting a jumper on J5 in location B. If the TBC device is out side the system chassis, then the External Buffered JTAG connector J11 should be used. Again, this connector must be selected as the JTAG source by fitting a jumper on J5 in location C. The jumpers J5, J11, J27, and J28 can be found in Where's that Jumper?.

Important Note:

There must only ever be one jumper fitted in J5

Multiple SMT300s can be cascaded in a JTAG chain, but the master device must drive out through either the buffered JTAG or the XDS-510 header, not both.

If you require all modules to be reset when using multiple SMT300s, the **Reset In** and **Reset Out** headers must be chained together. See Reset and Config headers.

There are three cable options for the SMT300:

- **SMT501-JTAG** is designed to connect two SMTxxx carrier boards, for example, a SMT300 controlling a SMT328 VME carrier. The length of SMT501-JTAG is 1 meter.
- **SMT510-XDS** is a variant of the SMT501-JTAG, providing an XDS-510 14-way connector to interface to non-Sundance products.
- **SMT503-JTAG-INT** is used to connect to the un-buffered XDS-510 compatible JTAG in and out headers

6.1 Using the SMT300 External/Internal JTAG with TI Tools.

For details on using the SMT300 with Texas Instruments Code Composer, see the SMT6012 documentation.

The SMT6012 is Sundance's driver for Code Composer and can be obtained separately.

The Texas Instruments Evaluation Module (EVM) kits can be used as stand-alone devices with an SMT300 as the JTAG master. When running with the EVM kits ensure that the EVM jumper is set up correctly: External JTAG must be selected and the DSP boot location must be set for internal memory space.

7 Global/Local Bus Transfers, DSP ↔ CompactPCI.

The traditional global bus interface on C6x DSP modules interfaces to the SMT300 via a local bus. This allows Global bus transfers on the DSP to be converted into local bus accesses, giving direct DSP accesses to the CompactPCI Bridge chip.

The resources in the CompactPCI Bridge chip are illustrated in the figure below.

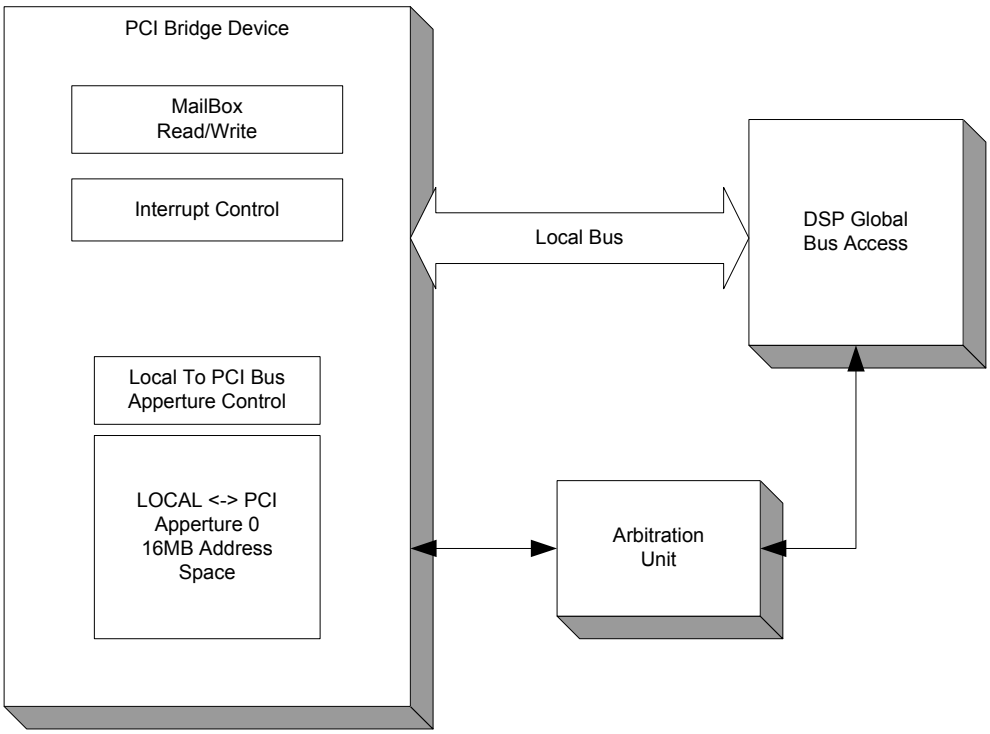


Figure 5: Local Bus to DSP Connectivity

7.1 Mailbox Accesses

The mailbox registers can be used to transfer commands or small amounts of data between the CompactPCI bus and the DSP, via the local bus. The CompactPCI bridge device provides 16 8-bit mailbox registers, which may be used to communicate data between the DSP and Host.

The mailbox registers are accessed from the DSP through the Local-to-Internal Register (LB_IO_BASE) aperture. As illustrated in section 5, table 4 of this document, this region is accessed by the DSP via a global bus access to the CompactPCI Bridge Registers (Address: $1C000000_{16}$).

The mailbox registers are on byte boundaries with offsets $C0_{16}$–CF_{16}, from LB_IO_BASE. As all DSP global bus accesses are carried out in aligned 4-byte units, a write access over the global bus to $1C000000_{16}$ + $C0_{16}$ will write to the first 4 mailbox registers in the CompactPCI Bridge device.

The mailbox registers are accessed from the CompactPCI bus through the CompactPCI-to-Internal Register (PCI_IO_BASE) aperture. This is accessed via the CompactPCI Bridge Chip Internal Register (BAR0, byte offset $C0_{16}$–CF_{16}).

7.1.1 Doorbell Interrupts

Each of the 16 mailbox registers can generate four different interrupt requests called doorbell interrupts. Each of these requests can be independently masked for each mailbox register. The four doorbell interrupt types are:

- DSP interrupt request on read from CompactPCI side
- DSP interrupt request on write from CompactPCI side
- CompactPCI interrupt request on read from DSP side
- CompactPCI interrupt request on write from DSP side

The CompactPCI read and DSP read interrupts are ORed together and latched in the mailbox read interrupt status register (MAIL_RD_STAT). Similarly, the CompactPCI write and DSP write interrupts are ORed together and latched in the mailbox write interrupt status register (MAIL_WR_STAT). All of the interrupt request outputs from the status registers are ORed together to form a single mailbox unit interrupt request and routed to both the Local and CompactPCI Interrupt Control Units.

When several mailbox registers are accessed simultaneously, for example when 4 mailbox registers are read as a word quantity, then each register affected will request a separate interrupt if programmed to do so.

See Interrupts for further information on Interrupts.

7.2 DSP Interrupt Control

Interrupts can be enabled from a number of different sources i.e. DSP►Host and Host►DSP. See section 8 for a description of these functions.

7.3 DSP To Local Aperture 0 control and Accessing

The quickest way to transfer information between the DSP and CompactPCI Bus is to use the Local-to-CompactPCI Aperture 0 in the CompactPCI Bridge device.

A DSP may need to transfer large amounts of acquired data to the PC host for data storage or post-processing. Allowing the DSP to take control of the CompactPCI bus means that the HOST only needs to be involved once the data have been transferred by the DSP to PC memory. Alerting the Host that data have been transferred can be accomplished in a number of ways, for example, by writing to a mailbox register to generate an interrupt.

The Local-to-CompactPCI Aperture 0 is mapped as a region of addressable space from 18000000_{16}–$183FFFFF_{16}$ (words), as shown in Table 4, section 5.

There are several registers to initialise before data can be read or written via this address space:

- Unlock the CompactPCI Bridge System register. This requires a write to the LB_CFG_SYSTEM (offset 78_{16}, BAR 0) with the value $A05F_{16}$.
- Write the upper 8 bits of your destination address (in bytes) to the upper 8 bits of the 32-bit Local Bus to CompactPCI Map 0 register (LB_MAP0_RES, offset in bytes $5c_{16}$).
- Convert you lower 24-bit address to a word aligned value.
- Write/Read data using Local-to-CompactPCI Aperture 0.

7.4 DSP Signals

AE*/DE*	active low address/data enable signals driven by the SMT300. When the DSP has ownership of the bus, these signals are driven low by the SMT300 allowing the DSP to drive the address and data pins.
CE0*	the tri-state control for the DSP's global bus control pins. This is permanently tied low by the SMT300, as the control signals are always enabled.
STRB1*	the data strobe signal from the DSP's global bus. It is driven low when the DSP is carrying out an access cycle. The DSP waits for RDY1* to be driven low by the SMT300 to indicate transfer has been completed. This transfer is carried out in synchronous burst mode. The DSP pulls STAT0 low to signal when the burst transfer has completed.
RDY1*	an active low transfer acknowledgement, driven by the SMT300 to indicate that the current transfer has been completed.
STAT0 **STAT1** **STAT2** **STAT3**	the DSP Status line. When all of the signals are logic '1' then the DSP Global bus interface is in an idle state. When any of these signals is driven low, the DSP is requesting ownership of the SMT300's local bus. STAT0 has a special meaning and is driven low by the DSP to indicate the last data packet transfer.
A0–A30	the DSP's global Bus address lines.
D0–D31	the DSP's global Bus data lines
IIOF0 **IIOF1** **IIOF2**	DSP Interrupt signals. These are open-collector signals on the SMT300 that can be driven by the DSP interrupt the host, or driven by the host to interrupt the DSP

In the timing diagram below all signals change relative to the rising LCLK signal. This signal is the H1 clock signal of the DSP when using the DSP global bus in synchronous mode.

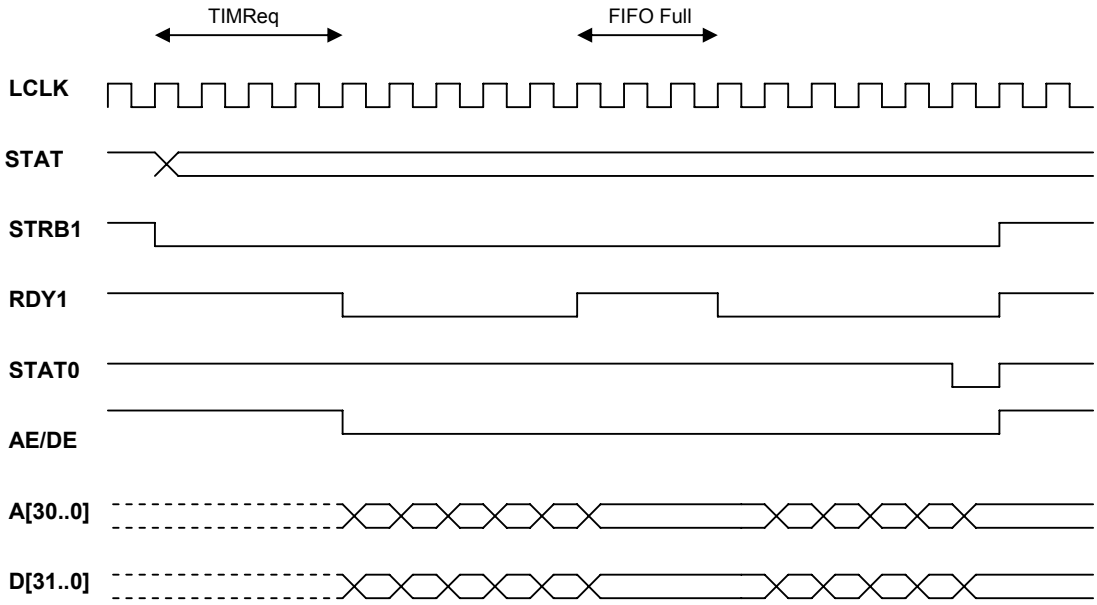


Figure 6: Timing diagram for DSP local bus access

LCLK Period =30ns, frequency is 33MHz.

The DSP initiates a global bus R/W by asserting the STRB1 low and STAT[1:3] change (see the TIM Spec for details of STAT[1..3]). Once the arbitration unit detects this, it waits for the last cycle of the Local bus to be completed by the CompactPCI Bridge, before allowing the DSP to become Bus Master. Once the DSP is Master the arbitration unit drives AE and DE low to enable the DSP's address and data lines. RDY1 is driven low by the arbiter to indicate to the DSP, on the next rising LCLK, that the data packet has been transferred. If the input FIFO (256 words deep) becomes full, the arbitration logic de-asserts the RDY1 signal to indicate a hold-off state.

Once the data have been transferred from the FIFO to the CompactPCI bus, RDY1 is re-asserted to continue the transfer. Asserting STAT0 low indicates the end of the burst access. If RDY1 is not active then STAT0 should remain asserted until ready is asserted and the final data transaction has been completed.

It is possible for a deadlock condition to arise if the CompactPCI bus is trying to read from the SMT300 resources while the DSP is reading from the CompactPCI Bus. If this happens, the arbitration unit gives the CompactPCI Bridge device priority and services the HOST CompactPCI access before giving bus ownership back to the DSP.

When running code composer applications to debug the DSP a reduction in the speed of the debugger may be noticed. The DSP has priority when accessing the local bus and any other accesses will only occur under the following conditions.

- Burst access finishes
- A deadlock condition occurs which forces the DSP to release ownership of the Bus.

For multi-threaded applications the length of the DSP burst can be reduced to allow CompactPCI bus R/W cycles to snatch cycles from the DSP.

8 Interrupts

8.1 SMT300-To-CompactPCI Interrupts

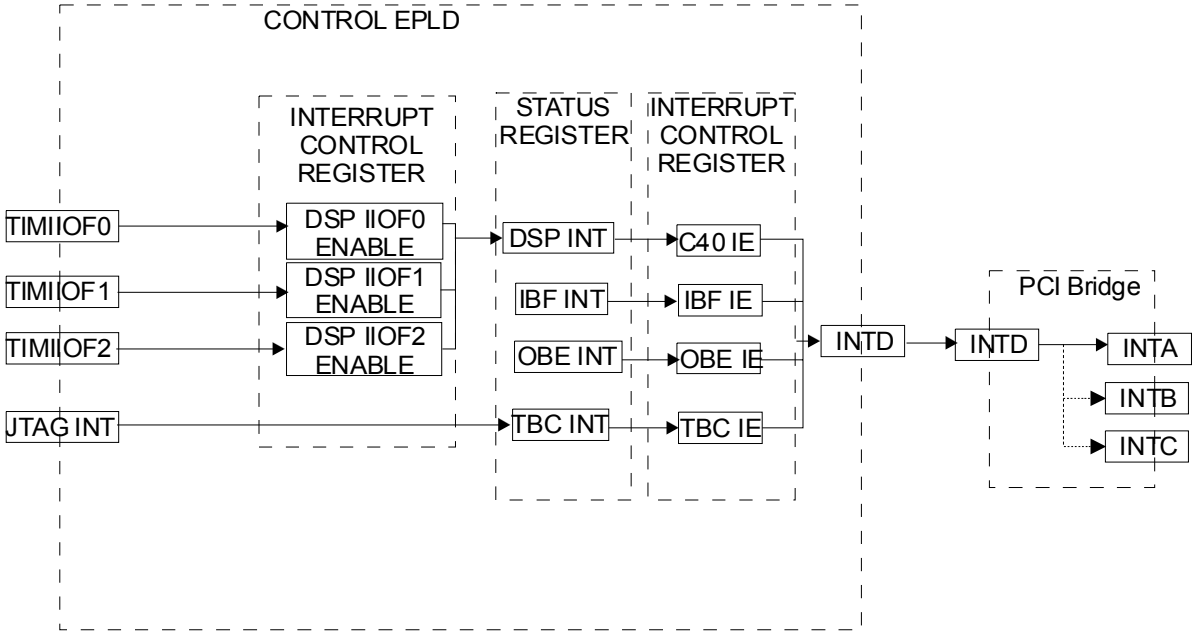


Figure 7: SMT300 to CompactPCI Interrupts

Interrupts can also be generated by the SMT300 writing or reading the mailbox registers in the CompactPCI Bridge.

8.2 CompactPCI-To-SMT300 Interrupts

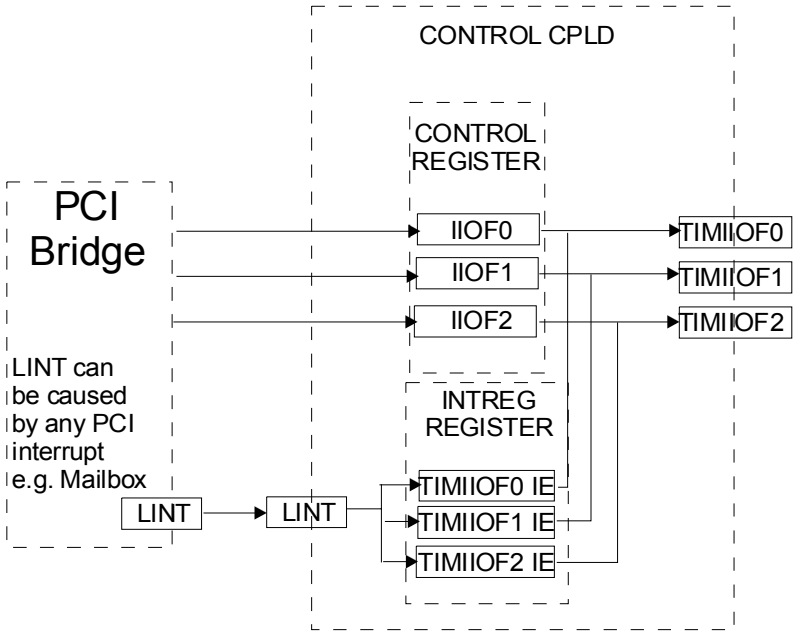


Figure 8: CompactPCI to SMT300 Interrupts

8.3 Interrupt Registers

The following registers are used to control CompactPCI►DSP and DSP►CompactPCI interrupts:

- CompactPCI bridge internal register
- CompactPCI Interrupt Configuration (BAR 0, $4C_{16}$)
- CompactPCI Interrupt Status (BAR 0, 48_{16})
- Local Bus Interrupt Mask (BAR 0, 77_{16})
- Local Bus Interrupt Status (BAR 0, 76_{16})
- CompactPCI Mailbox Write Interrupt Control (BAR 0, $D0_{16}$)
- CompactPCI Mailbox Read Interrupt Control (BAR 0, $D2_{16}$)
- Local Bus Mailbox Write Interrupt Control (BAR 0, $D4_{16}$)
- Local Bus Mailbox Read Interrupt Control (BAR 0, $D6_{16}$)
- Mailbox Write Interrupt Status (BAR 0, $D8_{16}$)
- Mailbox Read Interrupt Status (BAR 0, DA_{16})

Details of these registers can be found in the V363EPC Local Bus CompactPCI Bridge User Manual:
(http://www.quicklogic.com/home.asp?PageID=223&sMenuID=114#Docs)

Other Registers

Control Register (BAR1, Offset 14_{16}, WRITE-ONLY)

Interrupt Control Register (BAR1, Offset 18_{16})

INTREG Register (BAR1, Offset 40_{16})

8.3.1 INTREG Register (BAR1, Offset 40_{16})

Bits	Name	Description
15	-	Reserved
14	-	Reserved
13	-	Reserved
12	-	Reserved
11	-	Reserved
10	-	Reserved
9	-	Reserved
8	-	Reserved
7	-	Reserved
6	-	Reserved
5	-	Reserved
4	-	Reserved
3	-	Reserved
2	IIOF2EN	PC to DSP TIMIIOF2 interrupt enable
1	IIOF1EN	PC to DSP TIMIIOF1 interrupt enable
0	IIOF0EN	PC to DSP TIMIIOF0 interrupt enable

Table 8: INTREG Register

9 Memory Maps

All address information is given in bytes:

9.1 CompactPCI Bus Memory Map

9.1.1 CompactPCI Bridge Chip Internal Register (BAR0)

Please see the User Manual for the V363EPC Local Bus CompactPCI Bridge chip, http://www.quicklogic.com/home.asp?PageID=223&sMenuID=114#Docs, for details of internal registers.

9.1.2 I/O Space Register Assignments (BAR1)

In target mode, a host device accesses the SMT300 across the CompactPCI bus, which gives access to the target mode registers. The operating system or BIOS will normally allocate a base address for the target mode registers of each SMT300. Access to each register within the SMT300 is then made at offsets from this base address as shown in the table below.

Offset	Register (Write)	Register (Read)	Width
00_{16}	-	-	
04_{16}	-	-	
08_{16}	-	-	
$0C_{16}$	-	-	
10_{16}	COMPORT_OUT	COMPORT_IN	32
14_{16}	CONTROL	STATUS	32
18_{16}	INT_CONTROL		32
$1C_{16}$	-	-	
20_{16} to $3F_{16}$	COMPORT Configuration	COMPORT Configuration	
40_{16}	INTREG	INTREG	16
60_{16}	PLLREG1	PLLREG1	16
64_{16}	PLLREG2	PLLREG2	8
80_{16} to AF_{16}	TBC Write	TBC Read	16

Table 9: I/O address space map

9.1.3 Memory Space Assignments (BAR2)

Address	Description	Notes
00000000_{16}–$000FFFFF_{16}$	Shared Memory Bank	1MB SRAM
00200090_{16}	ComPort Data Mirror	Mirror of COMPORT_OUT / COMPORT_IN See Note 2
00200094_{16}	ComPort Status Mirror	Mirror of Control / Status See Note 2
00200098_{16}	ComPort Int_Control Mirror	Mirror of Int_Control See Note 2
00200000_{16}–$0020007F_{16}$	Global Bus	See Note 1
00200240_{16}–0020 $025F_{16}$	SDB Data Register	Input/Output 16 bit SDB Interface
00200260_{16}–$0020027F_{16}$	SDB Control Register	SDB Control/Status

Table 10: Memory space map

Note 1: In order for the TIM to respond to accesses for this area address line GADD30 and GADD19 of the TIM site connector must be decoded as high and GADD7 and GADD5 must be decoded as low.

Note 2: These mirrors of addresses in the I/O Space (BAR1) allow increased transfer speeds across the host ComPort link (in excess of ×10 increase).

9.1.4 DMA Engine

The CompactPCI Bridge DMA processor sees the shared memory at a different address from that used for normal accesses. For normal memory access the memory base address register offset is 00000000_{16}. For DMA access address line A28 (On hardware interface) must be high, therefore DMA memory access starts at 40000000_{16} (not 10000000_{16} as addressing is in bytes).

9.2 Local Bus Memory Map

The table below illustrates the resources and their corresponding address regions when accessed by the Master module.

Local bus access	Description	Notes
18000000_{16}–$183FFFFF_{16}$	Local-to-CompactPCI Aperture 0	CompactPCI Bridge Aperture 0 Space
14000000_{16}–$17FFFFFF_{16}$	Local-to-CompactPCI Aperture 1	CompactPCI Bridge Aperture 1 Space
$1C000000_{16}$–$1C0000FF_{16}$	CompactPCI Bridge Registers	CompactPCI Bridge Internal resisters
$D0000000_{16}$–$D00FFFFF_{16}$	Shared Memory Bank	1MB SRAM

Table 11: Memory space map

10 PLL

The PLL produces three programmable clocks that are available on the user defined pins of the TIM connectors (Bank2CLK pin 1 on J24, Bank3CLK pin 3 on J24, Bank4CLK pin 8 on J23).

These clocks are programmable through registers PLLREG1 and PLLREG2 (BAR1 Offset 60_{16} and 64_{16}).

10.1 PLLREG1 (BAR1 Offset 60_{16})

D15	D14	D13	D12	D11	D10	D9	D8
Bank3CLK Frequency Select				Bank3CLK Phase Shift Select			

D7	D6	D5	D4	D3	D2	D1	D0
Bank2CLK Frequency Select				Bank2CLK Phase Shift Select			

Table 12 : PLLREG1 Register

10.2 PLLREG2 (BAR1 Offset 64_{16})

D7	D6	D5	D4	D3	D2	D1	D0
Bank4CLK Frequency Select				Bank4CLK Phase Shift Select			

Table 13 : PLLREG2 Register

10.3 Frequency Select (Bank 2, 3 and 4)

Frequency (MHz)	MSB			LSB
100 / 1	0	1	0	1
100 / 3	0	1	1	1
100 / 8	1	1	0	1
100 / 12	1	1	1	1

Table 14 : PLL Frequency Select

Each clock output has a programmable phase shift in steps of t_u.

Where $t_u = 1 / (F_{NOM} * N)$

$F_{NOM} = 100$ MHz

$N = 16$

So t_u = 625 ps

10.4 Phase Shift Select (Bank 2)

Phase Shift	MSB			LSB
-4 t_u	0	1	0	1
-2 t_u	0	1	1	1
+2 t_u	1	1	0	1
+4 t_u	1	1	1	1

Table 15 : PLL Phase Shift Select (Bank 2)

10.5 Phase Shift Select (Bank 3 and 4)

Phase Shift	MSB			LSB
-8 t_u	0	1	0	1
-6 t_u	0	1	1	1
+6 t_u	1	1	0	1
+8 t_u	1	1	1	1

Table 16 : PLL Phase Shift Select (Bank 3 and 4)

11 Stand-Alone Mode

For the SMT300 to operate in stand-alone mode Jumper J18 (Where's that Jumper?) must be installed and the Auxiliary power header (J8) connected. The plug for power connector is AMP part N^{o} 640440-8. The connector requires wiring as shown in the pin diagram below. Wire of 0.3 mm^{2} core (22 AWG) should be used.

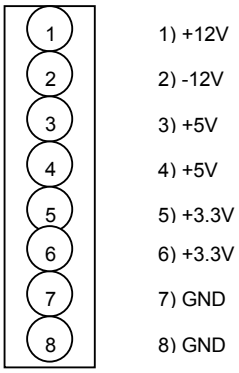


Figure 9: Auxiliary Power Connector

12 Specifications

12.1 Performance Figures

The following performance figures are for the SMT300 with the Rev. **A1** V^3 CompactPCI bridging device fitted and using a SMT335. Further performance figures will be issued as faster V^3 CompactPCI bridging devices become available and are fitted to the SMT300.

The figures shown below may vary greatly depending on the application. Some of the issues are:

- PC Architecture and performance
- Transfer parameters.
  - The transfer size.
  - Frequency of transfer.
  - The layout of the target memory. (Scatter/Gather or contiguous)
- Availability of the CompactPCI bus.
  - Other devices on the CompactPCI bus.
  - Debugging traffic on the bus.
  - ComPort traffic.

12.2 Relative JTAG speed

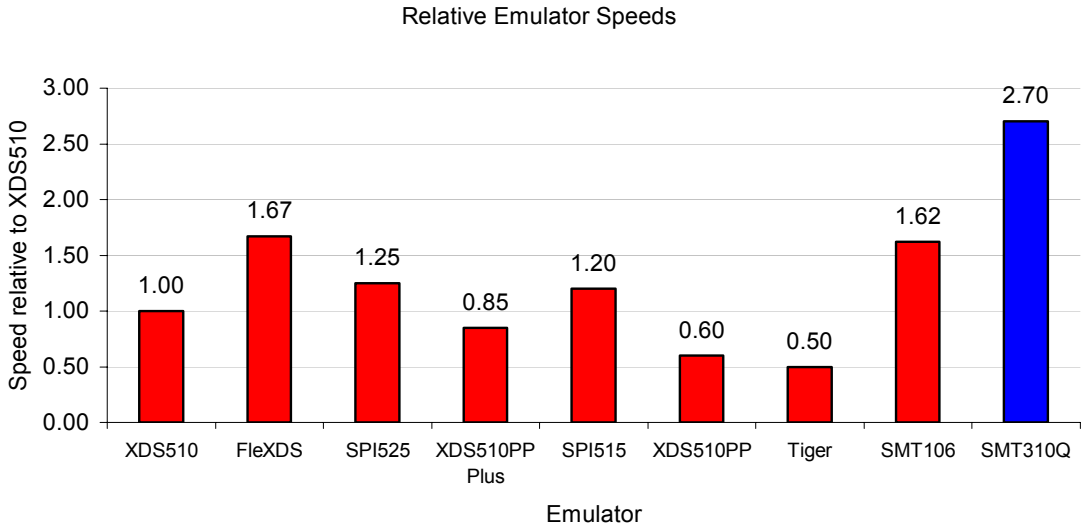


Figure 10: JTAG speed Comparison chart

12.3 Mechanical Dimensions

The board size is 108 mm by 175 mm

12.4 Power consumption

The SMT300 takes 3.3V and 5V power from the PC's internal power supply. The following current consumption figures were measured using a LEM current clamp during a quiescent period.

Current drawn from 3.3v supply: 260mA

Current drawn from 5v supply: 160mA

13 Cables and Connectors

13.1 SDB

No SDB cables are supplied with the SMT300. You can order them separately from Sundance with part number SMT510-SDBxx, where xx is the cable length in centimetres.

13.1.1 SDB Connector

Function	Pin	Pin	Function	Function	Pin	Pin	Function
GND	2	1	CLK	D9	21	22	GND
GND	4	3	D0	D10	23	24	GND
GND	6	5	D1	D11	25	26	GND
GND	8	7	D2	D12	27	28	GND
GND	10	9	D3	D13	29	30	GND
GND	12	11	D4	D14	31	32	GND
GND	14	13	D5	D15	33	34	GND
GND	16	15	D 6	USERDEF0	35	36	GND
GND	18	17	D7	WEN	37	38	REQ
GND	20	19	D8	USERDEF1	39	40	ACK

Table 17: SDB Pin-out

13.2 ComPorts

13.2.1 FMS Cabling

The cables used with FMS connectors are not supplied with the SMT300. You can order them separately from Sundance with part number SMT500-FMSxx, where xx is the cable length in centimetres.

When fitting FMS cables, make sure they have a twist: one end must have the blue side facing out and the other must have the silver side facing out.

Important Note.

If using FMS cables between two SMT300s[3] the reset headers must be connected to ensure that all ComPorts reset at the same time. See Reset and Config headers

[3] This is not recommended as long FMS cables can introduce communication problems.

Pin N°.	Signal	Pin N°.	Signal
1	GND	2	DATA0
3	DATA1	4	DATA2
5	DATA3	6	DATA4
7	DATA5	8	DATA6
9	DATA7	10	/CREQ
11	/CACK	12	/CSTRB
13	/CRDY	14	GND

Figure 11: FMS connector pin out

13.2.2 Buffered ComPort Cabling

Connecting between buffered ComPorts requires a 1 to 1 cable; the SMT502-Buffer is the recommended cable assembly and can be purchased separately.

Cable plugs	3M Scotchflex 10126-6000EL FES part 038740A
Plug shells	3M Scotchflex 10326-A200-00 FES part 038760D
Cable type	3M Scotchflex KUCKMPVVSB28-13PAIR FES part 038781E

This cable has 13 individual pairs, with an overall shield, and an outer diameter of 7mm. Cable length should be as short as possible. The maximum tested cable length is 1 meter.

On reset, each ComPort initialises to being either an input or an output.

Do not connect ‘Reset to Input’ ComPorts together.

Do not connect ‘Reset to Output’ ComPorts together.

However if this should occur, no damage will result, because ComPort direction signals disable relevant ComPorts.

The following table shows connector pin-out and cable pair connections. This is important, as the critical signals must be paired with a ground as shown. The allocation to twisted pairs is based on grouping the data signals because they change at the same time, so that crosstalk is not an issue. Each control signal has its own ground:

Pin	Twisted Pair	RTI Signal	RTO Signal	Pin	Twisted Pair	RTI Signal	RTO Signal
1	1	I/O_OUT	I/O_IN	15	8	D2	D2
2	1	GND	GND	16	8	D3	D3
3	2	I/O_IN	I/O_OUT	17	9	D4	D4
4	2	GND	GND	18	9	D5	D5
5	3	/CSTRB	/CSTRB	19	10	D6	D6
6	3	GND	GND	20	10	D7	D7
7	4	/CRDY	/CRDY	21	11	VCC	VCC
8	4	GND	GND	22	11	GND	GND
9	5	/CREQ	/CREQ	23	12	/RST_OUT	/RST_IN
10	5	GND	GND	24	12	GND	GND
11	6	/CACK	/CACK	25	13	/RST_IN	/RST_OUT
12	6	GND	GND	26	13	GND	GND
13	7	D0	D0	SHELL	-	SHIELD	SHIELD
14	7	D1	D1				

Table 18: Buffered ComPort connector pinout

The overall shield is attached to the body of the metal plug shell.

The signal VCC is fused on the board at 1 amp; the fuse automatically resets when the load is removed.

When the buffered ComPort is reset to input, pins 1 and 23 are always driven and pins 3 and 25 are always receivers. When the buffered ComPort is reset to output, pins 3 and 25 are always driven and pins 1 and 23 are always receivers.

13.3 JTAG cabling

The 20-way JTAG connectors require the following cabling components:

Cable plugs	3M Scotchflex 10120-6000EL, FES part 038739R
Plug shells	3M Scotchflex 10320-A200-00, FES part 038759A
Cable type	3M Scotchflex KUCKMPVVSB28-10PAIR, FES part 038780G

When the SMT300 is configured as a Slave using the Buffered JTAG connector as a JTAG source, the buffered connector pins are used as follows:

Pin	Signal	Direction	Description
1	TDI	IN	JTAG data in
2	GND		
3	TDO	OUT	JTAG data out
4	GND		
5	TMS	IN	JTAG Test mode select
6	GND		
7	TCK	IN	JTAG clock, up to 10MHz
8	GND		
9	TCK_RET	OUT	JTAG clock return
10	GND		
11	/TRST	IN	JTAG Reset
12	GND		
13	/RESET	IN	Board Reset in
14	PD	OUT	Presence detect, +5V 1A fused
15	/DETECT	IN	Detect external JTAG controller when grounded
16	CONFIG	OPEN COLL	Global open collector C4x CONFIG
17	EMU0	OUT	Buffered EMU0 output
18	EMU1	OUT	Buffered EMU1 output
19	SPARE1		
20	SPARE2		

Table 19: Buffered JTAG connector pin functionality as JTAG source

When the SMT300 is configured as a Master, using the Buffered JTAG connector to connect to a JTAG slave, the buffered connector pins are used as follows:

Pin	Signal	Direction	Description
1	TDI	OUT	JTAG data out
2	GND		
3	TDO	IN	JTAG data in
4	GND		
5	TMS	OUT	JTAG Test mode select
6	GND		
7	TCK	OUT	JTAG clock 10MHz
8	GND		
9	TCK_RET	IN	JTAG clock return
10	GND		
11	/TRST	OUT	JTAG Reset
12	GND		
13	/RESET	OUT	Board Reset out
14	PD	IN	Presence detect when pulled high
15	/DETECT	OUT	Detect external JTAG controller when grounded
16	CONFIG	OPEN COLL	Global open collector C4x CONFIG
17	EMU0	IN	Buffered EMU0 output
18	EMU1	IN	Buffered EMU1 output
19	SPARE1		
20	SPARE2		

Table 20: Buffered JTAG connector pin functionality as JTAG master

Pin	Signal	Direction	Description
1	TMS	Out	JTAG Test mode select
2	/TRST	Out	JTAG Reset
3	TDI	Out	JTAG data out
4	GND		
5	PD (+5)		5v Power
6	Key		No pin fitted
7	TDO	In	JTAG data in
8	GND		
9	TCK_RET	In	JTAG clock return
10	GND		
11	TCK	Out	JTAG clock 10MHz
12	GND		
13	EMU0	In	Buffered EMU0 In
14	EMU1	In	Buffered EMU1In

Table 21: Internal JTAG out (XDS-510) pin descriptions

Pin	Signal	Direction	Description
1	TMS	In	JTAG Test mode select
2	/TRST	In	JTAG Reset
3	TDI	In	JTAG data in
4	GND		
5	PD (+5)		5v Power
6	Key		No pin fitted
7	TDO	Out	JTAG data out
8	GND		
9	TCK_RET	Out	JTAG clock return
10	GND		
11	TCK	In	JTAG clock 10MHz
12	GND		
13	EMU0	Out	Buffered EMU0 Out
14	EMU1	Out	Buffered EMU1 Out

Table 22: Internal JTAG in (XDS-510) pin descriptions

13.4 Reset and Config headers

There are pairs of headers for /TIMRESET and /TIMCONFIG to allow several SMT300s to be chained together. The /TIMRESET headers are J26 (Reset Out) and J29 (Reset In), and the /TIMCONFIG headers are J16 (Config Out) and J10 (Config In).

Below is the pin out for each header:

Pin	Signal
1	/TIMRESET
2	GND

Table 23: Reset header pin out (IN/OUT)

Pin	Signal
1	/TIMCONFIG
2	GND

Table 24: Config header pin out (IN/OUT)

Pin 1 of header is the lower pin. These headers should be chained together for all boards in the system, Out to In.

14 JTAG Interface circuits

The buffered JTAG circuit on the SMT300 allows connection between SMT300 cards and other compatible carrier modules. This section describes the JTAG interfacing circuitry to customers custom-built slave devices.

14.1 Signal Description

Signal	Description
TDI	JTAG Test Data In. The **master** device drives this signal.
TDO	JTAG Test Data Out. The **slave** device drives this signal.
TMS	Test Mode Select. Driven by the **master** device.
TCK	JTAG Clock. Driven by the **master**
TCK_RET	JTAG Clock Return, driven by the **slave**.
/TRST	JTAG Reset, driven by the **master**.
/RESET	Board Reset. Driven my **master**. (Unused on SMT300)
PD	Pod Detect signal. This signal should be connected 3.3V or 5V on the slave device to indicate to the master that an external device is present.
/DETECT	A master pulls this signal to GND. If connecting two SMT300 together a jumper is used on one of the carriers (switching it to slave mode) to prevent two masters being connected together.
CONFIG	This signal is unused and should be left unconnected.
EMU0,EMU1	These are open collector JTAG emulation pins and should be connected to the DSP. Pull-up resistors are required.

Table 25: JTAG signals

The JTAG circuit for a slave target board is shown. Using the correct buffers and connectivity is essential to achieving a working JTAG interface.

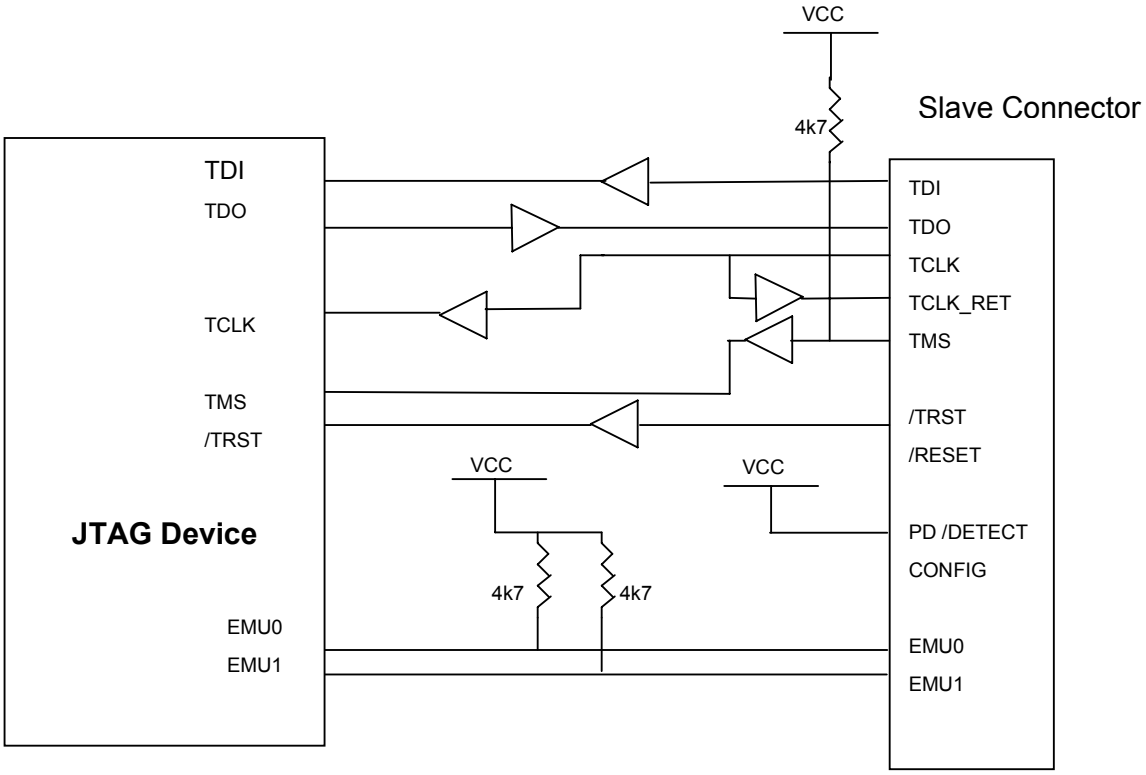


Figure 12: JTAG Slave circuit

All buffers are of type 74FCT244 (5V) / 74LV244 (3.3V) or equivalent.

N.B. When the JTAG device is NON-5v tolerant ensure that 3.3v buffers are used.

15 Firmware Upgrades

Much of the SMT300's control interface is achieved using EPLDs. Sometimes customers require slightly different interface protocols (i.e., SDB interface); this can be catered for by a firmware upgrade. To upgrade the firmware, Xilinx JTAG programming software is required together with a lead to connect to the SMT300's header. The image below shows the location of pin 1 of the JTAG connector J21. This connector is a 2×3 2mm pin header.

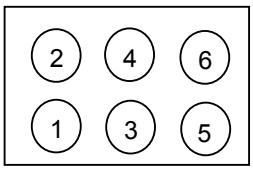


Figure 13: JTAG header pin numbers

Pin Number	Function
1	Vcc (5v)
2	Gnd
3	TCK
4	TDO
5	TDI
6	TMS

Table 26: JTAG Header pin function

There are 3 things you require to update the CPLDs on a SMT300

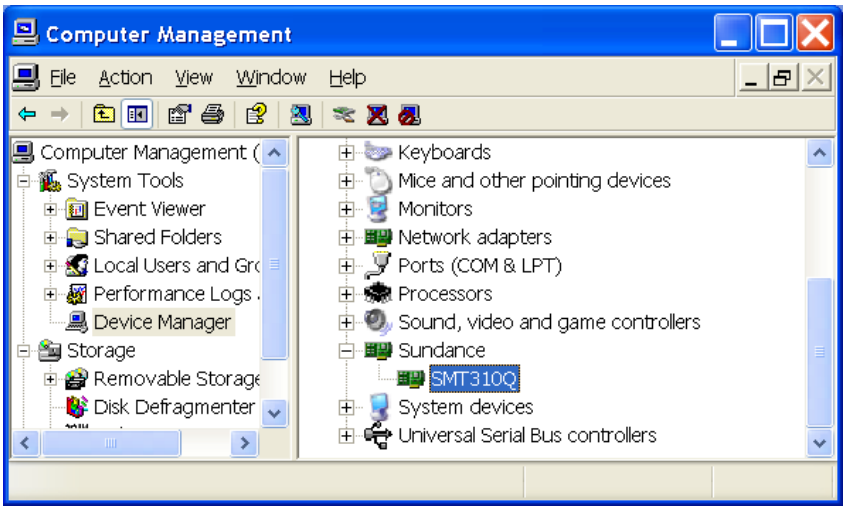
- The software package for Xilinx you will require is called Webpack. It is free and it includes Impact that will allow you to reprogram the CPLDs on the SMT300. You can download it from http://www.xilinx.com/xlnx/xil_prodcat_landingpage.jsp?title=ISE+WebPack
- The JTAG programming cable (Parallel Cable IV $95). The cable can be order on the Xilinx website. http://www.xilinx.com/xlnx/xil_prodcat_product.jsp?title=csd_cables
- The adaptor to connect the parallel cable to the header J21 is shown in the table above.

16 Checking for hardware resource conflicts

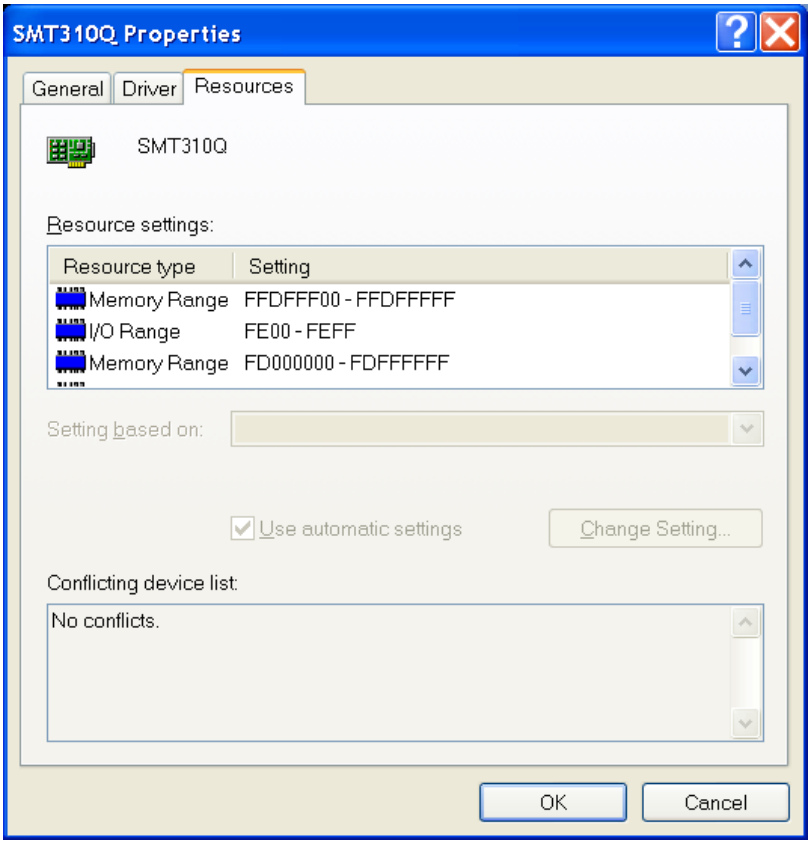
For 2000 and XP users:

Check for any resource conflicts by right clicking on the "My Computer" icon, and selecting "Manage" from the menu.

Select the "Device manager" in the left pane and the Sundance carrier board in the right.



Ensure that there are no resource conflicts by right clicking on the carrier board and selecting "Properties" from the menu.



If there are conflicts:

- Try inserting the carrier board into another CompactPCI slot.
- Try removing other CompactPCI devices.

17 Where's that Jumper?

Below is a diagram to help locate the jumpers:

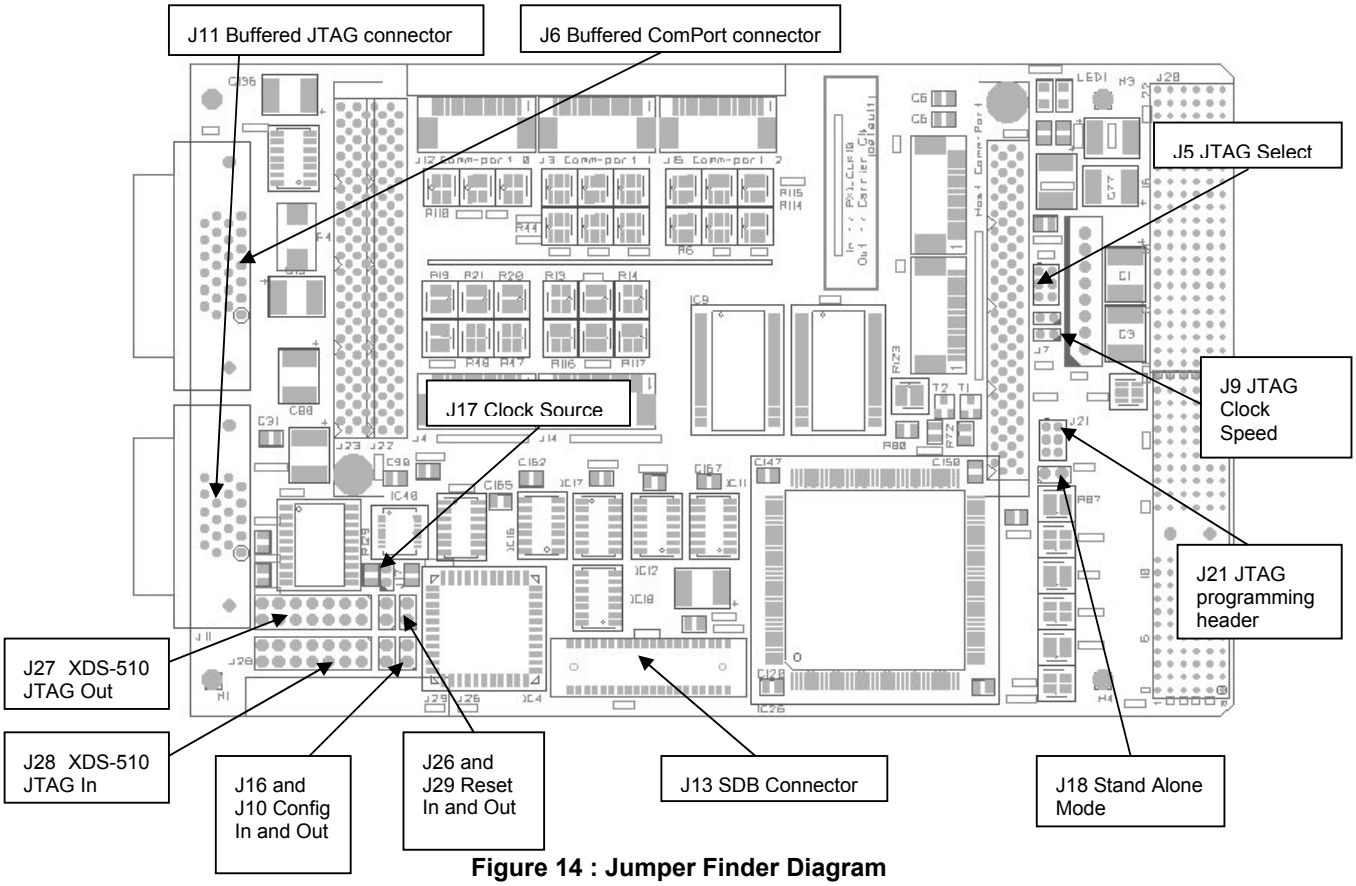


Figure 14 : Jumper Finder Diagram