Unit / Module Name:	VME Quad Site Module Carrier
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Outline Description

The SMT329 is a VME four-site module carrier developed to provide access to TIM Modules over the VME64 (parallel) and VXS (serial) busses. It is backward compatible with the Smt328, and can replace the Smt328 with no software modifications. By implementing the VME64 2eSST standard it offers up to 320M bytes/sec (2.56G bits/sec) across the VME bus, while 8 VXS ports offer up to 2.5G bits/sec each, making a VXS total of up to 20G bits/sec.

The SMT329 has 8M bytes of high speed static ram arranged as 1M by 64 bits, operating at 200MHz with up to 1.6G bytes/sec (12G bits/sec) throughput for 64 bit transfers.

Buffered front panel JTAG ports allow control and debug of all 4 TIM modules simultaneously, and multiple SMT329s.

All communications apart from JTAG and ComPorts are controlled by a single Virtex 4 FPGA.

The 6 ComPorts on each TIM (3 reset to out and 3 reset to in), and 2 ComPorts on the Virtex 4 (2 reset to out), are connected to a crossbar switch which allows a static configuration to specify which of the 14 reset to out ports is connected to each of the 12 reset to in ports. The switch is implemented in a Xilinx Spartan 3 FPGA. The switch topology is stored in NVRAM and copied to the switch at board reset by the Virtex4.

The 2 RSL ports on each TIM are connected to Virtex4 Rocket-IO ports.

Four Gigabit Ethernet ports are available on the VME P2 connector.

Two TIM sites have global bus interfaces to the Virtex4 for access to the static ram and VME bus.

A cut down SMT329 can be assembled with 3 row P1 & P2 connectors (VME64 has 5 row connectors), no P0 connector, and an on board 3.3V PSU. This version can be used in legacy VME racks. It does not guarantee to support 2eVME or 2eSST and does not support VXS, but it does retain the four Gigabit Ethernet ports on the P2 connector.

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Revision History

	Changes Made	Issue	Initials
19Jun05	**Revised draft**	**02**	**SEC**
25Jun05	**Replaced Pericom crossbar by Xilinx Spartan3, added detailed descriptions**	**03**	**SEC**
19Dec05	**Replaced FRAM with FLASH, added PCB placements**	**10**	**SEC**
10Jan06	**Typo corrections**	**1.01**	**FC**

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1 Introduction

The SMT329 allows four ‘C6x DSP Modules\FPGA Modules and/or slave I/O Modules to be integrated into a powerful processing system based on the VME64 standards. The SMT329 can accept up to four different processing or IO modules or two dual-width modules. It is a VME bus slave and bus master. It is backwards compatible with the SMT328, and can replace the SMT328, and offer higher performance, with no changes to the existing application(s).

1.1 Overview

The high speed 8M byte shared SRAM acts as a data transfer buffer. This is directly accessible via the Global Bus interfaces of two of the TIM sites and the VME64 bus, with programmable mailbox interrupts to any of these three busses. Additionally data from any of the Ethernet or Rocket-IO ports on the Virtex4 can be transferred by DMA to or from the sram. The sram is organized as 1M by 64 bits and is clocked at 200MHz, so peak throughput for 64 bit transfers is 1.6G bytes/sec.

The buffered front panel JTAG interface allows systems to be debugged using Code Composer Studio IDE. The JTAG interface is fully buffered to allow multiple SMT329 carriers to be debugged in a single JTAG chain, with suitable cabling.

Four single width or two double width TIM Modules can be fitted. Comms port communication between modules is through a cross bar switch, which allows the creation of a parallel processing system with any comms port topology. Each TIM site has 6 comms ports, 3 reset to in and 3 reset to out, each of which is connected to the comms port cross bar switch, along with 2 reset to out ComPortsin the Virtex4. This allows standard comms port communications over the VME bus. This connectivity is static and strictly point to point. The static connectivity map is loaded by the Virtex4 at board reset, and is not dynamically configurable. The configuration is held in flash memory, which can be write protected.

The enhanced VME64 interface allows data packets to be exchanged with the VME64 bus at speeds up to 320M bytes/sec using the 2eSST protocol. The data is moved to and from the sram using direct or auto increment addressing.

Each TIM site has 2 RSL ports, which are connected to Rocket-IO ports on the Virtex4. RSL data can be routed between TIMs, or from TIM to VSX bus, or from TIM to sram using DMA and or from VSX port to sram using DMA. This connectivity is static and strictly point to point. The static connectivity map is loaded by the Virtex4 at board reset, and is not dynamically configurable. The configuration is held in flash memory, which can be write protected.

The Virtex4 also provides 4 off 1 Gigabit Ethernet ports which are connected to the VME P2 “user-defined” pins, so they are available at the back plane. The data packets can be routed to or from the sram only. As the Virtex4 has 16 Rocket-IO transceivers, the Gigabit Ethernet ports are shared with 4 of the VXS ports. The ratio of VXS to Gigabit Ethernet ports available is fixed at assembly. An intelligent TIM is required to manage the Ethernet interface.

Two of the TIM sites have Global Bus connectors which allow direct access to the sram, the VME bus (as a bus master) and the control registers in the Virtex4.

1.2 Related Documents

SMT328 User Guide, version 7.1 dated 30/01/01

Texas Instruments TIM-40 Module Specification

VME64 Ansi standard, ANSI/VITA 1-1994 (R2002)

VME64 Extensions ANSI/VITA 1.1-1997

2eSST ANSI/VITA 1.5-2003

VXS VITA 41.0-200x (draft)

SN74VMEH22501A data sheet Texas Instruments SCES620 – DECEMBER 2004

2 Functional Description

Figure 1 shows the SMT329 block diagram. All communications apart from the comms port switching are routed through the Xilinx Virtex4 fpga, including all ram i/o. Comms port cross bar switching is performed by a Xilinx Spartan3.

2.1 Block Diagram

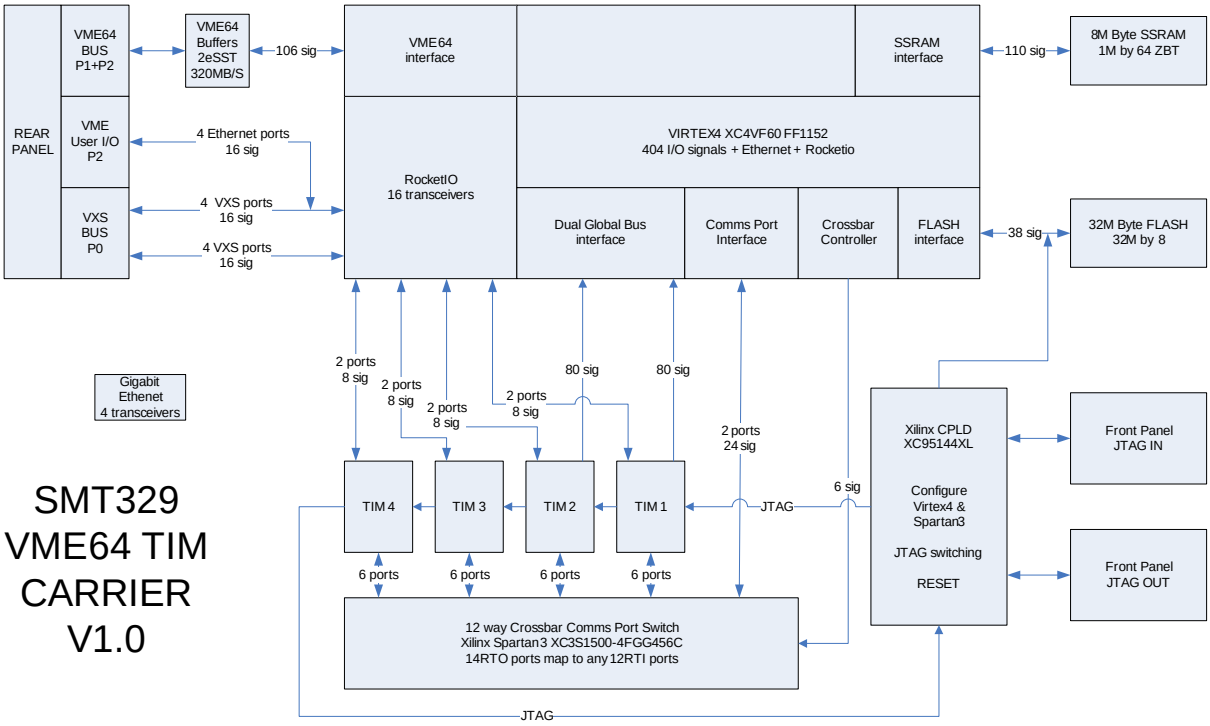


Figure 1: SMT329 Architecture

The VME64 bus is buffered with SN74VMEH22501A transceivers from TI which are specially designed to be compliant with VME64, 2eVME protocols in VME64x (ANSI/VITA 1.1) and 2eSST protocols in VITA 1.5. With proper design of a 21-slot VME system, a designer can achieve 320-Mbyte transfer rates on linear backplanes and, possibly, 1-Gbyte transfer rates on the VME320 backplane. The use of high speed transfer modes (2eVME and 2eSST) on legacy backplanes is not supported, and may or may not function reliably. A cut down SMT329 can be assembled with 3 row P1 & P2 connectors (VME64 has 5 row connectors), no P0 connector, and an on board 3.3V PSU. This version can be used in legacy VME racks. It does not guarantee to support 2eVME or 2eSST and does not support VXS, but it does retain the four Gigabit Ethernet ports on the P2 connector.

Figure 2 shows the SMT329 bus architecture within the Virtex4. This is backwards compatible with Smt328, with the addition of a 4 channel Ethernet DMA engine, a 4 channel Rocket-IO DMA engine, and a Rocket-IO cross bar switch matrix.

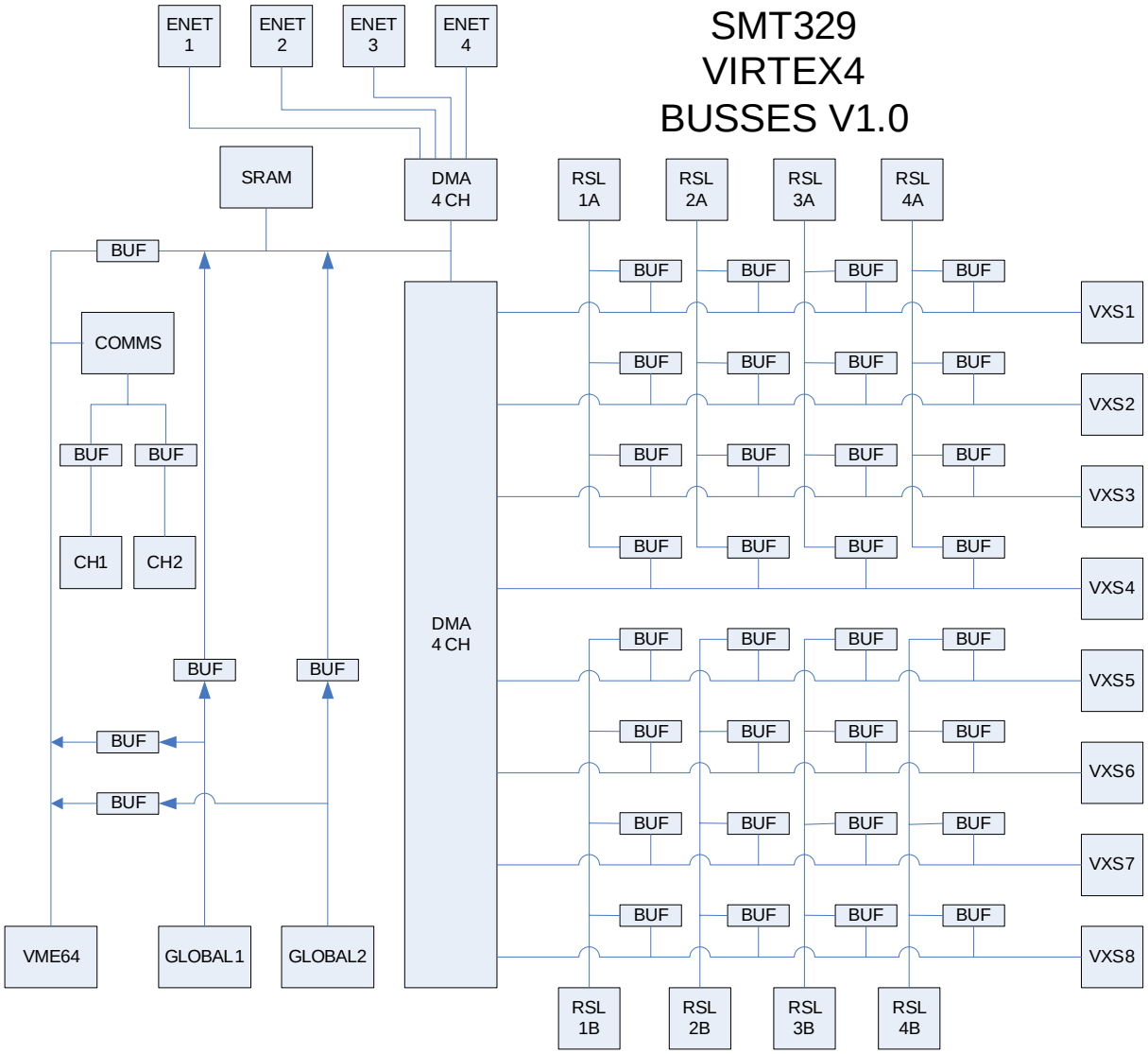


Figure 2: SMT329 Virtex4 internal bus architecture

2.2 Global Bus Resources

There are three global bus resources available to TIMs on this motherboard. These are the 32 bit VME bus, the 8 Megabyte static ram (sram), and the board control registers.

The two TIM sites with a global bus connector are the two nearest the VME connectors, at sites 1 (nearest P1) and 4 (nearest P2). The VME bus is directly accessible to the TIMs without routing via the sram bus, as in SMT328. This allows the TIMs to act as a VME bus master without reducing the availability of the sram to the communications DMA controllers.

The SRAM is organised to allow the VME bus master to perform D8, D16, D32 or D64 cycles, word swapping buffers are included for this purpose. Transfers can be single, or burst using either 2eVME or 2eSSTT. The SRAM is clocked at 250MHz, and the TIMs can access the SRAM with zero wait states, after arbitration for the SRAM bus.

Access to the global resources is selected by an arbitration state machine. Resources remain granted to the last resource master after the cycle has finished so that contiguous transfers proceed without further arbitration. Arbitration only occurs when two (or more) possible bus masters are requesting the same resource.

Because the TIMs have direct access to the VME bus, the risk of deadlock that was present in the SMT328 is now removed. This is because the VME bus arbiter, on another VME bus board, is the only arbiter in the path to granting bus master access to the VME bus for the TIM, whereas on SMT328 the VME bus arbiter and the SRAM bus arbiter both had to grant access.

2.3 VME to ComPort Interface

The VME interface, is designed to allow a VME bus master to perform D16, D32 or D64 cycles, to access the ComPort interface register. These accesses are converted to the correct protocol for communicating via a TIM comm port. This logic and associated circuitry includes fifo buffering on reads and writes. The reset to out ComPort which is connected to this interface can be switched to any TIM reset to in ComPort through the ComPort switch. There are 2 ComPort channels (ch0 & ch1) from the Virtex4 to the ComPort switch. The switch can connect each of these 2 channels (ch0 & ch1) to a different reset to in port on a TIM. Note that there is only 1 VME ComPort interface, and that a software switch allows dynamic switching of the VME ComPort interface between channel 0 and channel 1.

2.4 Interrupts

All interrupts are controlled by the Virtex4. It contains a status register showing unmasked interrupt sources, and mask registers. These allow the interrupt sources to be masked, before they are logically ORed, to generate interrupt inputs, one for each of the global TIM sites and one for the VME bus.

A VME interrupt, with programmable level, can be generated by either global access TIM. From each of these TIMs, the IIOF0 signal is connected to the interrupt controller, and the assertion of this line generates the interrupt if it is unmasked. The interrupt is cleared by the VME master, when it masks the source of the interrupt.

The Global TIM sites have the following interrupt sources:

A latched copy of VME bus error.

A software settable interrupt.

SRAM mailbox interrupts.

DMA controller interrupts.

The VME bus has the following interrupt sources:

A software settable interrupt.

TIM1 IIOF0 output

TIM4 IIOF0 output

VME ComPort RXFUL

VME ComPort TXEMPTY

SRAM mailbox interrupts.

DMA controller interrupts.

3 VME Interface

The VME64 interface uses the P1 connector and the centre row (B) of the P2 connector. The interface forms a complete D8/16/32/64 master/slave with additional 2eVME and 2eSST transfer modes. The SMT329 does not support slot 0 operation or unaligned transfers. The outer rows (A and C) of the P2 connector carry the Gigabit Ethernet connections with some pins remaining unconnected. The P2 input signals are connected to 10K Ohm pull ups to +5V so that operation is possible without a P2 back plane. In this configuration all transfers must be 16 bits and the I/O and DPR spaces must be set to addresses in the range: 0xFF000000 to 0xFFFFFFFF.

3.1 VME Slave Interface

There are 3 decoded address spaces:

Name	VME space	Size in Bytes	Description
VME configuration	A16	64	Identification and programmable base addresses for I/O and SRAM.
I/O	A32	256	ComPort, Board Reset, Control 1
SRAM	A32	8M	SRAM

The A16 VME configuration base address is set with an 8 way link block labelled SW1. This sets the value to compare to VME A6-A13, with A14-A15 always compared to 1 in order to generate a board decode. This A16 address space contains board identification registers and a pair of 16 bit registers which must be loaded with the base address of the I/O and SRAM spaces.

3.2 VME Master Interface

The SMT329 can support D8, D16, D32 and D64 transfers in A16, A24 and A32 address spaces. The TIM global data bus signals drive the VME data bus through buffers, but no byte or word swapping is performed. That is a D8 transfer to VME address 0x0000 would need the significant data to be in the global bus data bits 7..0. A D8 transfer to address 0x0001 would need the significant data to be in the global bus data bits 15..8. etc.

No support is provided for accessing words or long words across long word boundaries. i.e., all transfers must be aligned within long word boundaries.

The global bus address lines A0..A21 drive the VME address lines A2..23 to allow direct addressing. The VME DS signals and the VME address bits A1, A24-31, AM0-5, LWORD are set by the contents of Control register 4. This requires the use of a 4M Word global bus address region for VME bus master access.

3.3 VME Configuration Registers

The address of this configuration register block is defined by an 8-bit DIL switch (SW1). It is only accessed in A16 address space. The top two address lines (A14 and A15) must be '1'. The base address (set by SW1) is compared to address bits A6 to A13. The address bits A1 to A5 select which register to access.

Offset (hex)	**Register**
00	Board ID
02	Device type
04	Status / Control
06	DPR base address
08	I/O base address
0A-1D	Unused
1E	Manufacturer ID
20-3F	Unused

SW1 switch 1 corresponds to A13 and switch 8 to A6. When a switch is on the corresponding address bit must be 1 for the address to be decoded.

For example:

Address 0xC000 = All off

Address 0xD000 = All off except switch 2

Address 0xF800 = All on except switches 1,2,3

Address 0xFFC0 = All on

The VME address modifiers must be set to 0x29 or 0x2D as these define an A16 transfer.

3.3.1 VME ID Register (00)

The bit definitions for this register are:

Bit	Definition
11..0	Manufacturer ID (123 decimal)
13..12	01
15..14	01

Always reads as 507B hex.

3.3.2 VME Device Type Register (02)

The bit definitions for this register are:

Bit	8M byte SRAM
11..0	Model code (329 decimal)
15..12	Memory size (8 decimal)

Memory size is defined as the number of significant bits in an A32 address used to specify the SRAM base address.

So this register reads as: 0x8149

3.3.3 VME Status Register (04)

The bit definitions for the read only status register are:

Bit	Definition
0..1	0
2	1
3	Ready (connected to TIM config lines)
4	1
5..14	0
15	A32 enabled

3.3.4 VME Control Register (04)

The bit definitions for the write only control register are:

Bit	Definition
0	Reset board when set

15	Enable A32 when set

Bit 15 is cleared by a board reset so that the A32 base address registers can be initialised before A32 enable is set. A32 enable MUST be set to allow A32 access to the rest of the board.

If this bit is clear (0) then no A32 access will be decoded and a bus error will occur for all A32 read/write cycles.

It is very strongly recommended that all VME bus cycles have some form of BUS_ERROR checking enabled, as it is an essential error reporting feature which should not be ignored.

3.3.5 VME SRAM Offset Register (06)

This 16-bit register defines the base address of the SRAM for A32 addressing modes. The most significant 8 bits of this register are compared to VME address signals A31..24. The number of significant bits is specified in the 'Device Type' register.

3.3.6 VME I/O Offset Register (08)

This 16-bit register is used to set the base address (in 256 byte blocks) of the I/O address space.

This base address is compared to the incoming A32 address bits A8-23, while bits A24-31 are compared to FF hex. A match decodes a 256 byte space which is further decoded to access the various devices in the I/O address space.

3.3.7 VME Sub-class Register (1E)

The bit definitions for this 16-bit read only register are given below:

Bit	Definition
11..0	Manufacturer ID (123 decimal)
14..12	Manufacturer sub-class (1)
15	0

Always reads as 107B hex.

3.4 Summary of VME Address decoding

There are 3 VME block decodes:

VME Decode	VME A31..24	VME A23..16	VME A15..8	VME A7..0	VME space
Config	nnnnnnnn	nnnnnnnn	11aaaaaa	aaxxxxxx	A16
SRAM	bbbbbbbb	yyyyyyyy	yyyyyyyy	yyyyyyyy	A32
IO	11111111	cccccccc	cccccccc	zzzzzzzz	A32

Symbol	*3.4.1.1.1 Description*
A16	VME Address modifiers AM=$29 or $2D
A32	VME Address modifiers AM=$09 or $0D
x	VME Config register select for D16 transfer
y	VME SRAM address select for D16 or D32 transfers
z	VME IO register select for D16 or D32 transfers
a	Manually set at LK1: 1=Off, 0=On
b	Programmed in register SRAM Offset
c	Programmed in register IO Offset
n	Do not care bit

3.5 Control and Status Registers

There are 6 control registers:

3.5.1 Control Registers 1 & 2 = TIM Sites 1 & 4 Interrupt Masks

The VME bus error signal can generate a TIM interrupt at either site 1 or 4. Each of these TIM sites has its own register which is accessible to both the VME bus and the TIMs. The registers are the general control register 1 for TIM site 1, and general control register 2 for TIM site 4. These registers are identical. Note that 'VME Bus Error' is latched by either of the bit 8 masks below. Therefore both must be cleared to unlatch 'VME Bus Error', and at least 1 must be set to latch 'VME Bus Error'.

The software interrupt will always generate an interrupt when it is unmasked.

Note that a TIM must execute an 'IACK' instruction to external memory before any TIM interrupts can be generated. The SRAM mailbox, Ethernet DMA and Rocket-IO DMA have interrupt status and mask bits for each channel.

Bit	Definition
0	Software interrupt
1	Unused
2	Unused
3	SRAM mailbox 1
4	Ethernet DMA Ch1
5	Ethernet DMA Ch2
6	Ethernet DMA Ch3
7	Ethernet DMA Ch4
8	VME Bus Error mask
9	Unused
10	Unused
11	SRAM mailbox 2
12	Rocket-IO DMA Ch1
13	Rocket-IO DMA Ch2
14	Rocket-IO DMA Ch3
15	Rocket-IO DMA Ch4

General Control Registers 1 and 2

3.5.2 Control Register 3 = VME Interrupt Masks

Each of the two TIM sites 1 and 4 can generate an interrupt on the VME bus. The interrupt level is selected by bits 12 ..10 of Control Register 4. These can be enabled within the general control register 3 bits, described below. Also the VME ComPort can generate Receiver and Transmit ready interrupts, and there is a software interrupt which occurs as soon as it is unmasked.

Bit	Definition
0	Software interrupt
1	VME ComPort RX full
2	VME ComPort TX empty
3	SRAM mailbox 1
4	Ethernet DMA Ch1
5	Ethernet DMA Ch2
6	Ethernet DMA Ch3
7	Ethernet DMA Ch4
8	VME Bus Error mask
9	TIM1 IIOF0
10	TIM4 IIOF0
11	SRAM mailbox 2
12	Rocket-IO DMA Ch1
13	Rocket-IO DMA Ch2
14	Rocket-IO DMA Ch3
15	Rocket-IO DMA Ch4

General Control Register 3

3.5.3 Control Register 4 = VME Bus Master cycle control

This 32-bit control register is defined as the general control register 4, and the function is described below.

Bit	Definition
7..0	VME interrupt acknowledge vector
8	VME DS0 during bus master cycle
9	VME DS1 during bus master cycle
12..10	VME interrupt level request bits 2..0
14..13	VME Bus request level bits 1..0
15	ComPort to Ch1 when 1, Ch0 when 0
16	VME A1 during bus master cycle
17	VME LWORD during bus master cycle
23..18	VME AM5..0 during bus master cycle
31..24	VME A31..24 during C4x master cycle

General Control Register 4.

If no response from the addressed slave is observed within a fixed time (time-out period) then the VME Slot 0 controller will generate a 'Bus Error', the 'C4x cycle will be terminated and a VME Bus Error interrupt generated.

3.5.4 Control Register 5 = General Status Register

A status register is available for access by the TIMs and the VME. It contains the status of all interrupts before they are masked. The bit definitions are shown below:

Bit	Definition
0	Software interrupt
1	VME ComPort RX full
2	VME ComPort TX empty
3	SRAM mailbox 1
4	Ethernet DMA Ch1
5	Ethernet DMA Ch2
6	Ethernet DMA Ch3
7	Ethernet DMA Ch4
8	VME Bus Error mask
9	TIM1 IIOF0
10	TIM4 IIOF0
11	SRAM mailbox 2
12	Rocket-IO DMA Ch1
13	Rocket-IO DMA Ch2
14	Rocket-IO DMA Ch3
15	Rocket-IO DMA Ch4

General Control Register 5

3.5.5 Control Register 6 = VME High Speed Bus Master cycle control

This 32-bit control register is defined as the general control register 6, and controls the 2eVME and 2eSST high speed bus master transfer modes. For backwards compatibility with SMT328, this register has no effect following a board reset, until it is enabled by software.

Bit	Definition
0 to 31	TBD

General Control Register 6.

3.6 VME I/O Addressing

The VME I/O space occupies 256 bytes, and the VME address of these registers is an offset from the value set in the VME I/O Offset register:

VME Offset	Global Bus address	Peripheral	Read/Write
TBD	TBD	Ethernet DMA1-4	Read/Write
TBD	TBD	Rocket-IO DMA1-4	Read/Write
TBD	TBD	Xilinx Config EEPROM	Read/Write
TBD	TBD	FRAM address	Read/Write
TBD	TBD	FRAM data	Read/Write
TBD	TBD	Ch1 Mailbox Interrupt control	Read/Write
TBD	TBD	Ch2 Mailbox Interrupt control	Read/Write
80	None	ComPort data	Read/write
84	None	ComPort data	Read/write
90	None	ComPort status	Read/write
C2	None	Reset board	Read/Write
E0	C0000000	Control 1	Read/Write
E4	C0000001	Control 2	Read/Write
E8	C0000002	Control 3	Read/Write
EC	C0000003	Control 4	Read/Write
F0	C0000004	Status 1	Read
F4	C0000005	Control 5	Read/Write

Setting bit 4 of the Reset Board register, generates a continuous reset.

3.7 Static RAM (SRAM)

The 8M byte SRAM is composed of a pair of 1M by 32 bit wide zero bus turnaround (ZBT) synchronous static rams, making a single 1M by 64 bit SRAM. This can be accessed as D8, D16, D32 or D64 via the VME data bus. It can only be accessed in the A32 address space. The base address of this memory is set by the VME SRAM offset register, and it resides on a 8Mbyte boundary. The memory operates with a 200MHz clock so 64 bit transfers achieve 1.6G bytes/sec throughput. Smaller width transfers achieve correspondingly lower throughputs.

The DMA controllers always perform 64 bit reads and writes, while global bus reads from SRAM are always 64 bits, and converted to 2 off 32 bit transfers by the Virtex4, to maximise SRAM availability.

3.8 JTAG Debugging Logic

An external Jtag controller can be used to access the Tim sites via the front panel Jtag connector. The external controller can drive the JTAG scan chain through all TIM modules. If a module is not present then the modules SENSE signal is used to enable a switch inserted in the TDO/TDI (JTAG Data In and Data Out) scan chain to bypass that module. Two connectors are present on the front panel. One is the scan chain out, and the other is the scan chain in. The scan chain out connector is disabled when disconnected. This arrangement allows multiple boards to be debugged with a single JTAG sontroller.

The JTAG IN connector (nearest the PCB) has the following signals:

TDI, TDO, TRST, TMS, TCK, TCK_RET, EMU0, EMU1, GND, PD(+5v), RESETIN, CONFIG.

RESETIN is a board reset input, which is ORed with the VME bus reset to generate the local SMT329 board reset.

CONFIG is a bidirectional signal which indicates when high that all modules have finished configuration following a reset, and can commence normal operation.

The JTAG OUT connector (furthest from the PCB) has the following signals:

TDI, TDO, TRST, TMS, TCK, TCK_RET, EMU0, EMU1, GND, SENSE, RESETOUT, CONFIG.

RESETOUT is a buffered copy of the SMT329 board reset signal, which will reset the next SMT329.

SENSE is pulled down on the SMT329 so that if the JTAG OUT is connected to another SMT329 JTAG IN then the SENSE line is pulled high by the connection to PD(+5v). This disables the JTAG OUT bypass, so that the next SMT329 is included in the JTAG scan chain.

All outputs and inputs from and to the JTAG IN and OUT connectors are passed through buffers, except CONFIG, EMU0 and EMU1 which are global open collector signals. Both the JTAG in and out connectors are 3M 20-way, part number 10220-5212JL.

3.9 ComPort Interface

This interface provides a route by which a VME host can talk to a TIM ComPort. Both D16 and D32 accesses are allowed. The following address / register map is used:

Address	Register	Data bits	Read/Write
IO base + 80hex	ComPort Data	31..0	R/W
IO base + 84hex	ComPort Data	31..0	R/W
IO base + 90hex	ComPort Status	15..0	R

There is only one ComPort interface, and its data register is accessible at both addresses indicated in the table above.

The ComPort data register is accessible as a D16 resource by first writing the upper data bits (31 to 16) to address base + 84h and then the lower data bits to address base + 86h. This register, when read, contains the next word received from the comm port. Writing to this register causes a word to be sent to the comm port. The receive and transmit sections of this register are separate and each includes a 16 deep by 32 bit wide fifo.

The status register is accessible by the VME host as D16 at address base + 92h or in D32 at address base + 90h. The bit definition is as follows:

Bit	Definition
8	Receive fifo not empty
9	Transmit fifo not full
10	Receive fifo not empty
11	Transmit fifo not full
12	Receive fifo half full
13	Receive fifo full
14	Transmit fifo half full
15	Transmit fifo empty

The receive fifo not empty bit becomes set when a receive word is in the ComPort data receive fifo. When all the ComPort data in the receive fifo is read, this bit is reset.

When the transmit fifo not full bit is set, it indicates that the VME host can write a new word to the ComPort data register for later transmission to the comm port.

3.10 Reset Board Register

This special control register is accessed in A32 space as either D16 or D32. When accessed as D16 it uses address base + C2h, and when using D32 at address base + C0h. Only bit-4 is defined, and if this bit is set by the VME host, it causes all TIM sites, ComPort buffers, and other motherboard logic to become reset. The board remains in such a state until this bit is cleared by the VME host. This reset is the **same** bit as defined in VME control register bit-0.

4 TIM Memory Map

TIM sites 1 and 4 have access to the SRAM, general control registers, general status register and VME space. The global bus addresses used are given in the table below:

Address	Resource	Read/Write
C000 0000	Gen Control reg 1	Read/Write
C000 0001	Gen Control reg 2	Read/Write
C000 0002	Gen Control reg 3	Read/Write
C000 0003	Gen Control reg 4	Read/Write
C000 0004	Gen Status reg	Read
C100 0000 – C13F FFFF	VME bus	Read/Write
DFE0 0000 – DFFF FFFF	8M Byte Dual Port Ram	Read/Write

5 TIM ComPorts

Each TIM module has up to 6 byte-wide communications ports. Following a reset, 3 of these comm ports are in output mode, and the other 3 are in input mode. The Virtex4 also has 2 comm ports which reset to output (Ch0 & Ch1). TIM sites (1 to 4) have six numbered comm ports. Ports 0 to 2 are reset to output, and ComPorts 3 to 5 are reset to input.

6 TIM Sites

There are 4 TIM sites numbered 1 to 4. Sites 1 and 4 have the optional 80 way global connector to allow TIM access to the SRAM and VME bus.

6.1 TIM Connector Pin-Out

The global connector contains the full set of TIM global bus signals. For accesses by the TIM to the global bus, the most significant address bit, A31 is a ‘1’. This bit is not an output pin but used internally on a TIM. The global bus connector does not contain any power or ground signals.

The bottom, or secondary, connector is used only for ComPorts, power and user definable connections (UDP 7 to 12). The user-definable pins are not implemented on this motherboard. ComPorts 1, 2, 4 and 5 are on this connector.

The top, or primary, connector is used for the remaining two ComPorts (0 and 3), power, interrupts, control and JTAG. Both plus and minus 12v are supplied by the motherboard to these top connectors. The JTAG signals are derived from the external JTAG source (see JTAG section).

An external clock is supplied to all TIM sites. This clock is currently 50MHz, and MUST be used by TIMs in sites 1 and 3 if they are to perform any external accesses via their Global

TIM connector. Similarly, TIMs in sites 1 and 3 must provide both H1 and H3 clock outputs to the SMT329 if they are to perform any global bus accesses.

A power supply of +3.3 Volts is present at both TIM mounting holes. This can be connected to the TIM by using metal bolts.

Refer to the TIM-40 Module Specification from Texas Instruments for exact connector placement. Adjacent TIM sites are separated by exactly 2.6".

7 ROCKET-IO

The Virtex4 has a total of 16 Rocket-IO transceivers, 8 of which are connected to the VXS channels on the VME64 P2 connector, and the other 8 are connected to the TIM RSL ports. A cross bar switch is implemented in the Virtex4 which allows any RSL A port to be connected to VXS ports 1-4, and any RSL B port to be connected to VXS ports 5-8. In addition it can connect any Rocket-IO port to 1 of the 4 DMA channels, so that data can be streamed to or from the SRAM. The cross bar switch topology is strictly point to point, and is determined by a bit map held in the FLASH, which is only loaded into the crossbar switch following a board reset. Dynamic connectivity changes are not supported. All DMA and communications protocol control must be performed by an intelligent TIM module using the global bus. Note that 4 of the VXS transceivers are shared with Gigabit Ethernet, and this is set at board assembly, so the required option must be stated when ordering.

8 Gigabit Ethernet

The Virtex4 has 4 Gigabit Ethernet controllers which are directly connected to user defined I/O pins on row C of the VME P2 connector. This means they are available on the legacy version of the SMT329 which uses legacy 3 row VME connectors instead of the 5 row connectors used on the full version of SMT329. Each Ethernet controller has a dedicated DMA controller which can stream data to or from the SRAM at full Ethernet speed of 1G bit/sec. Note that the 4 Gigabit Ethernet transceivers are shared with VXS, and this is set at board assembly, so the required option must be stated when ordering.

9 DMA controllers

There are a total of 8 DMA channels on the SMT329. The Rocket-IO cross bar switch has 4 channels available, and each of the 4 Gigabit Ethernet transceivers has a dedicated DMA channel. All DMA channels have the same register set and control features including programmable interrupt generation. All perform 64 bit I/O to the SRAM and operate at 200MHz. An SRAM bus arbiter allocates each channel time slots on the SRAM bus on demand.

10 FLASH

The AMD/Spansion S29GL256M10TAIR1 32M byte flash is fitted. This device stores the connectivity bit maps for both the Virtex4 Rocket-IO cross bar switch and the comms port cross bar switch. It also stores the logic configuration data for each of these devices.

The Virtex4 implements 2 manual write protect board links which can selectively write protect critical sections of the flash. This is to ensure the connectivity maps can not be overwritten in an application where this function is not required.

11 Power Supplies

Connections are made to the following back plane power signals through VME connector P1: +12V, -12V, +5V. The +/-12V supplies are fed directly to the TIMs, they are not used anywhere else on the board. The +5V supply is also fed to the TIMs, and used for most of the logic, and to feed a DC-DC converter which generates +3.3V for the legacy 3 row VME connector version of SMT329. The full VME64 version of SMT329 obtains the +3.3V supply from the 160 pin 5 row P1 connector using the row D pins.

The +3.3V DC-DC controller on the legacy SMT329 is an TPS5602IDBT from Texas Instruments, which also generates 1.2V to supply the Virtex4 and Spartan3. The feedback point is taken from the +3.3V power plane. The power distribution is through a dedicated +3.3V power plane so the voltage drop here is minimal. The power plane distributes +3.3V to all 4 TIM sites through the metal TIM fixing posts. It is designed to supply 10 AMPS maximum, however this is only possible if the board receives adequate cooling. Failure to cool the board properly at high current levels could result in premature failure, and / or premature current limiting.

12 PCB Layout Details

The board conforms to the VME standard for a ‘Double Height’ board. This is:

160.0 (+0, -0.3) mm by 233.35 (+0, -0.3) mm.

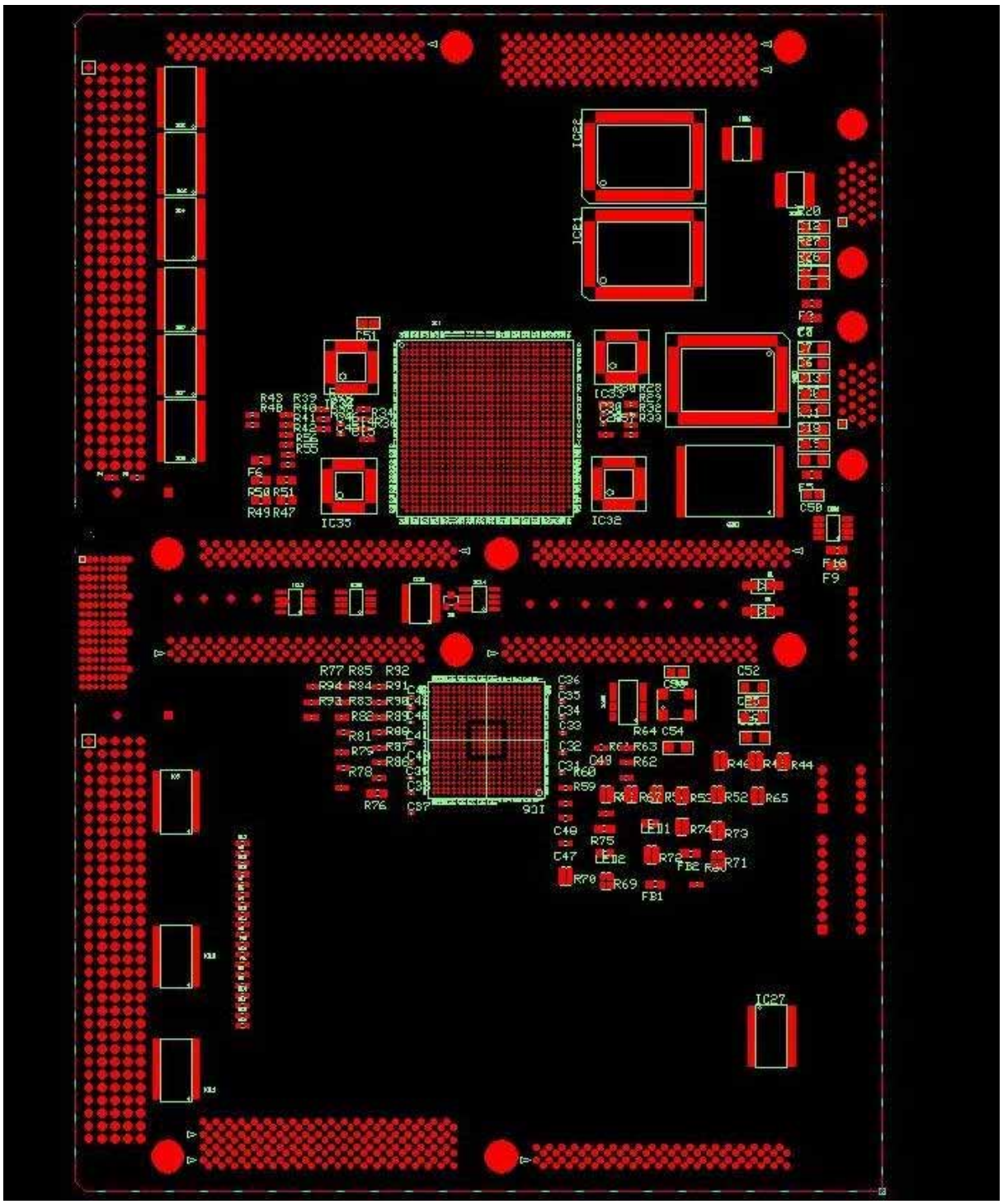
The board occupies 2 VME slots.

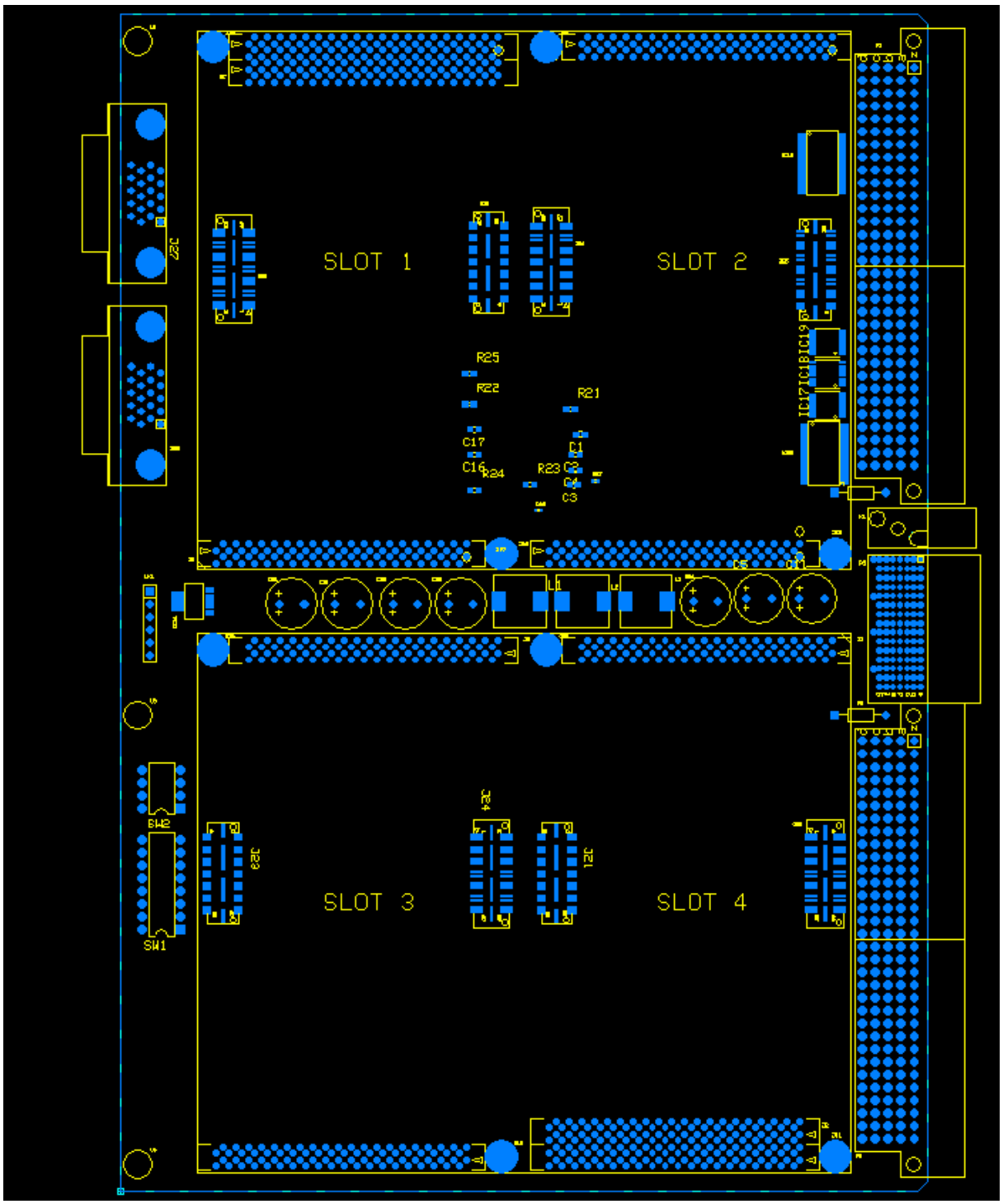
The SMT329 board layout is similar SMT328. To aid routing the top 2 TIM sites have been rotated together through 180 degrees.

The VME P0 connector present on SMT329 was not present on SMT328.

The front panel ComPort connectors on SMT328 have been removed.

The following drawings show prototype PCB components placements:


IC24
IC21
C51
IC35
IC32
C52
R64 C54
IC27


SLOT 1
SLOT 2
SLOT 3
SLOT 4
R25
R22
R21
C17
C16
R24
R23
C2
C1
C4
C3
IC17
IC18
IC19
SW2
SW1

13 Safety

This module presents no hazard to the user.

14 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.