SMT338-VP

User Manual

Revision History

Date	Comments	Engineer	Version
16/08/04	First revision	JPA	1.0
17/05/05	Corrected: purpose of Led 5 and Led 6	SM	1.1
07/06/05	Added: power consumption Added: SDRAM 63.75MB capacity	SM	1.2
1707/06	Updated DDR SDRAM description	JPA	1.3

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Precautions (Please Read this!)

SHB and RSL connectors are similar but their use is really different. Do NOT connect an SHB and an RSL connectors together with and SHB cable! This would cause irreversible damages to the modules.

In the event of a conflict between the text of this document and the user guide for SMT390-VP, SMT391-VP or SMT381-VP or any other DAQ daughter module, the text of this document DOESN'T take precedence.

Introduction

Overview

The *SMT338-VP* is a single width TIM base module that provides a communication platform between a Virtex-II Pro VP30 FPGA and the on-board 128MB Double Data Rate SDRAM memory, Rocket IOs for high speed serial connections, LVDS connections for high speed parallel connections and LVTTL connections and connectors.

The SMT338-VP can be coupled with analogue daughter boards such as SMT390, SMT391 or SMT381 for high performance DAQ applications.

The FPGA is configured at power-up via comport. The configuration process is controlled by a microprocessor MSP430.

Features

- 128MBytes of DDR SDRAM 133 MHz for sample storage.
- Two Standard Sundance comports,
- Two SHB interfaces for easy interconnection to Sundance products,
- RSL (**R**ocketIO **S**erial **L**ink) interfaces for fast transfers,
- On-board MSP430 microprocessor.

Power consumption

The SMT338-VP consumes about 2.12 Watts in idle state (FPGA not configured), and about 5.67 Watts once the FPGA is configured (bitstream for the SMT391-VP).

Related documents

SHB technical specification

Sundance help file

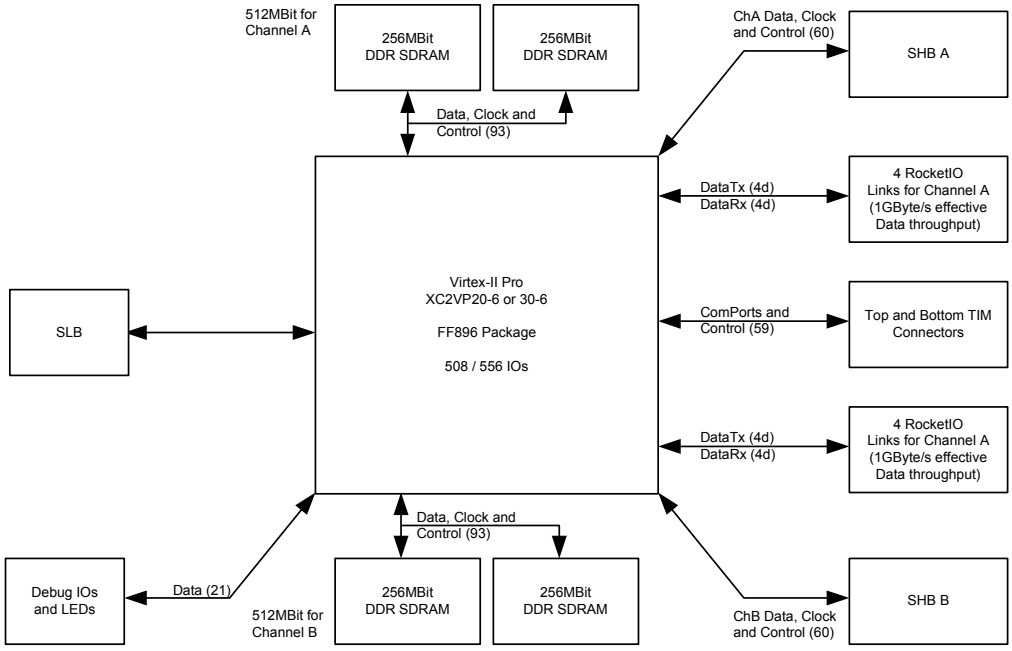
Sundance LVDS Bus (SLB) - Technical Specification

RSL Technical Specification

Architecture description

Bloc diagram

This section describes the major blocks of the SMT338-VP board.



Notes: The numbers in brackets denote the amount of FPGA IO pins requires. 'd' is used for differential pairs. 1d Will thus requre 2 IOs

FPGA

The SMT338-VP board uses a Xilinx Virtex II Pro (XC2VP20 or XC2VP30) to control the data flow between the SMT338-VP board and external devices. The FPGA is also used to implement the SHB, SLB, comport and DDR SDRAM interfaces.

The FPGA is configured via comport 3.

Memory

The SMT338-VP board contains four 166 MHz DDR SDRAM components (from Micron: MT46V16M16FN) that provide each 32 MB of storage capacity.

The DDR SDRAM is a high-speed CMOS, dynamic random-access memory.

Examples of DDR SDRAM controller are provided by Xilinx.

Micro-controller

The SMT338VP board is equipped with a micro-controller MSP430

The MSP430 implements board maintenance functions:

- Controls the power start-up sequence
- Controls the reset structure on the module
- Configures the FPGA

Sundance High Speed Bus

SMT338-VP provides two SHB connectors.

Interfaces connected to SHB connector depends on the daughter connected to SLB bus.

Please refer to the SUNDANCE SHB specification for more details.

Comport

The SMT338-*VP* provides 2 comports: 0 and 3.

ComPort 3 is used to configure and send control words to the FPGA. Comport 0 is left unused by the default firmware and is available for custom applications.

The TI comport specification provides more information about comports.

SLB

The SMT338-VP provides a SLB connector.

Interface to SLB is specific to daughter board.

Please refer to SLB specification for more details.

LED

Six LEDs are available on the board.

LED 1 is on when 5 volts is available on board.

LED 2 is on when 3.3 volts is available on board.

LED 3 and 4 are controlled by FPGA.

LED 5 is connected to MSP430. This led switches on when FPGA is configured.

LED 6 is mapped to the FPGA (pin AG6). It can be used as GPIO.

JTAG

The SMT338-VP includes JTAG connectors to access FPGA and MSP430. Both devices are in the same JTAG chain.

Connector J13 is a dedicated JTAG connector. See J13 pinout for more details.

JTAG chain is also available via some of the pins of the SLB connector. See SLB technical specification for the location of these pins. This is used when a daughter module is connected to SMT338-VP via SLB bus. In this case, J13 isn't accessible anymore and it is required to use SLB to access FPGA and MSP430 via JTAG.

Booting SMT338-VP

The booting of SMT338-VP requests two steps:

- Powering up board.
- Configuring FPGA with bitstream received from comport 3.

This is managed by MSP430.

The following diagram shows what the default micro-controller boot code does:

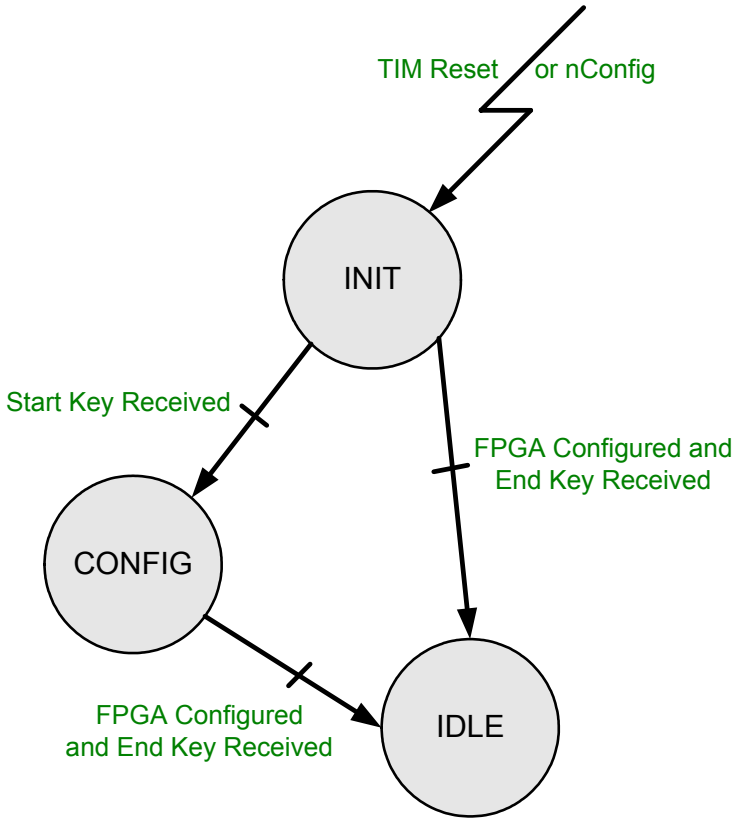


Figure 1 - Micro controller State Machine.

The SMT338-VP is reset by the TIM global reset.

There is also a TIM CONFIG signal provided on the TIM connector J4 pin 74. This provides a means of reprogramming the FPGA without having to drive the TIM Global Reset signal. CONFIG falling will reset the SMT338-VP in the same way that a TIM global Reset pulse will. Other modules in the system that are sensitive to the TIM global Reset signal will not be affected by CONFIG.

CONFIG is driven from another TIM site on the carrier board, for instance, from a DSP module running an application. (See General Firmware Description for information on the DSP TIM CONFIG signal).

After a Global Reset pulse, a DSP module drives CONFIG low and keeps it low by default.

At power-up or on a TIM Reset or on a nConfig line going low, the state machine goes into an *INIT State*.

From there, it has two choices depending on the state of the FPGA (configured i.e. DONE pin high or un-programmed i.e. DONE Pin Low). To reconfigure the FPGA, simply send a Start Key followed by the bitstream and then and End Key. To re-start the FPGA with the current bitstream loaded, simply send a End Key.

Start Key = 0xBCBCBCBC and End Key = 0xBCBCBC00.

A TIM Reset can be issued to reconfigure the FPGA at anytime, but may reset other modules as well. In the case of reconfiguring a particular module, the nConfig line is used.

The SMT6500 software package provides a library of functions to configure the FPGA via comport 3.

Getting started with SMT338-VP

This section gives basic guidelines to start with SMT338-VP.

The example shown below is for an *SMT8090_374* system, which is a *SMT374* and a *SMT390-VP* on an *SMT310Q* carrier board.

The SMT390-VP is a combination of SMT338-VP and a SMT390.

The following diagram shows both boards. The *SMT390* has got 4 holes, as well as the *SMT338-VP*, the usual two TIM mounting holes to provide the module with 3.3 Volts and two extra holes, smaller.

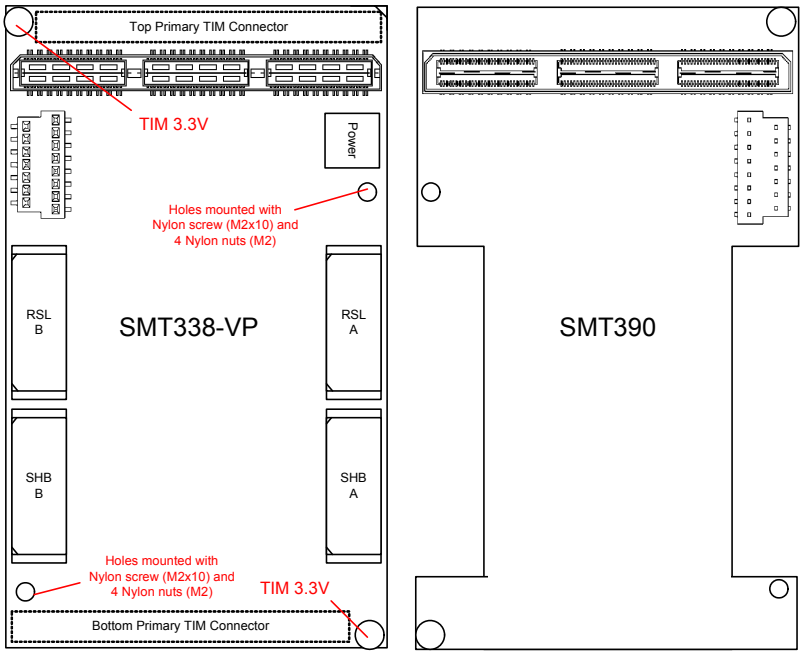


Figure 2 - SMT338-VP to SMT390 Interconnections.

Here is what is required to mount *SMT338-VP*+SMT*390* on the *SMT310Q*:

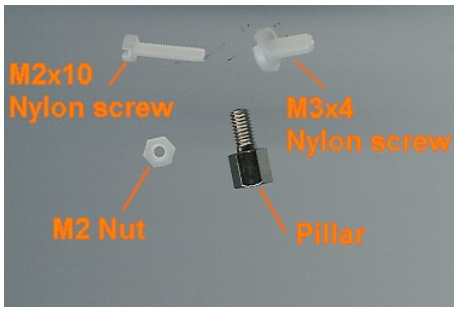
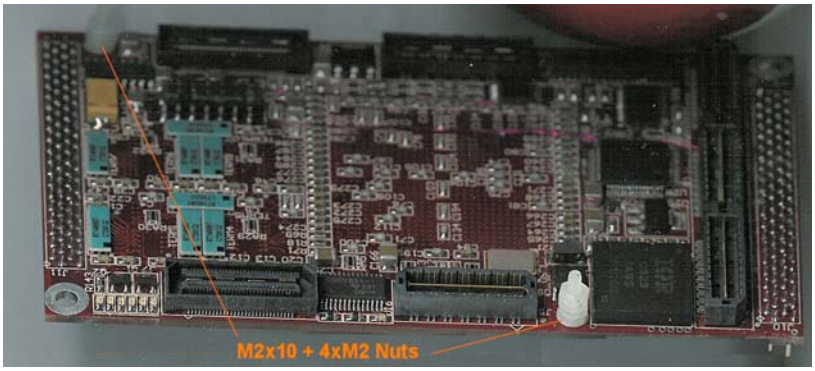


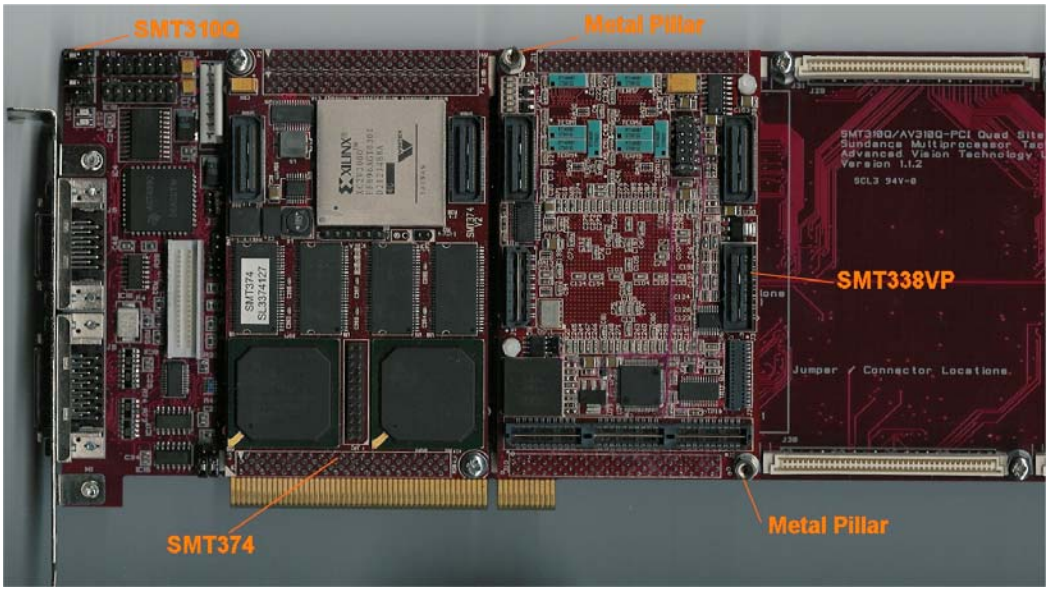
Figure 3 – Fixings

a – First, fit two Nylon screws (M2x10), pointing out (the head of the screws on bottom side).

b – Then fit four M2 nuts on each screw.

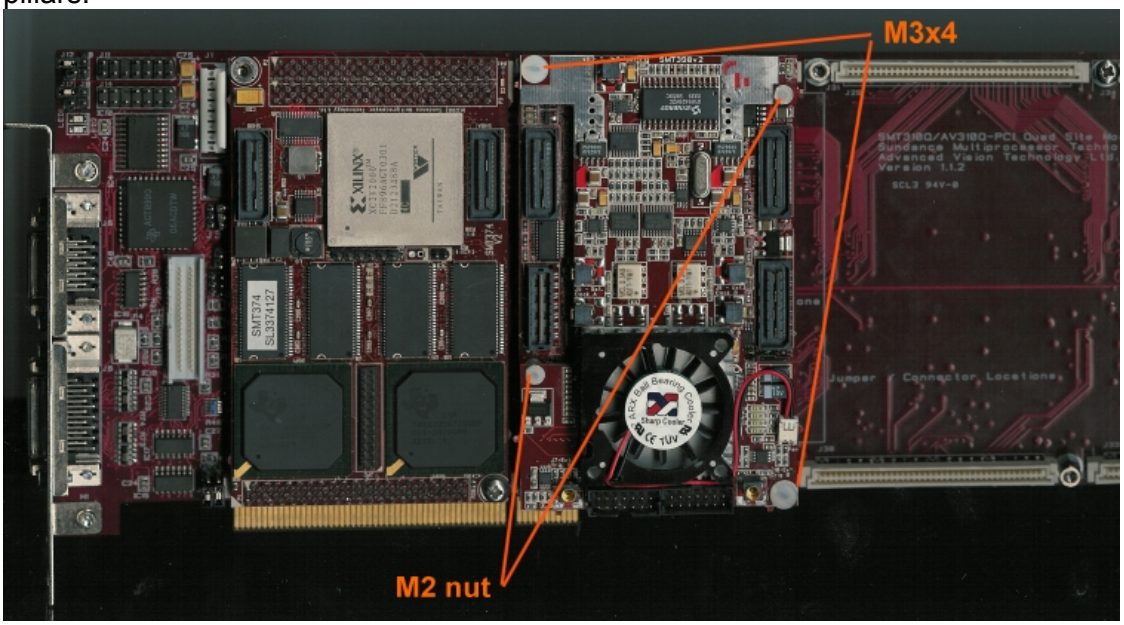


c – Place the *SMT338-VP* on the second site (*SMT374* already on first site) on the *SMT310Q* and fit two metal pillars (3.3 Volts).



d – Place the *SMT390* on top of the *SMT338-VP*. Make sure that both modules fit firmly.

e – Fit two M2 nuts on the Nylon screws and two M3x4 screws in the 3.3V pillars.



Functional description

This section describes in detail the implementation of the board.

Memory banks

Memory is organised in two independent banks.

Both banks can be accessed at the same time.

The following diagram shows how the DDR SDRAM components are organized within a memory bank:

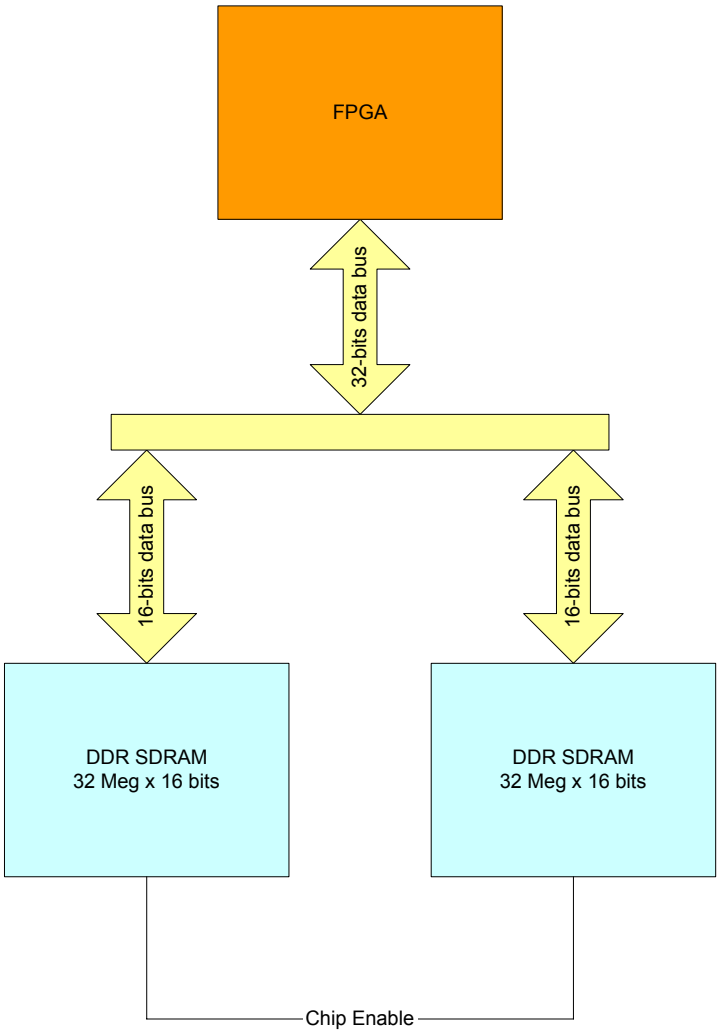


Figure 4: DDR SDRAM components bank organization

One bank is made from two 32M x 16-bits DDR SDRAM components (MT46V32M16FN), each of them having a 16-bit data bus. Memory components are accessed in pairs.

Oscillator

A 125 MHz low jitter oscillator is connected to the FPGA.

Connectors location

The following figure shows the location of connectors on SMT338-VP board.

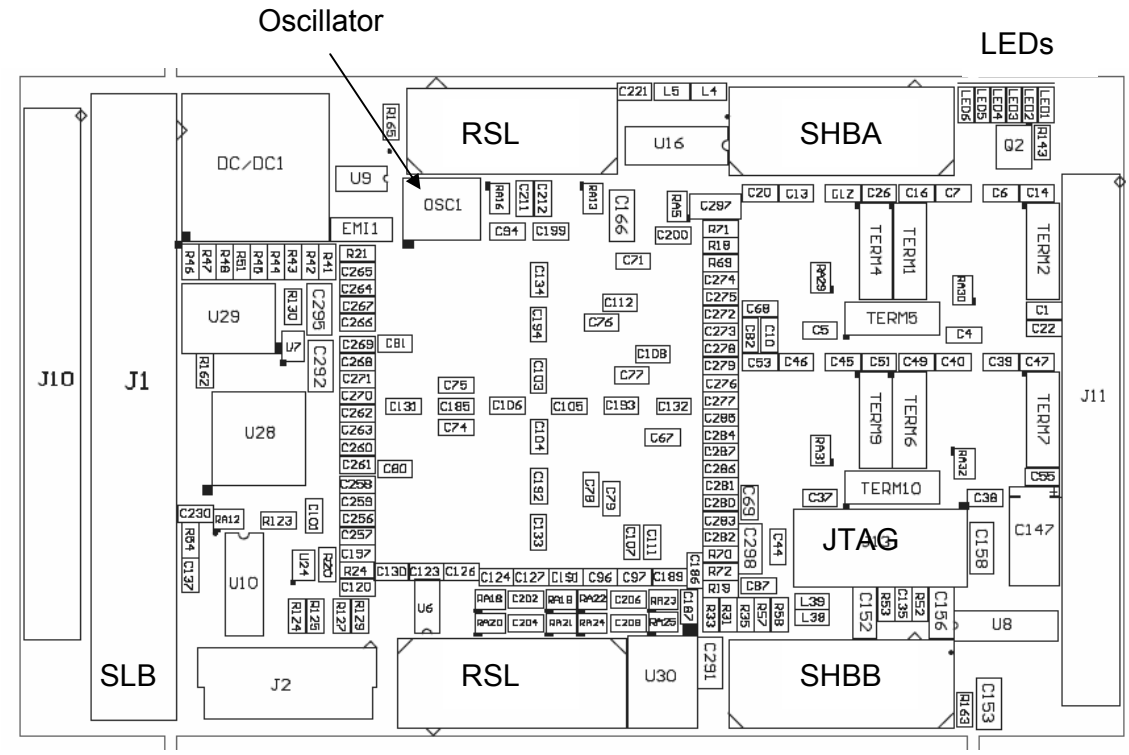


Figure 5: view of the top of SMT338-VP

FPGA pinout

FPGA pinout is gathered in a Xilinx User Constraint File (ucf).

Naming convention is described below for SHB and SLB. Other signals are directly commented in the UCF file itself.

SHB Pinout (LVTTL only)

The following provides naming convention for SHB signals.

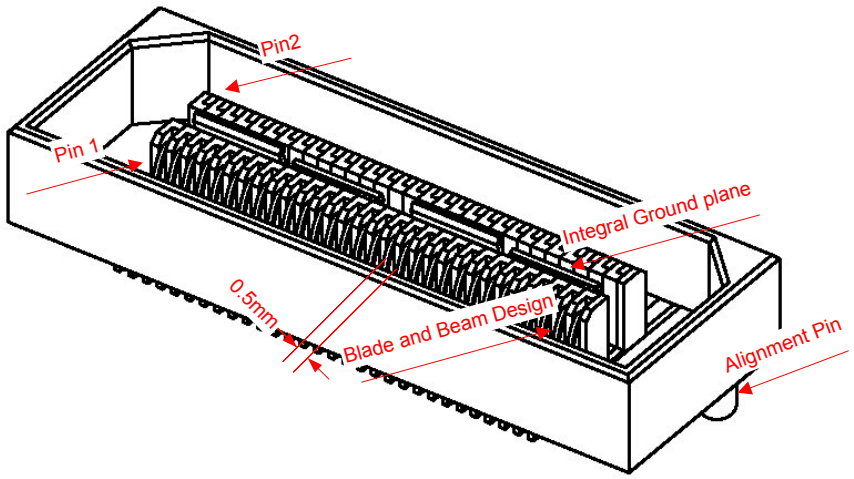


Figure 6: Top view QSH 30

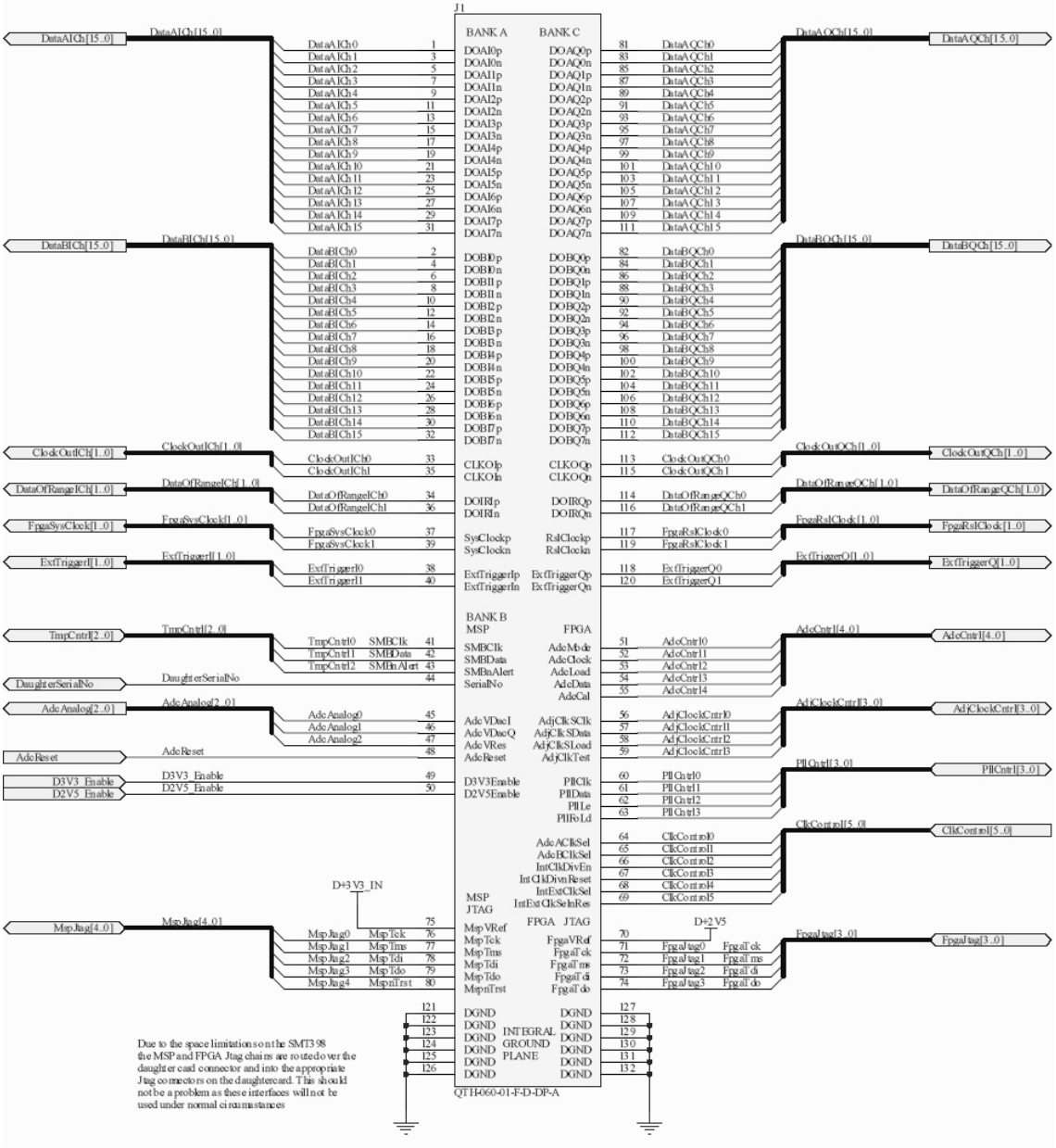
	UCF signal name	Hw	QSH Pin number	QSH Pin number		UCF signal name	Hw
Hw0	Shb?Hw0Clock	SHBxCLK0	1	2	Hw0	Shb?Hw0Data	SHBxD0(0)
	Shb?Hw0Data	SHBxD0(1)	3	4		Shb?Hw0Data	SHBxD0(2)
	Shb?Hw0Data	SHBxD0(3)	5	6		Shb?Hw0Data	SHBxD0(4)
	Shb?Hw0Data	SHBxD0(5)	7	8		Shb?Hw0Data	SHBxD0(6)
	Shb?Hw0Data	SHBxD0(7)	9	10		Shb?Hw0Data	SHBxD0(8)
	Shb?Hw0Data	SHBxD0(9)	11	12		Shb?Hw0Data	SHBxD0(10)
	Shb?Hw0Data	SHBxD0(11)	13	14		Shb?Hw0Data	SHBxD0(12)
	Shb?Hw0Data	SHBxD0(13)	15	16		Shb?Hw0Data	SHBxD0(14)
	Shb?Hw0Data	SHBxD0(15)	17	18		Shb?Hw0Control(0)	SHBxUSER0(16)
	Shb?Hw0Control(1)	SHBxUSER0(17)	19	20		Shb?Hw0Control(2)	SHBxUSER0(18)
	Shb?Hw0Control(3)	SHBxUSER0(19)	21	22		Shb?Hw0Control(4)	SHBxWEN1
	Shb?Hw0Control(5)	SHBxREQ1	23	24		Shb?Hw0Control(6)	SHBxACK1
	Shb?FpgaIo(0)	SHBxUSER1(23)	25	26		Shb?FpgaIo(1)	SHBxUSER1(24)
	Shb?FpgaIo(2)	SHBxUSER1(25)	27	28		Shb?FpgaIo(3)	SHBxUSER1(26)
	Shb?FpgaIo(4)	SHBxUSER1(27)	29	30		Shb?FpgaIo(5)	SHBxUSER1(28)
	Shb?FpgaIo(6)	SHBxUSER1(29)	31	32		Shb?FpgaIo(7)	SHBxUSER1(30)
	Shb?FpgaIo(8)	SHBxUSER1(31)	33	34		Shb?FpgaIo(9)	SHBxUSER1(32)
	Shb?FpgaIo(10)	SHBxUSER1(33)	35	36		Shb?FpgaIo(11)	SHBxUSER1(34)
Hw1	Shb?Hw1Clock	SHBxCLK3	37	38	Hw1	Shb?Hw1Data	SHBxD1(0)
	Shb?Hw1Data	SHBxD1(1)	39	40		Shb?Hw1Data	SHBxD1(2)
	Shb?Hw1Data	SHBxD1(3)	41	42		Shb?Hw1Data	SHBxD1(4)
	Shb?Hw1Data	SHBxD1(5)	43	44		Shb?Hw1Data	SHBxD1(6)
	Shb?Hw1Data	SHBxD1(7)	45	46		Shb?Hw1Data	SHBxD1(8)
	Shb?Hw1Data	SHBxD1(9)	47	48		Shb?Hw1Data	SHBxD1(10)
	Shb?Hw1Data	SHBxD1(11)	49	50		Shb?Hw1Data	SHBxD1(12)
	Shb?Hw1Data	SHBxD1(13)	51	52		Shb?Hw1Data	SHBxD1(14)
	Shb?Hw1Data	SHBxD1(15)	53	54		Shb?Hw1Control(0)	SHBxUSER2(52)
	Shb?Hw1Control(1)	SHBxUSER0(17)	55	56		Shb?Hw1Control(2)	SHBxUSER2(54)
	Shb?Hw1Control(3)	SHBxUSER0(19)	57	58		Shb?Hw1Control(4)	SHBxWEN4
	Shb?Hw1Control(5)	SHBxREQ4	59	60		Shb?Hw1Control(6)	SHBxACK4

Table 1: SHB interfaces table.

16-bit interface

SLB pinout

The following diagram shows the SLB connector signals connected to the FPGA. These names match with names available in UCF file.



JTAG connector

The following 2 diagrams show connector J13 pinout.

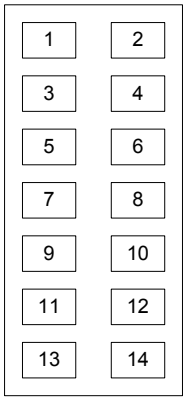


Figure 7: J13 footprint

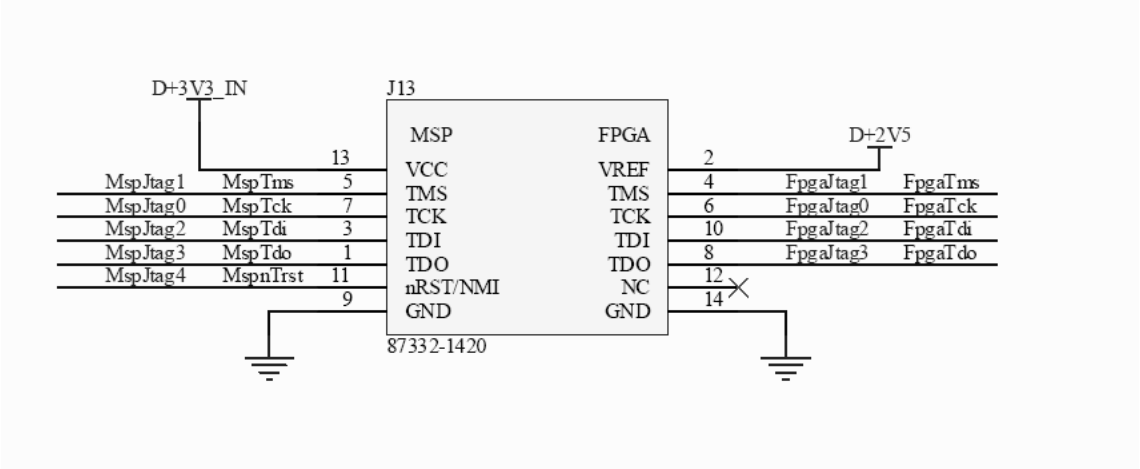


Figure 8: JTAG connector J13 pinout

RSL

Follow is the RSL pinout.

RSL pin name refers to RSL pin-outs documentation.

RSL type B:

RSL pin name	FPGA pin number
TxLink0p	A26
TxLink0n	A27
RxLink0p	A25
RxLink0n	A24
TxLink1p	A19
TxLink1n	A20
RxLink1p	A18
RxLink1n	A17
TxLink2p	A13
TxLink2n	A14
RxLink2p	A12
RxLink2n	A11
TxLink3p	A6
TxLink3n	A7
RxLink3p	A5
RxLink3n	A4

RSL type A:

RSL pin name	FPGA pin number
TxLink0p	AK6
TxLink0n	AK7
RxLink0p	AK5
RxLink0n	AK4
TxLink1p	AK13
TxLink1n	AK14
RxLink1p	AK12
RxLink1n	AK11
TxLink2p	AK19
TxLink2n	AK20
RxLink2p	AK18
RxLink2n	AK17
TxLink3p	AK26
TxLink3n	AK27
RxLink3p	AK25
RxLink3n	AK24