Sundance Multiprocessor Technology Limited **Design Specification**	Form : QCF51 Dated : 20 December 2001 Revision : 5.1 Approved : Mark Ainsworth

Unit / Module Name:	Dual 125-MSPS ADC / 500-MSPS DAC module
Unit / Module Number:	SMT350
Used On:	SMT368 and other Virtex-4 SLB base modules
Document Issue:	1.3
Date:	08/06/2005

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Approvals		Date
Managing Director		
Software Manager		
Design Engineer		

Revision History

	Changes Made	Issue	Initials
02/02/05	Original Document based on SMT370A specifications.	1.0	PSR
18/02/05	Detailed description of DAC and ADC input stages added.	1.1	PSR
04/03/05	Change of Clock Structure: one common external clock for ADCs and DAC instead of 2 separate external clocks.	1.2	PSR
08/06/05	Clock synthesizer (CDC7005) changed for later chip (CDCM7005). Correction added for targeting SMT368 base module only. Register re-definition.	1.3	PSR

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1 Introduction

1.1 Overview

The *SMT350* is a single width expansion TIM that plugs onto the SLB base module SMT368 (Virtex-4 FPGA) and incorporates 2 Texas Instrument Analog-to-Digital Converters (ADS5500) and a Texas Instrument dual-channel Digital-to-Analog Converter (DAC5686). The *SMT350* implements a comprehensive clock circuitry based on a CDCM7005 chip that allows synchronisation among the converters and cascading modules for multiple receiver or transmitter systems as well as the use of an external reference clock. It provides a complete conversion solution and stands as a platform that can be part of a transmit/receive base station.

ADCs are 14-bit and can sample at up to 125 MHz. The DAC has a resolution of 16 bits and is able to update outputs at up to 500MHz. All converters are 3.3-Volt.

The Xilinx FPGA (Virtex-4) on the base module is responsible for handling data going/coming to/from one of the following destination/source: TI converters, **C**omport (TIM-40 standard), **S**undance **H**igh-speed **B**us (SHB). These interfaces are compatible with a wide range of Sundance's modules.

The memory on base module can be divided into two 16-bit wide independent blocks for storing incoming and/or outgoing samples.

Converter configuration, sampling and transferring modes are set via internal control registers stored inside the FPGA and accessible via Comport.

1.2 Module features

The main features of the *SMT350* are listed below:

- Dual 14-bit 125MSPS ADC (ADS5500),
- Dual channel 16-bit 500MSPS DAC (DAC5686),
- On-board low-jitter clock generation (CDCM7005),
- One external clocks, two external triggers and one reference clock via MMCX connector,
- One SLB connector to link *SMT350* and *SMT368*,
- Synchronisation signals,
- All Analogue inputs/outputs are 50-Ohm terminated.
- Temperature sensors.

1.3 Possible applications

The *SMT350* can be used for the following application (this non-exhaustive list should be taken as an example):

- High Intermediate-Frequency (IF) sampling architecture,
- Cellular base station such as CDMA and TDMA,
- Baseband I&Q systems,
- Wireless communication systems,
- Communication instrumentation,
- ...

1.4 Related Documents

ADS5500 Datasheet – Texas Instrument:
http://focus.ti.com/docs/prod/folders/print/ads5500.html
DAC5686 Datasheet – Texas Instrument:
http://focus.ti.com/docs/prod/folders/print/dac5686.html
CDCM7005 Datasheet – Texas Instrument:
http://focus.ti.com/docs/prod/folders/print/cdcm7005.html
Sundance **H**igh-speed **B**us (*SHB*) specifications – Sundance.
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification.pdf
Sundance **L**VDS **B**us (SLB) specifications – Sundance.
http://www.sundance.com/docs/SLB%20-%20Technical%20Specifications.pdf
TIM specifications.
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf
Xilinx Virtex-4 FPGA.
http://direct.xilinx.com/bvdocs/publications/ds031.pdf
MMCX Connectors – Hubert Suhner.
MMCX Connectors
Surface Mount MMCX connector
Sundance Multiprocessor Technology Ltd.
SMT368

2 Functional Description

In this part, we will see the general block diagram and some comments on some the *SMT350* entities.

2.1 Block Diagram

The following diagram describes the architecture of the *SMT350*, coupled – as an example – with an *SMT368* to show how mezzanine and base modules are connected together:

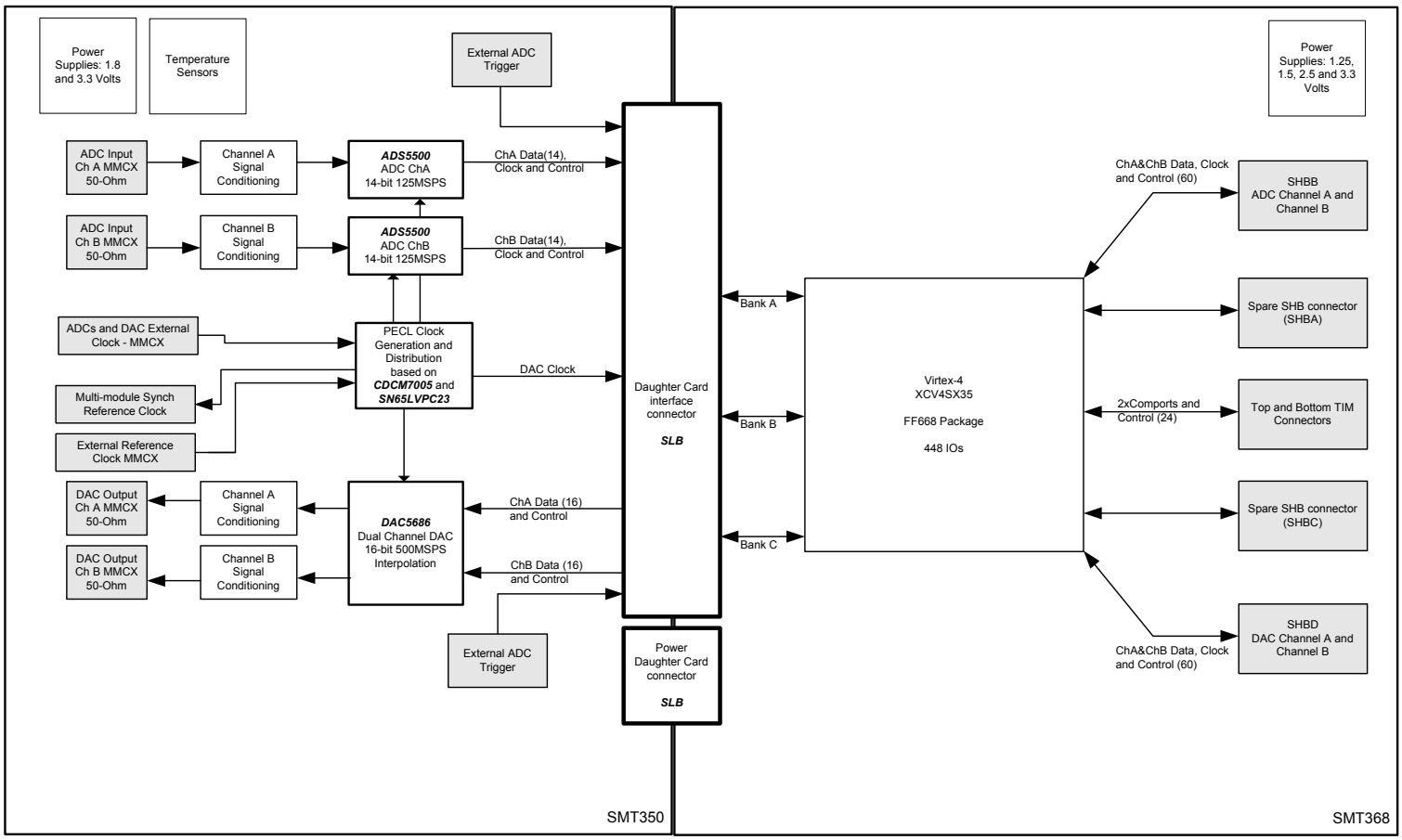


Figure 1 - Block Diagram.

2.2 Module Description

The module is built around two TI ADS5500 14-bit sampling analog-to-digital converters and one TI DAC5686 dual 16-bit digital-to-analog converter.

ADCs: Analog data enters the module via two MMCX connectors, one for each channel. Both signals are then conditioned (AC coupling; DC optional) before being digitized. Both ADCs gets their own sampling clock, which can be either on-board generated or from an external reference or an external clock, common to ADCs and DAC (MMCX connector). Digital samples travel to the FPGA on the base module via the inter-module connector (*SLB* – **S**undance **L**VDS **B**us, used in this case as 'single-ended').

DAC: Digital samples are routed from the FPGA to the DAC via the inter-module connector. Internal interpolation scheme allows reaching 500 Mega Samples per Second. The DAC

shows other modes such as Dual DAC, Single side-band, Quadrature or up conversion. Both outputs are AC-coupled. By default they are single-ended but can optionally be differential.#

Clock generator and distribution: All samplings clocks are generated by the same chip. It allows having them all synchronized to a single reference clock.

Multi-module Synchronization: There are two types of synchronization available on the *SMT350*. The first one is frequency synchronization, by passing the external reference clock to an other module. It first goes through a 0-delay buffer and is then output. The second type is register synchronization between DACs. It is achieved by the way of an extra link between several modules to synchronize DAC internal registers (DAC signal PHSTR passed from one module to the other and driven by the master FPGA).

Inter-module Connector: it is made of a power (33 pins) and data connectors (120 pins). It is called **S**undance **L**VDS **B**us. Please refer to the SLB specifications for more details. In the case of the SMT350, the SLB is used as 'single-ended'.

A global reset signal is mapped to the FPGA from the bottom TIM connector.

External Clock signals, used to generate Sampling clocks. There is one external clock, common to ADCs and DAC When used, the CDC7005 is used as a clock multiplexer. Also available, an external reference clock that can be passed to an other SMT350 module with '0-delay'. This external Reference must be an entire multiple of the VCXO frequency in order for the CDC7005 to lock.

External Trigger: passed directly to base module. There are two, one for the ADCs and one for the DAC.

Temperature Sensor: available for constant monitoring.

2.3 ADC Channels.

2.3.1 ADC Main Characteristics.

The main characteristics of the *SMT350* ADCs are gathered into the following table.

Analogue Inputs	
Input voltage range	1 Vp-p – Full scale - AC coupled
Impedance	50Ω - terminated to ground – single-ended
Bandwidth	ADC bandwidth: 750 MHz.
External Reference Input	
Input Voltage Level	0 – 3.3 Volts.
Frequency Range	24 – 200 MHz.
External Reference Output	
Output Voltage Level	0 – 3.3 Volts
External Sampling Clock Input	
Format	Single-ended or differential (3.3V PECL).
Frequency range	10-125 MHz
External Trigger Inputs	

Format	Single-ended or differential (3.3 V PECL).
Frequency range	62.5 MHz maximum
***ADCs* Output**	
Output Data Width	14-Bits
Data Format	2's Compliment or offset binary (Changeable via control register)
SFDR	82dBs maximum (manufacturer)
SNR	70dBs maximum (manufacturer)
Minimum Sampling Clock	10 MHz (ADC DLL off)
Maximum Sampling Frequency	125 MHz (ADC DLL on)

Figure 2 - Main features.

2.3.2 ADC Input Stage.

Each ADC Analogue input is AC-coupled via and RF transformer. Both sides of the transformers are balanced so the input is 50-Ohm single-ended.

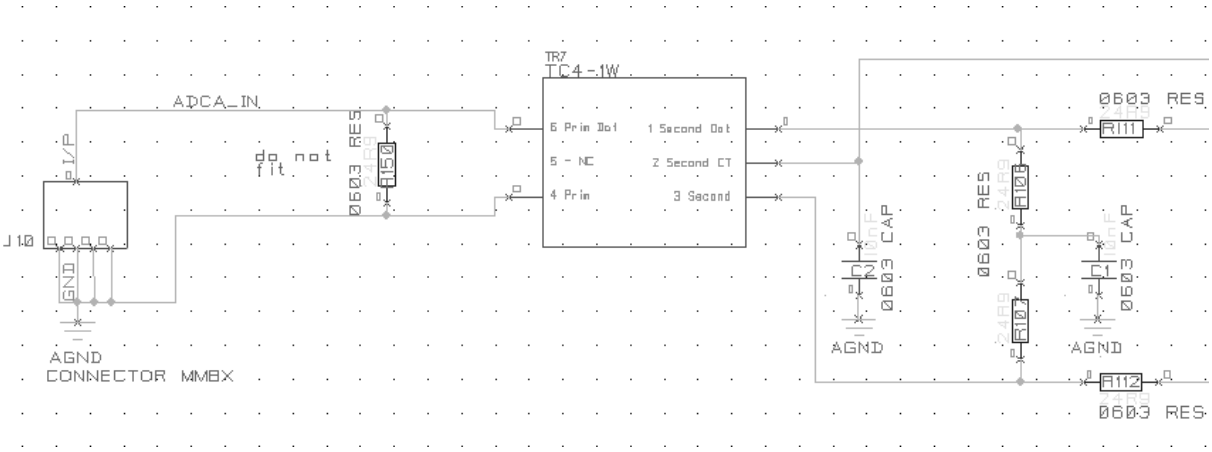


Figure 3 - ADC Input Stage.

2.4 Dual-Channel DAC.

2.4.1 DAC Main characteristics.

The main characteristics of the *SMT350* DAC are gathered into the following table.

Analogue Outputs	
Input voltage range	1 Vp-p – Full scale - AC coupled
Impedance	50Ω - terminated to ground – single ended
Bandwidth	TBD
External Reference Input	

Input Voltage Level	0 – 3.3 Volts.
Frequency Range	24 – 200 MHz.
External Reference Output	
Output Voltage Level	0 – 3.3 Volts
External sampling clock inputs	
Format	Single-ended or differential (3.3V PECL).
Frequency range	1-160 MHz
External Trigger Inputs	
Format	Single-ended or differential (3.3 V PECL).
Frequency range	80 MHz maximum
DAC Input	
Output Data Width per channel	16-Bits
Data Format	2's Compliment or offset binary (Changeable via control register)
SFDR	89dBs maximum (manufacturer)
SNR	80dBs maximum (manufacturer)
Maximum input data rate	160 MSPS
Maximum Sampling rate	500 MSPS

2.4.2 DAC output stage.

The following piece of schematics shows how the DAC outputs are coupled. The DAC5686 generates differential output signals that are fed into an RF transformer (Ohm ratio 4), that makes both DAC channels AC coupled. 100-Ohm resistors to Vcc on the primary stage of the transformer allow balancing the secondary stage to 50 Ohm single-ended.

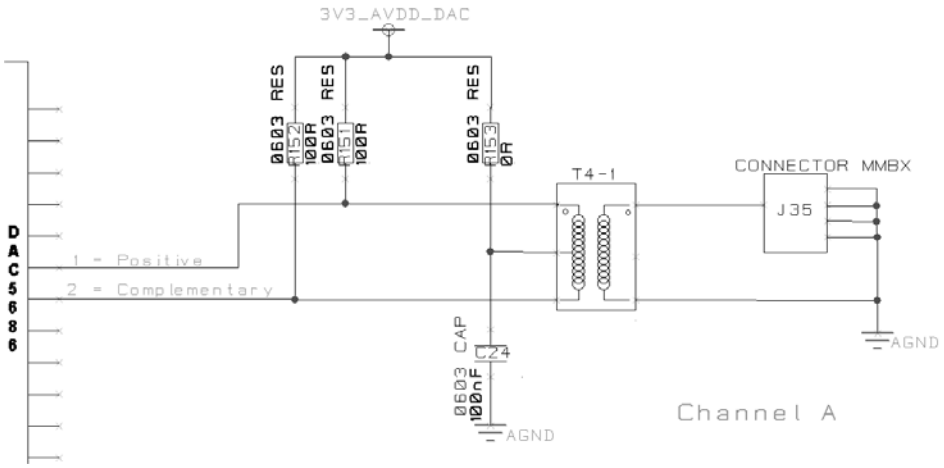


Figure 4 - DAC Output Stage.

2.5 Clock Structure

There is one integrated clock generator on the module (CDCM7005 – Texas instrument). The user can either use this clock (on-board) or provide the module with an external clock (input via MMCX connector).

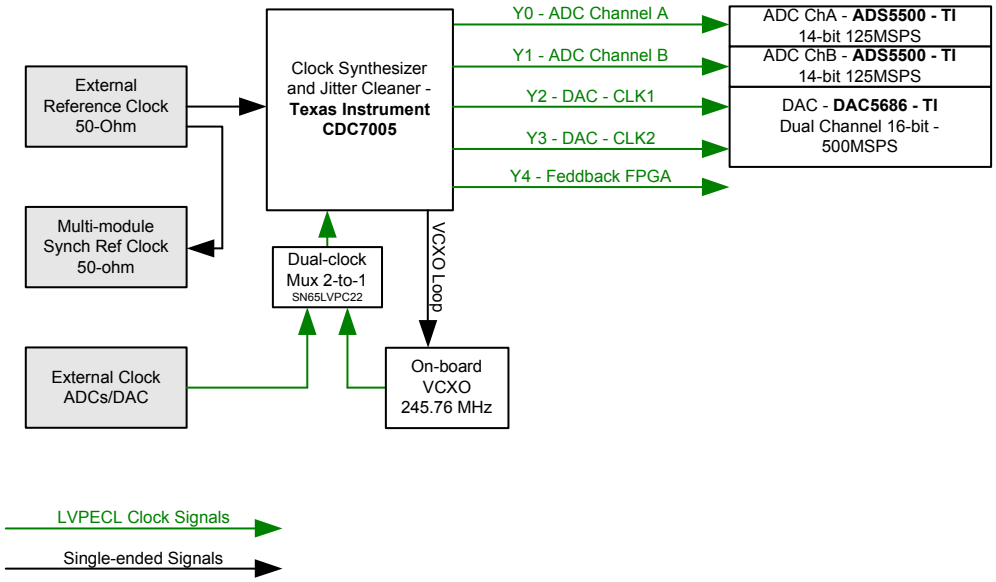


Figure 5 - Clock Structure.

ADCs can both receive the same clock or the integer multiple of it (x2, x3, x4, x6, x8 or x16), the maximum being 125MHz for each ADC. This clock can be coming from the on-board ADC crystal or from an external source.

The DAC can receive the DAC on-board (from DAC on-board crystal) or a DAC external or even the ADC clock. In the last case, ADCs and DAC can be all synchronised on the same frequency or on integer multiple (x2, x3, x4, x6, x8 or x16).

An extra connector outputs the reference clock for multiple-module systems.

Below is shown how the external clock is fed to the system. By default it is single-ended and AC-coupled before being converted into LVPECL format. The option of having a differential external clock is still possible on the hardware by the way of fitting or not some of the components.

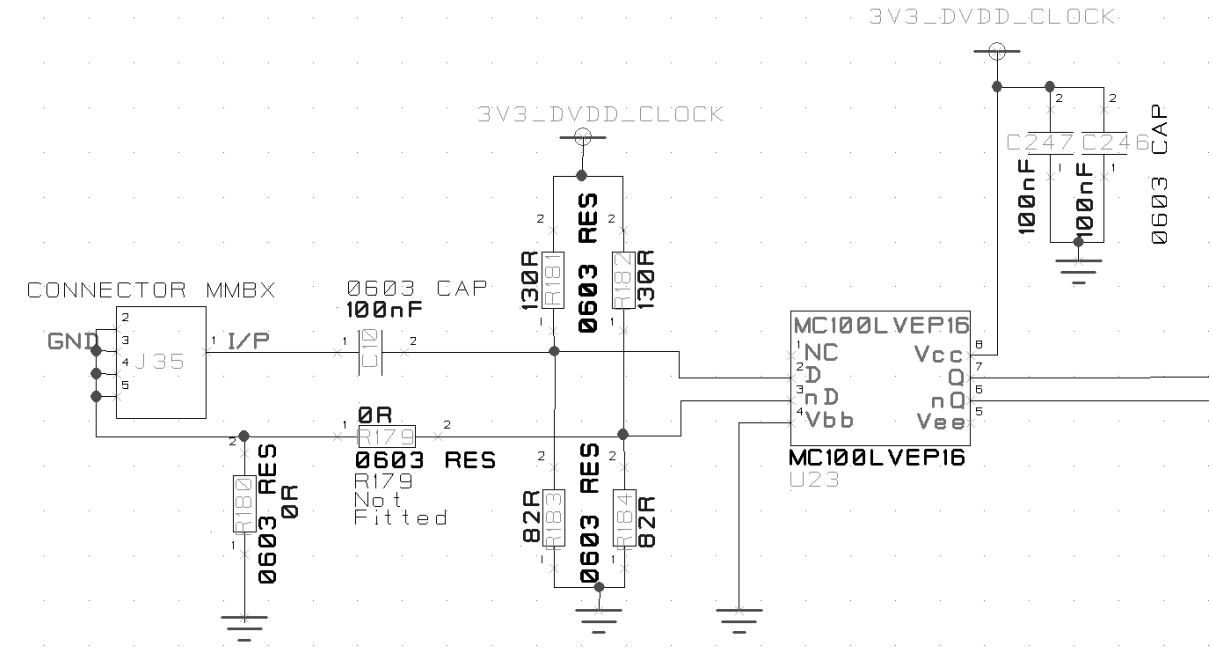


Figure 6 - External Clock.

2.6 Power Supply and Reset Structure

The *SMT350* gets two power sources from the base module: 3.3 and 5 Volts. Linear regulators are used to provide a clean and stable voltage supply to the analog converters.

2.7 Green LEDs.

There are some LEDs on the Daughter Module. Three are dedicated for the power supplies (3.3Volt, 5V ADC Channel A and ADC Channel B). Green LEDs being ON meaning that the supply is under power.

2.8 Mezzanine module Interface

The daughter module interface is made up of two connectors (data and power). The first one is a 0.5mm-pitch differential Samtec connector. This connector is for transferring data such as ADC or DAC samples to and from the FPGA on the main module. The second one is a 1mm-pitch Samtec header type connector. This connector is for providing power to the daughter-card.

Sundance defines these two connectors as the **S**undance **L**VDS **B**us (***SLB***). It has originally been made for data transfers using LVDS format but can also be used with single-ended lines, which is the case for the *SMT350*. To know more about the SLB, please refer to the SLB specifications.

The figure underneath illustrates this configuration. The bottom view of the daughter card is shown on the right. This view must the mirrored to understand how it connects to the main module.

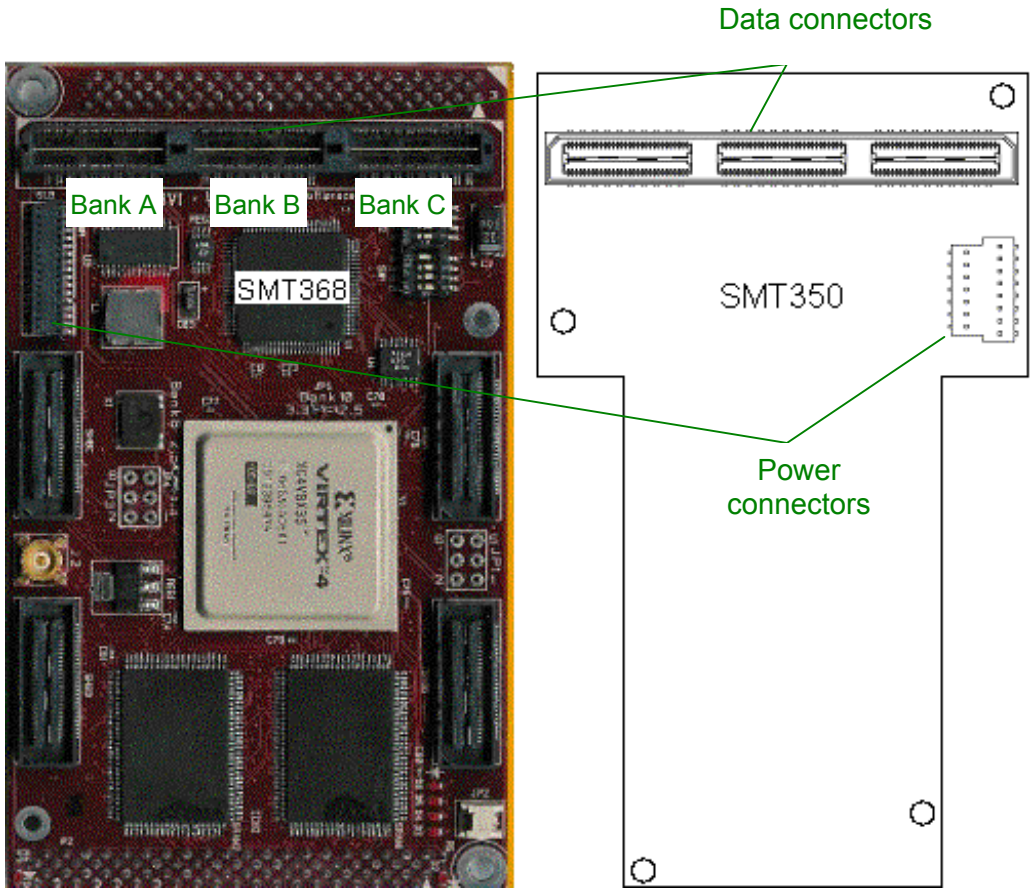


Figure 7 – Mezzanine module Connector Interface (SLB data and power connectors).

The female differential connector is located on the base module. The Samtec Part Number for this connector is QTH-060-01-F-D-DP-A.

The female power connector is located on the base module. The Samtec Part Number for this connector is BKS-133-03-F-V-A

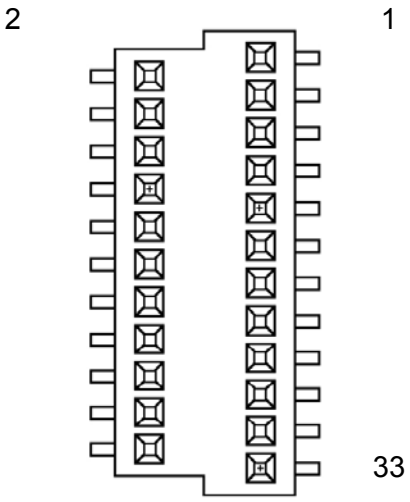
The male differential connector is located on the mezzanine card. The Samtec Part Number for this connector is QSH-060-01-F-D-DP-A

The male power connector is located on the mezzanine card. The Samtec Part Number for this connector is BKT-133-03-F-V-A

The mated height between the main module and the daughter card is 5 mm.

Some JTAG Lines are also mapped onto this connector to be used in case the Daughter module would have a TI Processor. They would allow debugging and programming via JTAG.

The following table shows the pin assignment on the power connector:

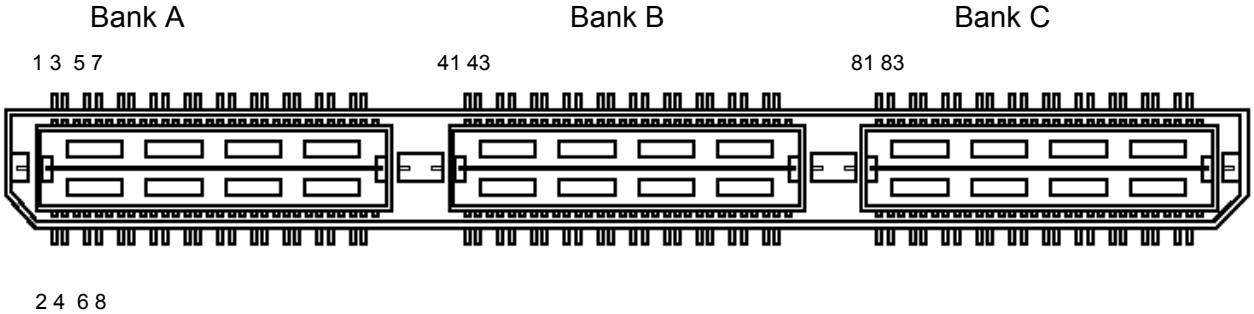


Pin Number	Pin Name	Description of Signal
1	D+3V3	Digital 3.3 Volts
2	DGND	Digital Ground
3	D+3V3	Digital 3.3 Volts
4	DGND	Digital Ground
5	D+3V3	Digital 3.3 Volts
6	DGND	Digital Ground
7	D+3V3	Digital 3.3 Volts
8	DGND	Digital Ground
9	D+5V0	Digital 5.0 Volts
10	DGND	Digital Ground
11	D+5V0	Digital 5.0 Volts
12	DGND	Digital Ground
13	D+5V0	Digital 5.0 Volts
14	DGND	Digital Ground
15	D+5V0	Digital 5.0 Volts
16	DGND	Digital Ground
17	D+12V0	Digital +12.0 Volts – not used on the SMT350
18	DGND	Digital Ground
19	D+12V0	Digital +12.0 Volts – not used on the SMT350
20	DGND	Digital Ground
21	D-12V0	Digital –12.0 Volts – not used on the SMT350
22	DGND	Digital Ground
23	D-12V0	Digital –12.0 Volts – not used on the SM350
24	DGND	Digital Ground
25	DGND	Digital Ground
26	EMU0	Emulation Control 0 – not used on SMT350
27	EMU1	Emulation Control 1 – not used on SMT350
28	TMS	JTAG Mode Control – not used on SMT350

29	nTRST	JTAG Reset – not used on SMT350
30	TCK	JTAG Test Clock – not used on SMT350
31	TDI	JTAG Test Input – not used on SMT350
32	TDO	JTAG Test Output – not used on SMT350
33	DGND	Digital Ground

Figure 8 – Mezzanine Module Interface Power Connector and Pinout.

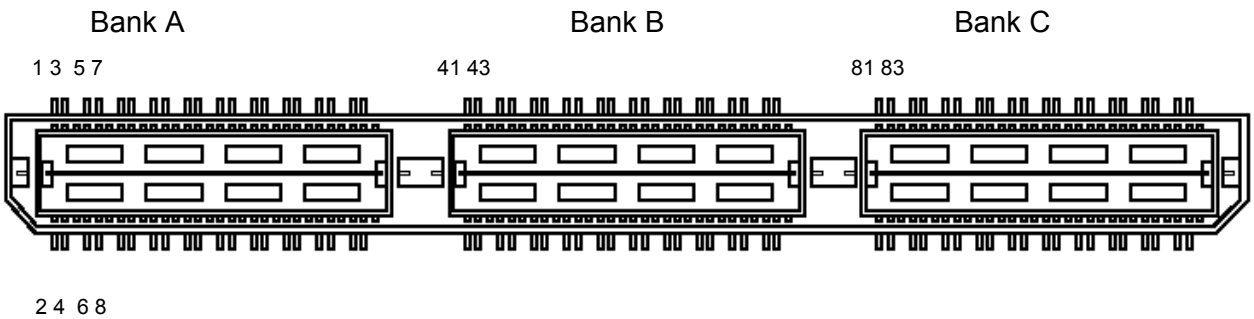
The following few pages describes the signals on the data connector between the main module and the daughter card. Bank A on the connector is used for the ADC Channels A and B. Bank C is used for the DAC channels A and B. Bank B is used for system clock and trigger signals, ADC/DAC/Clock control signal.



Bank A (ADCs)

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
1	DOAI0p	Data Out 0, Channel A.	2	DOBI0p	Data Out 1, Channel A.
3	DOAI0n	Data Out 2, Channel A.	4	DOBI0n	Data Out 3, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
5	DOAI1p	Data Out 4, Channel A.	6	DOBI1p	Data Out 5, Channel A.
7	DOAI1n	Data Out 6, Channel A.	8	DOBI1n	Data Out 7, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
9	DOAI2p	Data Out 8, Channel A.	10	DOBI2p	Data Out 9, Channel A.
11	DOAI2n	Data Out 10, Channel A.	12	DOBI2n	Data Out 11, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
13	DOAI3p	Data Out 12, Channel A.	14	DOBI3p	Data Out 13, Channel A.
15	DOAI3n	Over Range, Channel A.	16	DOBI3n	Data Out 0, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
17	DOAI4p	Data Out 1, Channel B.	18	DOBI4p	Data Out 2, Channel B.
19	DOAI4n	Data Out 3, Channel B.	20	DOBI4n	Data Out 4, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
21	DOAI5p	Data Out 5, Channel B.	22	DOBI5p	Data Out 6, Channel B.
23	DOAI5n	Data Out 7, Channel B.	24	DOBI5n	Data Out 8, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
25	DOAI6p	Data Out 9, Channel B.	26	DOBI6p	Data Out 10, Channel B.
27	DOAI6n	Data Out 11, Channel B.	28	DOBI6n	Data Out 12, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
29	DOAI7p	Data Out 13, Channel B.	30	DOBI7p	Over Range, Channel B.
31	DOAI7n	Led ADC	32	DOBI7n	Status Lock CDCM7005
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
33	ClkOIp	Data Clock Out, Channel A.	34	DOIRIp	Status VCXO CDCM7005
35	ClkOIn	Data Clock Out, Channel B.	36	DOIRIn	Status Ref CDCM7005
Dir	Reserved.		Dir	Reserved.	
37	Reserved.	Reserved.	38	Reserved	ADC External Trigger, P.
39	Reserved.	Reserved.	40	Reserved	ADC External Trigger, N.

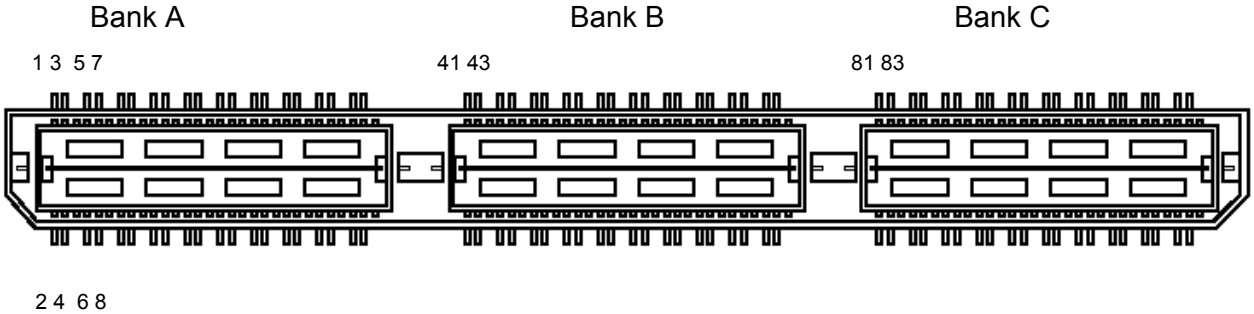
Figure 9 – Daughter Module Interface: Data Signals Connector and Pinout (Bank A).



Bank B

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Type	**Clock and Trigger System Signals**		**Type**	**Clock and Trigger System Signals**	
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
41	SMBClk	Temperature Sensor Clock.	42	SMBData	Temperature Sensor Data.
43	SMBnAlert	Temperature Sensor Alert.	44	SerialNo	Reserved
Dir	Daughter Card to Main Module		Dir	Reserved	
45	AdcVDacI	Reserved	46	AdcVDacQ	Reserved
47	AdcVRes	Reserved	48	AdcReset	Reserved
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
49	D3v3Enable	Reserved	50	D2v5Enable	Reserved
51	AdcMode	ADCA Serial Clock.	52	AdcClock	ADCA Serial Data.
Type	**ADC Specific Signals**		**Type**	**ADC Specific Signals**	
Dir	Main Module to Daughter Card		Dir	Reserved	
53	AdcLoad	ADCA Serial Enable.	54	AdcData	ADCB Serial Clock.
55	AdcCal	ADCB Serial Data.	56	AdjClkCntr0	ADCB Serial Enable.
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
57	AdjClkCntr1	ADCs Format (binary, 2's)	58	AdjClkCntr2	ADCs Reset
59	AdjClkCntr3	ADCs Output Enable	60	PllCntr0	CDCM7005 serial Enable.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
61	PllCntr1	CDCM7005 serial Clock.	62	PllCntr2	CDCM7005 serial Data.
63	PllCntr3	CDCM7005 Clock Selection.	64	AdcAClkSel	DAC PhStr.
Type	**Module Control Signals**		**Type**	**Module Control Signals**	
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
65	AdcBClkSel	DAC Reset.	66	IntClkDivEn	DAC Pll Lock.
67	IntClkDivnReset	DAC Serial Enable.	68	IntExtClkDivEn	DAC Serial Clock.
Dir	Main Module to Daughter Card		Dir	Main Module to Daughter Card	
69	IntExtClkDivnReset	DAC Serial Data.	70	FpgaVRef	Reserved
71	FpgaTck	Reserved	72	FpgaTms	Reserved
Dir	Daughter Card to Main Module		Dir	Reserved	
73	FpgaTdi	Reserved	74	FpgaTdo	Reserved
75	MspVRef	Reserved	76	MspTck	Reserved
Dir	Daughter Card to Main Module		Dir	Reserved	
77	MspTms	Reserved	78	MspTdi	Reserved.
79	Msptdo	Reserved	80	MspnTrst	Reserved

Figure 10 – Daughter Module Interface: Data Signals Connector and Pinout (Bank B).



Bank C (DAC)

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
81	DOAQ0p	Data In 0, Channel A.	82	DOBQ0p	Data In 1, Channel A.
83	DOAQ0n	Data In 2, Channel A.	84	DOBQ0n	Data In 3, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
85	DOAQ1p	Data In 4, Channel A.	86	DOBQ1p	Data In 5, Channel A.
87	DOAQ1n	Data In 6, Channel A.	88	DOBQ1n	Data In 7, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
89	DOAQ2p	Data In 8, Channel A.	90	DOBQ2p	Data In 9, Channel A.
91	DOAQ2n	Data In 10, Channel A.	92	DOBQ2n	Data In 11, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
93	DOAQ3p	Data In 12, Channel A.	94	DOBQ3p	Data In 13, Channel A.
95	DOAQ3n	Data In 14, Channel A.	96	DOBQ3n	Data In 15, Channel A.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
97	DOAQ4p	Data In 0, Channel B.	98	DOBQ4p	Data In 1, Channel B.
99	DOAQ4n	Data In 2, Channel B.	100	DOBQ4n	Data In 3, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
101	DOAQ5p	Data In 4, Channel B.	102	DOBQ5p	Data In 5, Channel B.
103	DOAQ5n	Data In 6, Channel B.	104	DOBQ5n	Data In 7, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
105	DOAQ6p	Data In 8, Channel B.	106	DOBQ6p	Data In 9, Channel B.
107	DOAQ6n	Data In 10, Channel B.	108	DOBQ6n	Data In 11, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
109	DOAQ7p	Data Out 12, Channel B.	110	DOBQ7p	Data Out 13, Channel B.
111	DOAQ7n	Data Out 14, Channel B.	112	DOBQ7n	Data Out 15, Channel B.
Dir	Daughter Card to Main Module		Dir	Daughter Card to Main Module	
113	Reserved.	DAC Clock P.	114	Reserved.	DAC LED.
115	Reserved.	DAC Clock N.	116	Reserved.	DAC Power Down.
Dir	Reserved.		Dir	Reserved.	
117	Reserved.	Reserved.	118	Reserved.	DAC External Trigger, P.
119	Reserved.	Reserved.	120	Reserved.	DAC External Trigger, N.

Figure 11 – Daughter Module Interface: Data Signals Connector and Pinout (Bank C).

3 Control Register Settings

The Control Registers control the complete functionality of the *SMT350*. They are setup via the Comport0 or 3. The settings of the ADC, triggers, clocks and the configuration of the SHB interfaces and the internal FPGA data path settings can be configured via the Control Registers.

3.1 Control Packet Structure

The data passed on to the *SMT350* over the Comports must conform to a certain packet structure. Only valid packets will be accepted and only after acceptance of a packet will the appropriate settings be implemented. Each packet will start with a certain sequence indicating the start of the packet (0xFF). The address to write the data payload into will follow next. After the address the data will follow. This structure is illustrated in the following figure:

	Byte Content							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'
1	Address 7	Address 6	Address 5	Address 4	Address 3	Address 2	Address 1	Address 0
3	Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
4	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

Figure 12 – Setup Packet Structure.

3.2 Reading and Writing Registers

Control packets are sent to the *SMT350* over Comport 0 or 3. This is a bi-directional interface. The format of a 'Read Packet' is the same as that of a write packet.

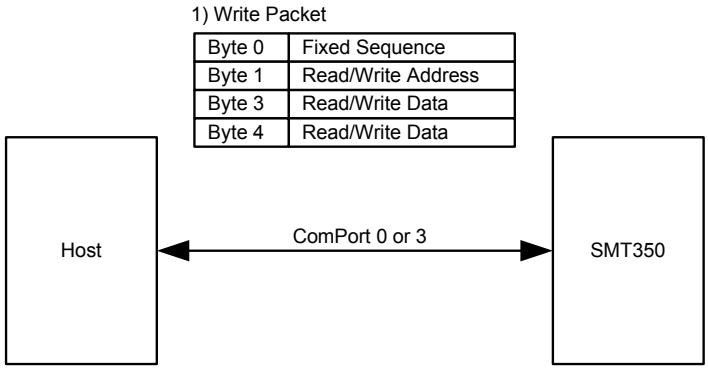


Figure 13 – Control Register Read Sequence.

3.3 Memory Map

The write packets must contain the address where the data must be written to and the read packets must contain the address where the required data must be read. The following figure shows the memory map for the writable and readable Control Registers on the *SMT350:*

Address	Writable Registers	Readable Registers
0x00	Reset Register.	Reserved.
0x01	Test Register.	Reserved.
0x02	ADCA Register 0.	Read-back ADCA Register 0.
0x03	ADCA Register 1.	Read-back ADCA Register 1.
0x04	ADCA Register 2.	Read-back ADCA Register 2.
0x05	ADCB Register 0.	Read-back ADCB Register 0.
0x06	ADCB Register 1.	Read-back ADCB Register 1.
0x07	ADCB Register 2.	Read-back ADCB Register 2.
0x08	DAC Register 0.	Read-back DAC Register 0.
0x09	DAC Register 1.	Read-back DAC Register 1.
0x0A	DAC Register 2.	Read-back DAC Register 2.
0x0B	DAC Register 3.	Read-back DAC Register 3.
0x0C	DAC Register 4.	Read-back DAC Register 4.
0x0D	DAC Register 5.	Read-back DAC Register 5.
0x0E	DAC Register 6.	Read-back DAC Register 6.
0x0F	DAC Register 7.	Read-back DAC Register 7.
0x10	CDCM7005 Register 0.	Read-back CDCM7005 Register 0.
0x11	CDCM7005 Register 1.	Read-back CDCM7005 Register 1.
0x12	CDCM7005 Register 2.	Read-back CDCM7005 Register 2.
0x13	CDCM7005 Register 3.	Read-back CDCM7005 Register 3.
0x14	CDCM7005 Register 4.	Read-back CDCM7005 Register 4.
0x15	CDCM7005 Register 5.	Read-back CDCM7005 Register 5.
0x16	CDCM7005 Register 6.	Read-back CDCM7005 Register 6.
0x17	CDCM7005 Register 7.	Read-back CDCM7005 Register 7.
0x18	Reserved	Main Module Temperature
0x19	Reserved	Main Module FPGA Temperature
0x1A	Reserved	Mezzanine Module Temperature
0x1B	Reserved	Mezzanine Module Converter Temperature
0x1C	Misc Register (Trigger, Clock Selection, etc…).	Read- Misc Register.
0x1D	Reserved	Firmware Version

Figure 14 – Register Memory Map.

3.4 Register Descriptions

3.4.1 Reset Register – 0x0.

	Reset Register – 0x0							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved				CDCM7005 Reset	DAC Reset	ADCs Reset	FPGA Registers Reset
Default	'0000'				'0'	'0'	'0'	'0'

3.4.2 Test Register – 0x1.

Any 16-bit value written in this register can be read-back to check that the Comport used works properly.

	Test Register – 0x1							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0								
1								

3.4.3 ADCA Register 0 – 0x2.

For more details, refer to ADS5500 datasheet.

	ADCA Register 0 – 0X2							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved						PLL	Reserved
Default	'000000'						'0'	'0'

	ADCA Register 0 – 0X2	
Setting	**Bit 1**	**Description**
0	0	PLL OFF – for sampling frequencies between 10 and 80 MHz
1	1	PLL ON – for sampling frequencies between 60 and 125 MHz

3.4.4 ADCA Register 1 – 0x3.

For more details, refer to ADS5500 datasheet.

	ADCA Register 1 – 0X3							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved					TP1	TP0	Reserved
Default	'000000'					'0'	'0'	'0'
0	Reserved							
Default	'00000000'							

	ADCA Register 1 – 0X3		
Setting	**TP1**	**TP0**	**Description**
0	0	0	Normal Mode of Operation
1	0	1	All outputs are zeroes
2	1	0	All outputs are ones
3	1	1	Continuous stream of ‘10’

3.4.5 ADCA Register 2 – 0x4.

For more details, refer to ADS5500 datasheet.

	ADCA Register 2 – 0X4							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved				PDN	Reserved		
Default	‘0000’				‘0’	‘000’		
0	Reserved							
Default	‘00000000’							

	ADCA Register 2 – 0X4	
Setting	**PDN**	**Description**
0	0	Normal Mode of Operation
1	1	Device in Power Down Mode

3.4.6 ADCB Register 0 – 0x5.

For more details, refer to ADS5500 datasheet.

	ADCB Register 0 – 0X5							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved						PLL	Reserved
Default	‘000000’						‘0’	‘0’

	ADCB Register 0 – 0X5	
Setting	**Bit 1**	**Description**
0	0	PLL OFF – for sampling frequencies between 10 and 80 MHz
1	1	PLL ON – for sampling frequencies between 60 and 125 MHz

3.4.7 ADCB Register 1 – 0x6.

For more details, refer to ADS5500 datasheet.

	ADCB Register 1 – 0X6							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved					TP1	TP0	Reserved
Default	‘000000’					‘0’	‘0’	‘0’
0	Reserved							
Default	‘00000000’							

	ADCB Register 1 – 0X6		
Setting	**TP1**	**TP0**	**Description**
0	0	0	Normal Mode of Operation
1	0	1	All outputs are zeroes
2	1	0	All outputs are ones
3	1	1	Continuous stream of ‘10’

3.4.8 ADCB Register 2 – 0x7.

For more details, refer to ADS5500 datasheet.

	ADCB Register 2 – 0X7							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved				PDN	Reserved		
Default	‘0000’				‘0’	‘000’		
0	Reserved							
Default	‘00000000’							

	ADCB Register 2 – 0X7	
Setting	**PDN**	**Description**
0	0	Normal Mode of Operation
1	1	Device in Power Down Mode

3.4.9 DAC Register 0 – 0x8.

For more details, refer to DAC5686 datasheet.

	DAC Register 0 – 0X8							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	atest					Version		
Default	‘000000’					‘000’		
0	Freq_int[7:0]							
Default	‘00000000’							

3.4.10 DAC Register 1 – 0x9.

For more details, refer to DAC5686 datasheet.

	DAC Register 1 – 0X9							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Freq_int[15:8]							
Default	‘00000000’							
0	Freq_int[23:16]							
Default	‘00000000’							

3.4.11 DAC Register 2 – 0xA.

For more details, refer to DAC5686 datasheet.

	DAC Register 2 – 0XA							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Freq_int[31:24]							
Default	'00000000'							
0	Phase_int[7:0]							
Default	'00000000'							

3.4.12 DAC Register 3 – 0xB.

For more details, refer to DAC5686 datasheet.

	DAC Register 3 – 0XB							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Phase _int[15:8]							
Default	'00000000'							
0	Mode[1:0]		Div[1:0]		Sel[1:0]		Counter	Full bypass
Default	'00'		'00'		'00'		'0'	'0'

3.4.13 DAC Register 4 – 0xC.

For more details, refer to DAC5686 datasheet.

	DAC Register 4 – 0XC							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Ssb	Interl	Sinc	Dith	Sync Phstr	Nco	Sif4	Twos
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
0	Dual_clk	DSS_gain[1:0]		Rspect	Qflag	Pll_rng[1:0]		Rev_bus
Default	'0'	'00'		'0'	'0'	'00'		'0'

3.4.14 DAC Register 5 – 0xD.

For more details, refer to DAC5686 datasheet.

	DAC Register 5 – 0XD							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Daca_offset[7:0]							
Default	'00000000'							
0	Daca_gain[7:0]							
Default	'00000000'							

3.4.15 DAC Register 6 – 0xE.

For more details, refer to DAC5686 datasheet.

	DAC Register 6 – 0XE							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Daca_offset[10:8]			sleepa	Daca_gain[11:8]			
Default				'0'	'0000'			
0	Dacb_offset[7:0]							
Default	'00000000'							

3.4.16 DAC Register 7 – 0xF.

For more details, refer to DAC5686 datasheet.

	DAC Register 7 – 0XF							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Dacb_gain[7:0]							
Default	'00000000'							
0	Dacb_offset[10:0]				sleepb	Dacb_gain[11:8]		
Default	'0000'				'0'	'000'		

3.4.17 CDCM7005 Register 0 – 0x10.

For more details, refer to CDCM7005 datasheet.

	CDCM7005 Register 0 – 0X10							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	VCXO_divider[3:0]				Reference Divider[9:6]			
Default	'0000'				'0000'			
0	Reference Divider[5:0]						Register Selection[1:0]	
Default	'000000'						'00'	

3.4.18 CDCM7005 Register 1 – 0x11.

For more details, refer to CDCM7005 datasheet.

	CDCM7005 Register 1 – 0X11							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Freq Detect	Manual or Auto Ref.	Programmable Delay N[2:0]			Programmable Delay M[2:0]		
Default	'0'	'0'	'000'			'000'		
0	VCXO_divider[11:4]							
Default	'00000000'							

3.4.19 CDCM7005 Register 2 – 0x12.

For more details, refer to CDCM7005 datasheet.

	CDCM7005 Register 2 – 0X12							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	OUT2A0	OUT1B1	OUT1B0	OUT1A1	OUT1A0	OUT0B1	OUT0B0	OUT0A1
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
0	OUT0A0	Output Signaling Selcetion[5:0]					Register Selection[1:0]	
Default	'0'	'00000'					'00'	

3.4.20 CDCM7005 Register 3 – 0x13.

For more details, refer to CDCM7005 datasheet.

	CDCM7005 Register 3– 0X13							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	90Div8	90Div4	ADClock	Status VCXO	Status Ref	OUT4B1	OUT4B0	OUT4A1
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
0	OUT4A0	OUT3B1	OUT3B0	OUT3A1	OUT3A0	OUT2B1	OUT2B0	OUT2A1
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

3.4.21 CDCM7005 Register 4 – 0x14.

For more details, refer to CDCM7005 datasheet.

	CDCM7005 Register 4 – 0X14							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Y0_MUX			Width FB_MUX			PDF Pulse	
Default	'000'			'000'			'00'	
0	CP Current				PRECP	CP_DIR	Register Selection[1:0]	
Default	'0000'				'0'	'0'	'00'	

3.4.22 CDCM7005 Register 5 – 0x15.

For more details, refer to CDCM7005 datasheet.

	CDCM7005 Register 5– 0X15							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Hold	Reset	ResHold	Power Down	Y4_MUX			Y3_MUX
Default	'0'	'0'	'0'	'0'	'000'			'0'
0	Y3_MUX		Y2_MUX			Y1_MUX		
Default	'00'		'000'			'000'		

3.4.23 CDCM7005 Register 6 – 0x16.

For more details, refer to CDCM7005 datasheet.

	CDCM7005 Register 6 – 0X16							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved				Hold	Hold Function 2	Hold Function1	Fast Clock
Default	'0000'				'0'	'0'	'0'	'0'
0	Fast Clock	Cycle Slip	Lock Cycles		Lock Window		Register Selection[1:0]	
Default	'0'	'0'	'00'		'00'		'00'	

3.4.24 CDCM7005 Register 7 – 0x17.

For more details, refer to CDCM7005 datasheet.

	CDCM7005 Register 7 – 0X17							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved							
Default	'00000000'							
0	Reserved							
Default	'00000000'							

3.4.25 Main Module Temperature – 0x18

	Main Module Temperature – 0X18							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Temperature in Celcius Degrees							
Default	'00000000'							

3.4.26 Main Module FPGA Temperature – 0x19

	Main Module FPGA Temperature – 0X19							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Temperature in Celcius Degrees							
Default	'00000000'							

3.4.27 Mezzanine Module Temperature – 0x1A

	Mezzanine Module Temperature – 0X1A							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Temperature in Celcius Degrees							
Default	'00000000'							

3.4.28 Mezzanine Module Converters Temperature – 0x1B

	Mezzanine Module Converters Temperature – 0X1B							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Temperature in Celcius Degrees							
Default	'00000000'							

3.4.29 Miscellaneous Register – 0x1C.

	Miscellaneous Register – 0X1C							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved		DAC Trigger		ADC Trigger		Clock Source	
Default	'00'		'00'		'00'		'00'	
0	ADCB Decimation Factor				ADCA Decimation Factor			
Default	'0000'				'0000'			

3.4.30 PCB and Firmware Version Registers

The PCB and Firmware Version registers can only be read by the Host. These registers indicate the PCB and Firmware versions of the SMT350.

4 PCB Layout

The following figures show the top and bottom view of the main module, the top view of the daughter-card and the module composition viewed from the side.

Figure 15 – Main Module Component Side.

Figure 16 - Main Module (*SMT368*) Solder Side.

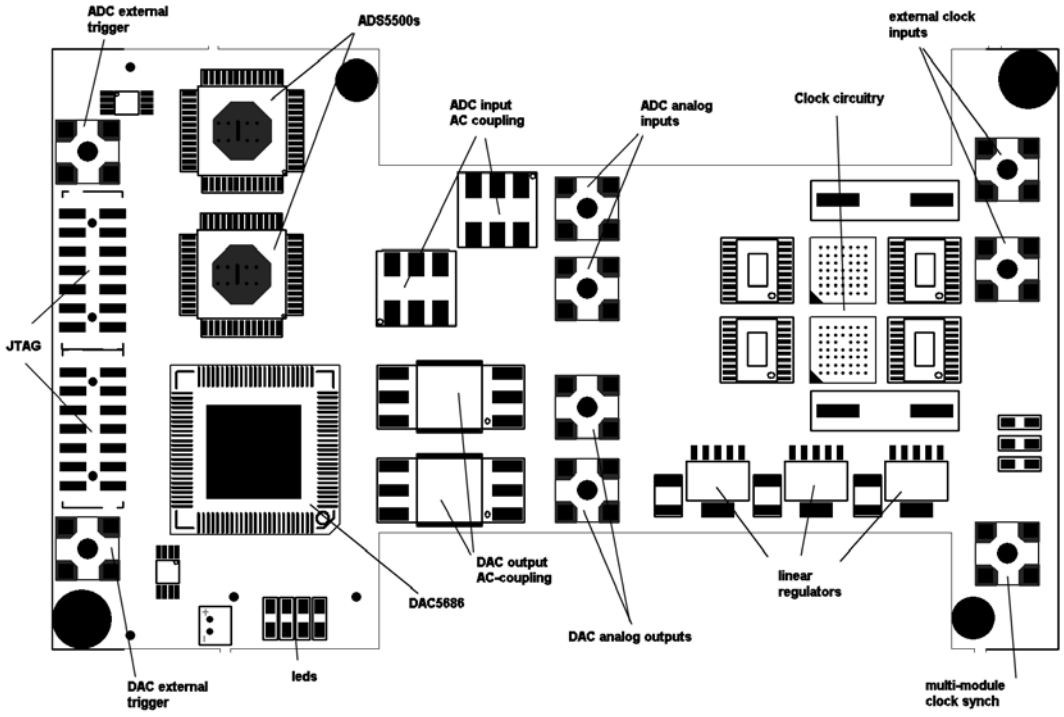


Figure 17 - Daughter Module Component Side.

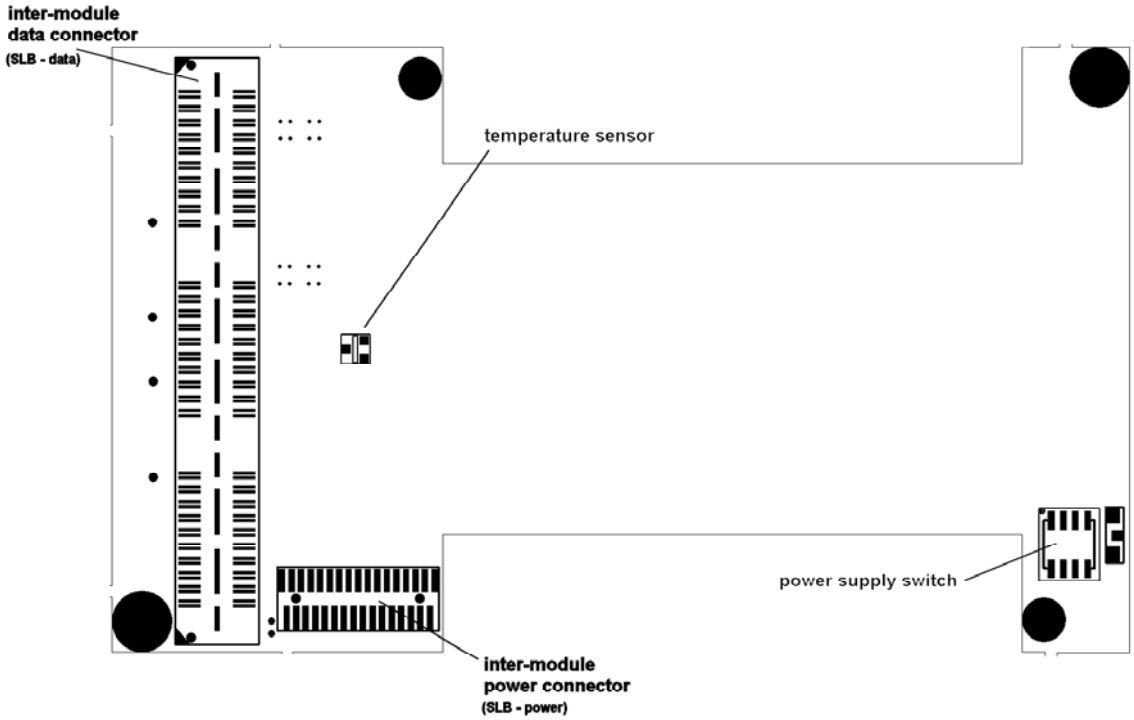


Figure 18 - Daughter Module Solder Side.