Unit / Module Name:	Memory module
Unit / Module Number:	
Used On:	SMT320, SMT310Q, SMT327, SMT300Q
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CONFIDENTIAL

Approvals		Date
Managing Director		
Software Manager		
Design Engineer		

Revision History

	Changes Made	Issue	Initials
24/06/02	Original release	1.0	PSR
01/07/02	Power supply re-designed; Layout modified; Virtex II Pinout added	1.1	PSR
02/07/02	Power LEDs and fan added	1.2	PSR
08/07/02	Improvements	1.3	PSR, JJW
01/08/02	CommPort 1 removed for FPGA pin assignment purpose	1.4	PSR
11/11/02	XC17v04 replaced by XC18v04	1.5	PSR
06/12/02	Memory package changed; Memory power consumption updated; JTAG connector pinout changed		PSR
18/6/03	Memory changed to MT46V16M16	2.0	GP
27/8/03	New pcb layout. Major text re-write.	2.1	GP
15/9/03	New pcb layout.	2.2	GP
16/9/03	Added ‘options’ section and updated PSU details.	2.3	GP
22/01/04	Updated Flow diagram Updated SHB section (2x32-bits interface) Added operating mode section Updated validation procedure (TIM tested with 370 and 365) Added external triggered functionality	2.4	JPA

Table of Contents

Table of Figures

1 Introduction

1.1 Overview

The *SMT351* is a single width TIM populated with 60-FBGA package memory devices. The module is able to store up to 1 Gigabyte or 512 Megabytes of data, depending on the version. Two or more modules can be cascaded to increase the storage capacity.

A Xilinx Virtex-II Pro FPGA (XC2VP7/20/30 FF896) controls input and output data flows coming in or going out on the two Sundance High-speed Bus (SHB*),* and two RSL (Rocket-IO) connectors. These busses are compatible with a wide range of Sundance processor, converter and I/O modules. It also controls transfers on the ComPorts.

The FPGA configuration is loaded via any one of the 6 ComPorts (jumper selectable).
The user controls the module by sending control words via the selected ComPort.

Four TTL I/Os are available (on a 6-pin header - Ground, 3.3V and 4 lines connected to the FPGA) for general purpose and eight LEDs as well (1 to indicate that the FPGA is configured, 3 to indicate that the power supplies are working and 4 driven by the FPGA).

The *SMT351* may require an external 5-Volt power supply.

1.2 Related Documents

Sundance High-speed Bus (*SHB*) specifications – Sundance.
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification_v1_0.pdf

TIM specifications.
ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf

Xilinx Application Note 134 – SDRAM Controller.
http://www.xilinx.com/xapp/xapp134.pdf

2 Functional Description

In this part, we will see the general block diagram and some comments on each of its entities. The architecture is built around a fast VirtexII-Pro FPGA that controls every single operation on the board. It receives control words from the outside world via a selected ComPort link and drives the DDR RAM blocks.

2.1 Block Diagram

The following diagram shows the block diagram of the *SMT351*:

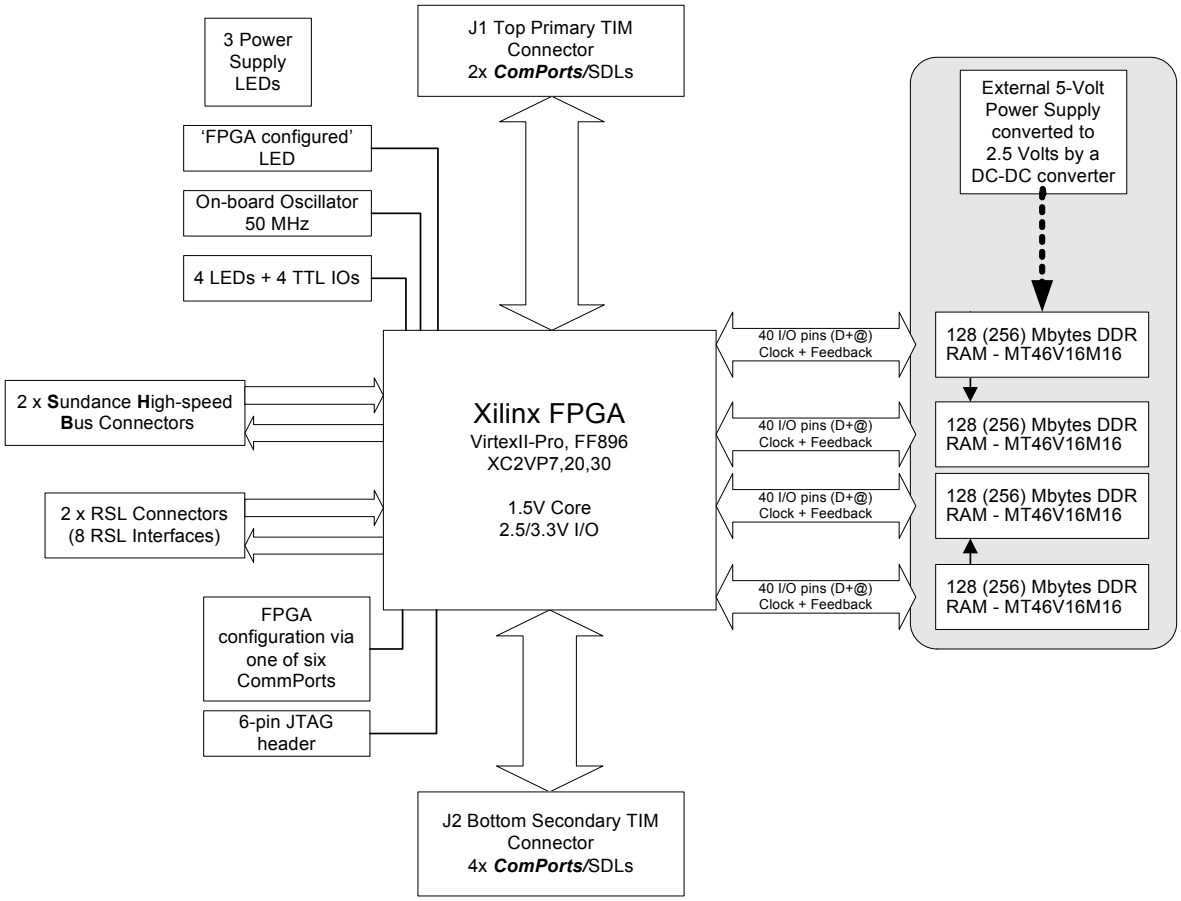


Figure 1 - Block diagram.

2.2 Module Description

The *SMT351* is a volatile storage module, built around a Xilinx VirtexII-Pro FPGA.
Input and output data travel to and from the FPGA via two 32-bit SHB interfaces or via the Rocket IO FPGA interfaces. The 32-bit interfaces are mapped onto 60-pin SHB connectors.

IMPORTANT
This module is available either with an XC2VP7, XC2VP20 or XC2VP30 FPGA. See the Manufacturing Options section for full details on available interfaces with each type of FPGA.

The *SMT351* is populated with DDR SDRAM memory (16 devices produced by Micron), controlled by the FPGA. It manages operations such as refreshing and bank pre-charging selection. The capacity can be either 512 Megabytes or 1 Gigabyte depending on the memory type. The memory is divided into 4 hardware banks (two clock-independent), to allow read and write operations of 32-bit words at up to 100 MHz.

The Xilinx FPGA VirtexII-Pro is configured via a 6-pin JTAG header or from a user selectable ComPort.

The internal register is loaded into the FPGA via a ComPort. Six ComPort links following the Texas Instrument C4x standard are available on the board and connected to the FPGA.

A global reset signal is mapped to the FPGA from the bottom TIM connector.
The FPGA drives four LEDs connected to give information while the board is working.
Four external TTL I/Os (pin header) are also available and connected to the FPGA.

A 5-Volt external power supply (an adaptor is available to connect a standard PC drive connector to the 351) may be used to provide enough current to the memory chips in cases where the carrier card's bus is insufficient (e.g. a PCI bus can't provide the required power).

2.3 Flow Diagram

The following flow diagram gives a different point of view of the *SMT351*.

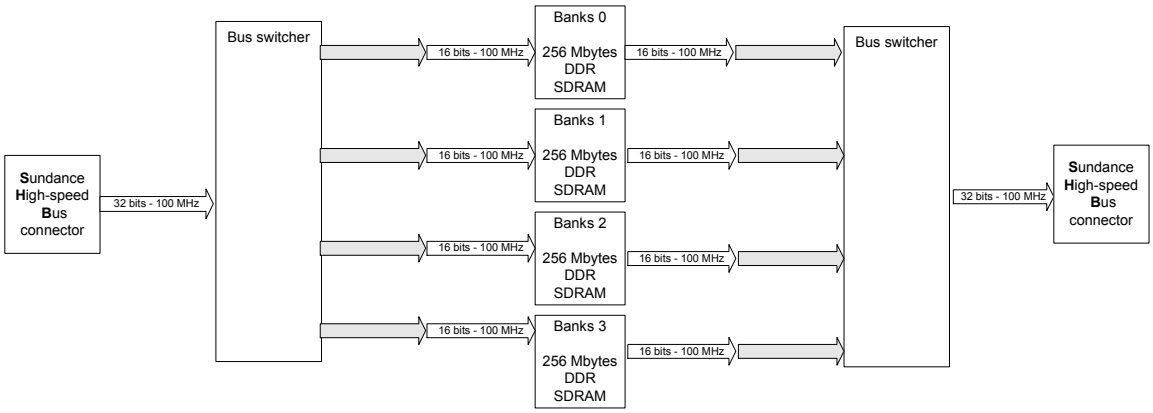


Figure 2 - Flow Diagram.

We can see more clearly on this diagram, how data goes through the board. The FPGA is responsible for multiplexing, bus switching, writing, reading, de-multiplexing and controlling the DDR memory.
Bus switching is controlled automatically.

2.4 Interface Description

2.4.1 3.3-Volt mounting holes

This module conforms to the TIM standard for single width modules. It requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards), which must be provided by the two diagonally opposite mounting holes.

2.4.2 5-Volt power supply

Each of the 16 memory devices takes about 0.6 Watt (Estimation made from an application note - TN-48-10 provided by Micron). The total amount of current is close to the maximum that the PCI can provide. In consequence, an external 5-Volt power source must be provided externally via a standard PC drive power connector.

2.4.3 Electric Fan

A fan (ARX Ball Bearing Cooler – BP0535SA7-1) on the FPGA is required to cool it down. It is connected to a 5-Volt 2-pin Molex right angle connector.

2.4.4 Digital connector : SHB

The *SMT351* includes two 60-pin connectors to transfer data in and out. Samtec manufactures the on-board connectors. It is a high-speed socket strip: *QSH-030-01-L-D-A-K*. Both connectors are identical and have a centreline of 0.5mm (0.0197”). This link gives further details: http://www.samtec.com/ftppub/pdf/QSH.PDF.
The external SHB cables are custom made by *Precision Interconnect* and a cable assembly solution builder can be found at: http://www.precisionint.com/tdibrsb/content/howtouse.asp. They are micro-coax cables and can achieve high-speed data transfer between TIM modules. As a result, no differential lines are required to transfer data on longer cables.

2.4.5 Digital connector : RSL

Very high speed serial data may be presented to the FPGA via the RSL connectors. These are Samtec QTE and QSE types, and carry differential signals (Xilinx Rocket IO) direct to the FPGA. Two types of connector are defined, and reference should be made to the RSL Pin-out document from Sundance.

2.4.6 Configuration connector

The *SMT351* includes a 6-pin JTAG header (2mm DIL header), which allows re-programming the FPGA using a cable such as Xilinx Parallel III or Parallel IV *cables*.

The pin-out of the JTAG 6-pin header:

Pin	Signal
1	VCC
2	GND
3	TCK
4	TMS
5	TDI
6	TDO

Figure 3 - JTAG 6-pin header.

2.4.7 ComPort interface

ComPorts (Communication ports) links follow Texas Instrument C4x standard. They are 8-bit parallel inter-processor ports of the ‘C4x processors.
The *SMT351* provides 6 links. These are given the numbers 0 to 5.

The ComPorts drive at 3.3v signal levels, and are not 5V tolerant.
See Manufacturing Options section for details about available ComPorts.

The FPGA can implement up to six FIFO buffered ComPort interfaces fully compliant with the TIM standard. They are guaranteed for a transfer rate of 20MB/s.
The FIFOs are useful to maintain a maximum bandwidth and to enable parallel transfers.
Therefore, as an example, each ComPort can be associated with two Xilinx 15x32-bit unidirectional FIFOs implemented into the FPGA; one for input and one for output. An additional one-word buffer makes them appear as 16x32-bit FIFOs.

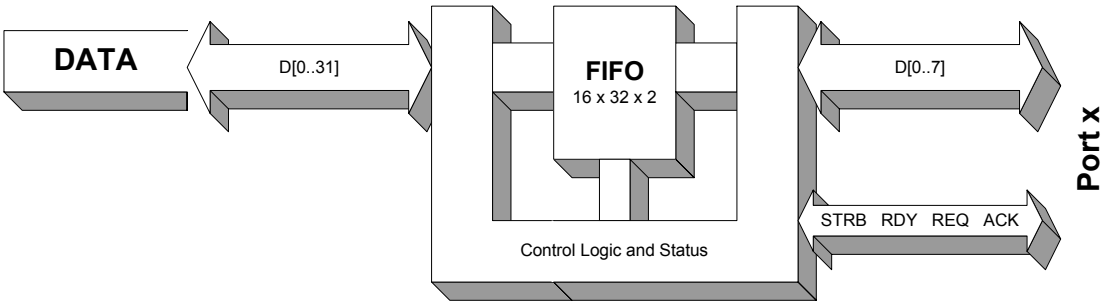


Figure 4 - ComPort interface data path.

Control words can be loaded via only one ComPort, the one selected using the on-board jumpers.

2.4.8 *SHB* interface

SHBs are parallel communication links for synchronous transmissions.
A 32-bit unidirectional interface is implemented on each SHB connector.

SHBA = 32-bits SHB interface receiver only (400MB/sec).
SHBB = 32-bits SHB interface transmitter only (400MB/sec).

Both *SHB* buses are identical and 60 bits wide.

2.5 Operating mode

The default FPGA configuration implements one 32-bit unidirectional interface on each SHB connector.

SHBA = 32-bits SHB interface receiver only (400MB/sec).
SHBB = 32-bits SHB interface transmitter only (400MB/sec).

Data on the bus is grabbed when Write Enable is low. Read-back operations are started automatically or by sending the right control word.

Data is written or read-back by blocks of 1024 words of 16 bits.
Two modes are available:

Automatic single module mode: the FPGA controls data addressing. Data are written from SHBA and read on SHBB. Read and write operation can happen simultaneously.

Automatic multiple module mode: the FPGA controls data addressing. Data are written from SHBA and read on SHBB. Read and write operation can happen simultaneously. Data first received are written into the last module and then into the one above in the chain once the last module memory is full. Data are passed through the first module(s) when written into the last one.
Switch SW2 is used to determine if the board is the last one in the chain.

Read back operation will start as soon as the first bank is full or buffer size is reached (buffer size represent the amount of data to store and will be set in a register by user) if RBEN bit is set. SHBB send data until its ACK signal is activated signalling that transmittion must be interrupted.
Receiver asserts ACK ACTIVE to stop transmittion when its memory buffer is full.

If EXTTG bit of control register is set then read back operation will be triggered by an external signal coming from connector JP2 pin 2.

2.5.1 Registers definition:

Read back start address: (optionnal)

19-2	0-1
SNMB	BX
W*, 000000000000000000	W*,00

* : not available for the current version of the firmware.

Field	Description (flags are active when 1)		
BX	Memory bank number	00	Bank 0
		01	Bank 1
		10	Bank 2
		11	Bank 3
SNMB	Sample number in selected memory bank. Must be a multiple of a row size (256*32-bits words). 0 <= SNMB <= 8192*4*4 0 <= SNMB <= 131072		

Control register:

3	2	1	0
EXTRGLVL	EXTTG	RBEN	CLR
W,1	W,0	W,1	W,0

Field	Description (flags are active when 1)
CLR	Clear FIFOs, reset memory, and reinitialise board with user settings.
RBEN	Read back enable. When this bit is set read back of memory is enabled.
EXTTG	0 : External trigger off, 1 : Read back operation triggered by external signal
EXTRGLVL	0 : external trigger active level is low, 1 : external trigger active level is high

Buffer size:

This register defines the total amount of data that will be stored on board.

2.5.2 Power supplies

5.0V	This is supplied directly from the TIM connectors to the power module mezzanine.
3.3V	This is supplied by the TIM mounting holes. It is used for the CPLD (FPGA configuration) and some FPGA I/O pads. It further supplies power to the power module mezzanine.
2.5V	This supply is required for the FPGA I/O, FPGA aux. and DDR memories. It is derived from 5.0V using a switching converter.
2.5Vrocket	The FPGA's RocketI/O transceivers require a separate 2.5V supply. This is provided using two linear regulators fed with 3.3V.
1.5V	The FPGA core requires a 1.5V supply. This comes from the power module and is produced from 5.0V using a switching converter.
1.25V	The DDR memories require that most control lines be terminated to 1.25V. Again, this is provided using a switching converter from 3.3V.

3 Manufacturing Options

The module can either have an XC2VP7, VP20 or VP30 FPGA fitted. The choice of component will be determined by various factors such as available resources and cost.

The following table shows what resources are (and are not) available with each FPGA.

FGPA Device Fitted			
XC2VP7		XC2VP20 / 30	
Available	Not available	Available	Not available
ComPort0 ComPort3	ComPort1 ComPort2 ComPort4 ComPort5	ComPort0 ComPort1 ComPort2 ComPort3 ComPort4 ComPort5	
4x16-bit SHBs	All SHB USER pins SHB B2 pins	4x16-bit SHBs SHB USER pins 0-3	SHB B2 pins
8xRocket I/O		8xRocket I/O	
1xPowerPC processor block		2xPowerPC processor blocks	

4 Verification Procedures

The specifications will be tested using the following:

1) ComPorts: ComPort transfers between an *SMT365* and the *SMT351*.
2) SHB:

SMT370===>SMT351===>SMT365 (data-logging)
SMT365===>SMT351===>SMT370 (playback)
SMT365===>SMT351===>SMT365 (DSP-MEM loop)

5 Review Procedures

Reviews will be carried out as indicated in design quality document QCF14 and in accordance with Sundance's ISO9000 procedures.

6 Validation Procedures

7 Timing Diagrams

8 Circuit Diagrams

9 PCB Layout Details

9.1 Component Side

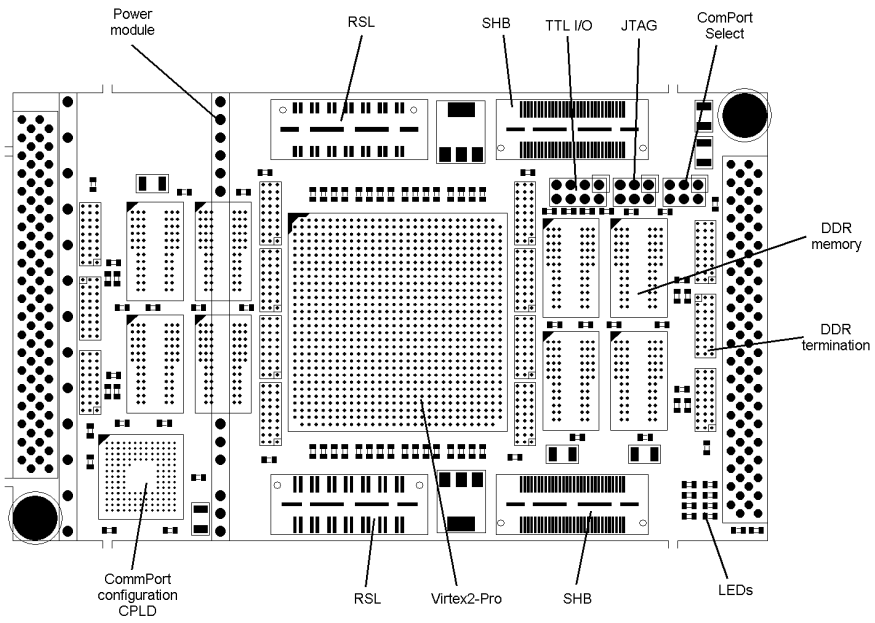


Figure 5 - SMT351 Layout – Top side.

9.2 Solder Side

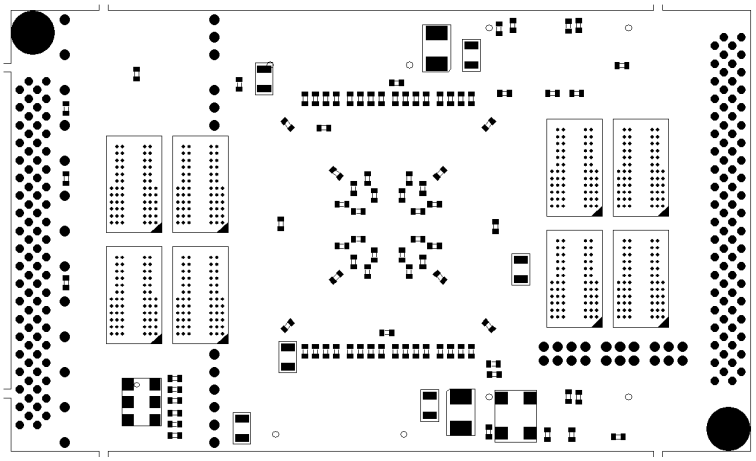
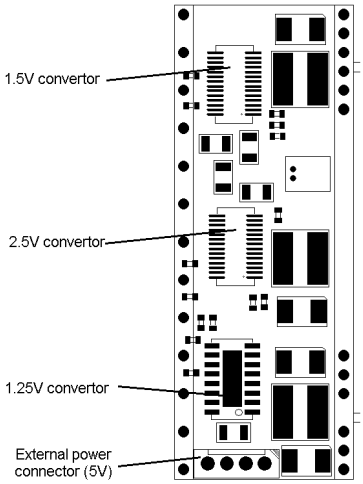


Figure 6 - SMT351 Layout – Bottom side.

9.3 Power Module



10 Safety

This module presents no hazard to the user.

11 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.
This module is protected from damage by fast voltage transients originating from outside the host system, which may be introduced through the output cables.
Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.