Unit / Module Description:	What is this all about?
Unit / Module Number:	SMT362
Document Issue Number:	2.2
Issue Date:	29th April 2009
Original Author:	Graeme Parker

User Manual for SMT362

Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	5/2/07	GKP
1.1	Update	20/6/07	GKP
1.1.1	Added CCS basic info.	2/8/07	GKP
1.2	Added default firmware links configuration	2/6/08	E.P
1.3	Added McBSP connectivity detail.	21/7/08	GKP
1.4	Added FPGA pin-out	22/7/08	GKP
2.0	Major update to include missing detail from the technical specification.	3/10/08	GKP
2.1	Corrected PHY references.	17/12/08	GKP
2.2	Default for McBSP1 or GPIO is GPIO.	29/4/09	GKP

Table of Contents

1 Introduction

The SMT362 is a dual processor module. Each TMS320C6455 processor runs at up to 1GHz. This provides a module performance of up to 16GIPS.

Each processor has independent access to 256Mbytes of DDR2 memory.

A single 4Mbyte flash memory device is directly connected to the primary DSP (DSP A). This device contains the DSP boot code and FPGA (Virtex-4) configuration.

The secondary DSP (DSP B) boots from its Host Port Interface, which is directly connected to DSP A.

The FPGA provides 6 TIM compatible comm. ports, 2 Sundance SHBs, up to 16 RSLs, and other minor functions. The FPGA can be easily customised.

The SMT362 could be used in applications where the FPGA does the pre-processing, the first DSP the 'Input Signal Processing', the second DSP does 'Output Signal Processing', and the FPGA does the final post-processing.

2 Related Documents

TI TMS320C6455 material (http://focus.ti.com/docs/prod/folders/print/tms320c6455.html).

Sundance SHB specification. (ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification_v1_0.pdf)

Sundance RSL specification. (http://www.sundance.com/docs/RSL - Technical Specification Rev01 Iss03.pdf)

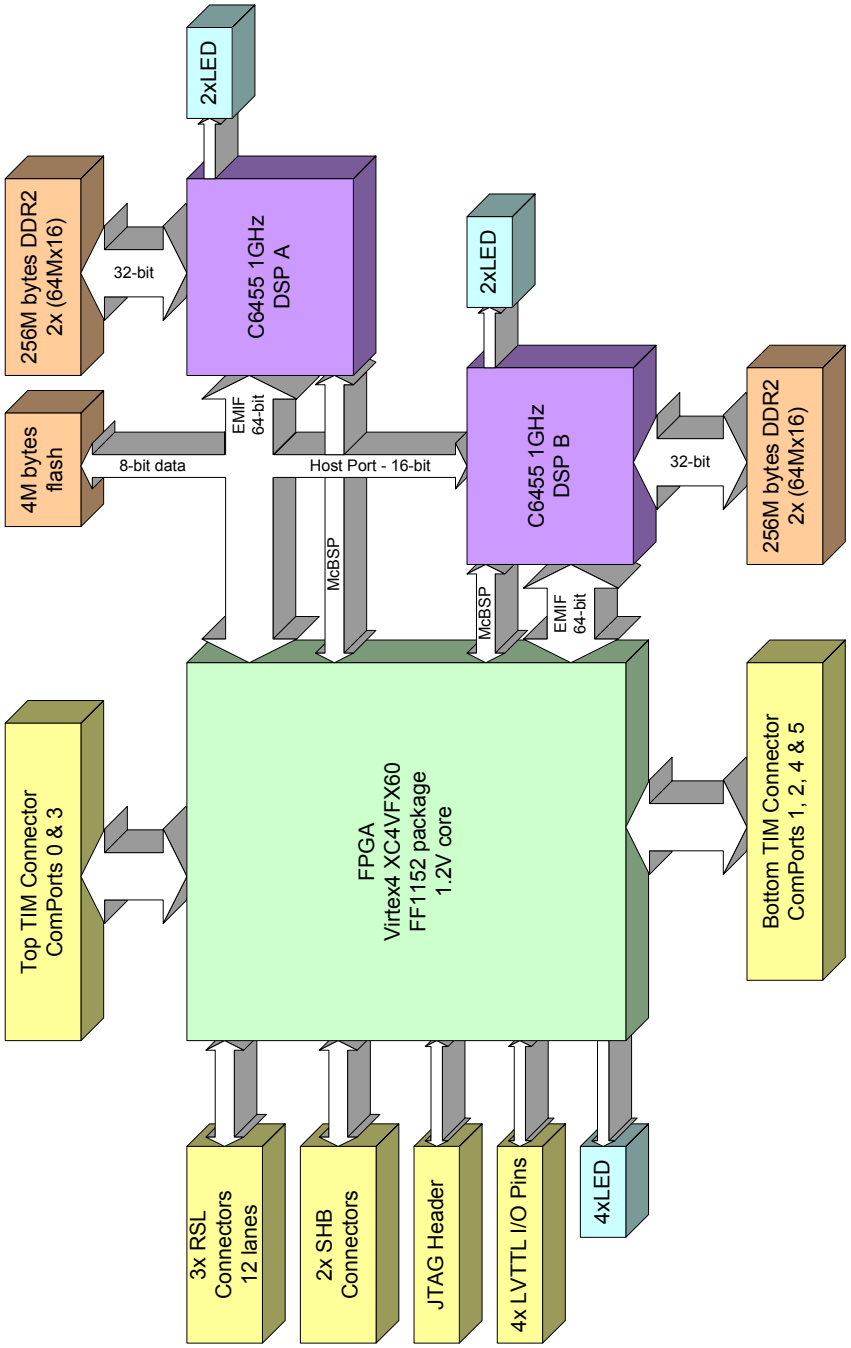
TI TIM specification & user's guide. (ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf)

3 Acronyms, Abbreviations and Definitions

A list of acronyms etc (http://www.sundance.com/web/files/static.asp?pagename=acc).

4 Functional Description

4.1 Block Diagram



4.2 Module Description

4.2.1 Mechanical Interface

This module conforms to the TIM standard for single width modules. It requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards) that must be provided by the two diagonally opposite mounting holes.

4.2.2 Processor

The module incorporates two TMS320C6455 DSPs.

A JTAG interface is provided to enable application debugging via a suitable JTAG controller and software. The DSPs' JTAG interfaces are chained and available only on the Top TIM connector. Typically, the JTAG controller this will be an SMT107 or 310/Q and TI Code Composer Studio. This is an invaluable interface that enables the application programmer to quickly debug a 'chain' of processors in single or multi-processor situations.

The DSPs have two external memory interfaces. One connects directly to the DDR2 (2 devices of 128M bytes clocked at 250MHz:DDR2-500) and the other (EMIFA, clocked at 133MHz) is used to interface to the remaining peripherals.

Each DSP provides 4 chip selects (numbered 2-5) on its EMIFA interface. The function of each is shown below;

Chip select	Base Address (hex)	DSPA	DSPB
CE2	A0000000	FPGA	FPGA
CE3	B0000000	Flash	Unused
CE4	C0000000	HPI of DSPB	Unused
CE5	D0000000	FPGA configuration	Unused

Separate to the EMIFA, the DSP provides an interface solely for the connection of DDR2 memory. This is addressed as shown here;

DDR2	E0000000	DDR2 SDRAM	DDR2 SDRAM

4.2.3 Flash

A 4Mbyte flash memory is provided with direct access by DSP A. This device contains boot code for the DSP and the configuration data for the FPGA.

This device is directly connected to DSP A. This is an 8-bit wide device.

The flash is mapped with address bits 0 & 1 (byte addressing) connected to the top address of the flash so a sector erase will need to erase 4 sectors at once. This is equivalent to having a flash of 32 128Kwords sectors (instead of 128 32Kwords sectors). The flash is only accessible byte-wise so it gives a total capacity of the flash of 4MB.

4.2.4 DSP Reset

The DSPs' configuration is determined during the reset process. The state of the EMIF address lines is examined, and this determines the on-chip peripheral status.

The following table details this;

EMIFA	Comment
0	Latched at reset. Not used on the 362.
1	Latched at reset. Not used on the 362.
2	Latched at reset. Not used on the 362.
3	Pull-up via 1k0.
4	GP01 function. Connected to CPLD via 1k0. A ‘0’ (default) makes this an I/O pin. A ‘1’ enables the SYSCLK3 signal to be output.
5	McBSP1 or GPIO selection. Connected to the CPLD via 1k0. A ‘1’ enables the McBSP (default if GPIO).
6	NC – PCI speed.
7	NC – internal pull-down.
8	NC – PCI auto-init.
9	Pull-up with 1k0. Used to select MAC with an RGMII interface.

EMIFA	Comment
10	Pull-up with 1k0. Used to select MAC with an RGMII interface.
11	Pull-up via 1k0.
12	UTOPIA or EMAC select. Internal pull-down selects EMAC.
13	Internal pull-up selects little endian operation.
14	Internal pull-down selects 16 bit HPI operation.
15	Connected to CPLD via 1k0. A ‘0’ selects external clock for EMIF. A ‘1’ selects SYSCLK3/8 as EMIF clock.
16	Internal pull-down. Set to ‘0’ for DSPA. Set to ‘1’ for DSPB. Together with EMIFA17-19, this sets the boot mode.
17	Internal pull-down.
18	Internal pull-down. Set to ‘1’ for DSPA. Set to ‘0’ for DSPB.
19	Internal pull-down.

Boot mode is the 4-bit value from EMIFA[19:16]. This is 0100 for DSPA (ROM boot) and 0001 for DSPB (HPI boot).

4.2.5 DSP Boot

When the module is reset, both DSPs come out of their reset state. DSPA will begin execution of code stored in the flash memory. DSPB is set to boot from host port, and will thus wait until is has had its boot code loaded by DSPA. The DSPA boot code (factory programmed by default) will load the FPGA configuration (again from flash), boot DSPB over the EMIF to host port interface, perform any necessary initialisation and then enter a ComPort boot sequence. The ComPort boot involves polling the ComPort status register(s) and downloading code from the first active port.

DSPB, when booted, will simply enter the ComPort boot sequence after initialising any of its internal devices.

4.2.6 Host Port Interface (HPI)

The HPI of DSPA is not connected, and DSPB's is connected to the EMIF of DSPA.

4.2.7 Virtex 4 FX FPGA

This device, a Xilinx XC4VFX, is responsible for the provision of the two SHBs, 6 Com-Ports, and the RSLs. On power-up, this device is un-configured (SRAM based FPGA technology). During the DSP boot process, the FPGA is configured for normal operation.

4.2.7.1 FPGA Configuration

Before any functions of the FPGA can be used it must be configured. This is a process undertaken by DSP A during its boot procedure. The FPGA is configured via the slave serial mode with the DSP presenting the serial data on EMIF data bit 8.

First, the PROG pin must be asserted low, then high. The FPGA's PROG pin is connected directly to DSPA's general purpose i/o pin 2 (GPIO).

Then data must be read from the flash (During the normal boot process, the configuration data is read from flash. If the FPGA needs to be reconfigured during application execution, then the configuration data maybe read from any source.) and written to the FPGA.

This procedure is completely automatic during the module's boot process.

Removing jumper JP2 will hold the FPGA in an unconfigured state. This could be useful if an erroneous bit stream has been loaded into flash (EMIF data bus corruption etc), which could result in the module not being accessible even using Code Composer (JTAG).

4.2.7.2 FPGA Configuration via JTAG

The FPGA may also be configured using a Xilinx JTAG programming system connected to header JP1. The pin-out of this header is given here;

Signal	Pin	Pin	Signal
Power	1	4	TMS
Ground	2	5	TDI
TCK	3	6	TDO

4.2.7.3 Com-Ports

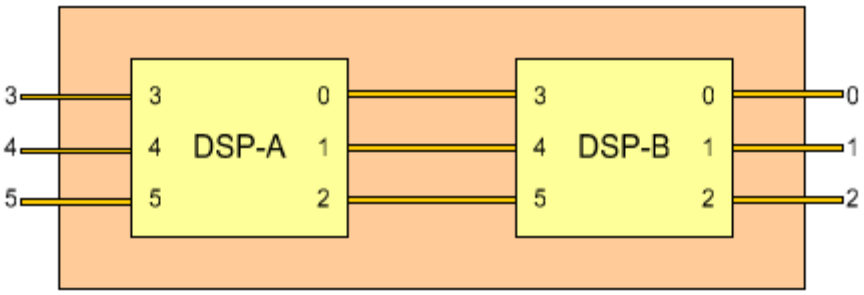


Figure 1: Default firmware ComPort links..

4.2.7.4 SHB

The SMT362 has two SHB connectors, both of which are connected to DSPA to give 32-bit SDB interfaces.

SDB0 and SDB1 on DSPA are presented on the TIM's SHB connectors, SHBA and SHBB respectively. SDB0 and SDB1 on DSP-B are not connected. SDB2 of DSPA has a fixed internal connection to SDB2 of DSPB.

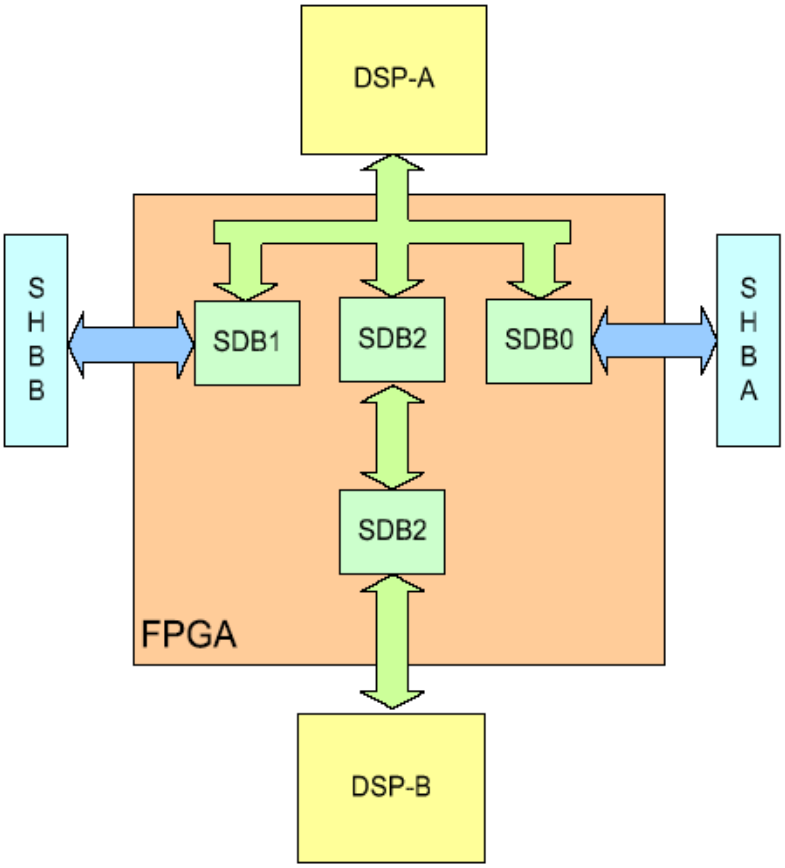


Figure 2: Default firmware SHB links. See the general firmware description.

4.2.7.5 PXI

An external PXI clock and 4 trigger signals are available on the user defined pins of the TIM connectors. These can be used for a variety of purposes, including synchronisation and triggering of data acquisitions, or for any user application specific function.

4.2.8 GPIO (General Purpose I/O)

Two GPIO signals from each DSP are used to illuminate LEDs as shown here;

	DSPA	DSPB
GPIO 14	D3	D5
GPIO 15	D2	D4

The LEDs are labelled on the board as 'Dn'.

Four other GPIO signals from the FPGA are connected directly (un-buffered, 3.3V LVTTL ONLY) to connector JP3. The pin-out and FPGA pad number is shown here;

Signal	Pin	Pin	Signal
3.3V	1	4	Pad D10
Ground	2	5	Pad H10
Pad C10	3	6	Pad G10

All of the DSP's GPIO signals are described here;

GPIO	Function
0	CLKR1 (to FPGA)
1	SYSCLK3
2	PROG
3	CLKX1 (to FPGA)
4	INT4 (to FPGA)
5	INT5 (to FPGA)
6	INT6 (to FPGA)
7	INT7 (to FPGA)

GPIO	Function
8	DR1 (to FPGA)
9	DX1 (to FPGA)
10	FSR1 (to FPGA)
11	FSX1 (to FPGA)
12	Flash A20
13	Flash A21
14	LED1
15	LED2

The McBSP signals (CLKR1, CLKX1, DR1, DX1, FSR1 and FSX1) are all connected to the FPGA. They are normally set to function as McBSP signals, but it is possible to enable these as GPIO and hence a source of a further 6 interrupts to the DSP.

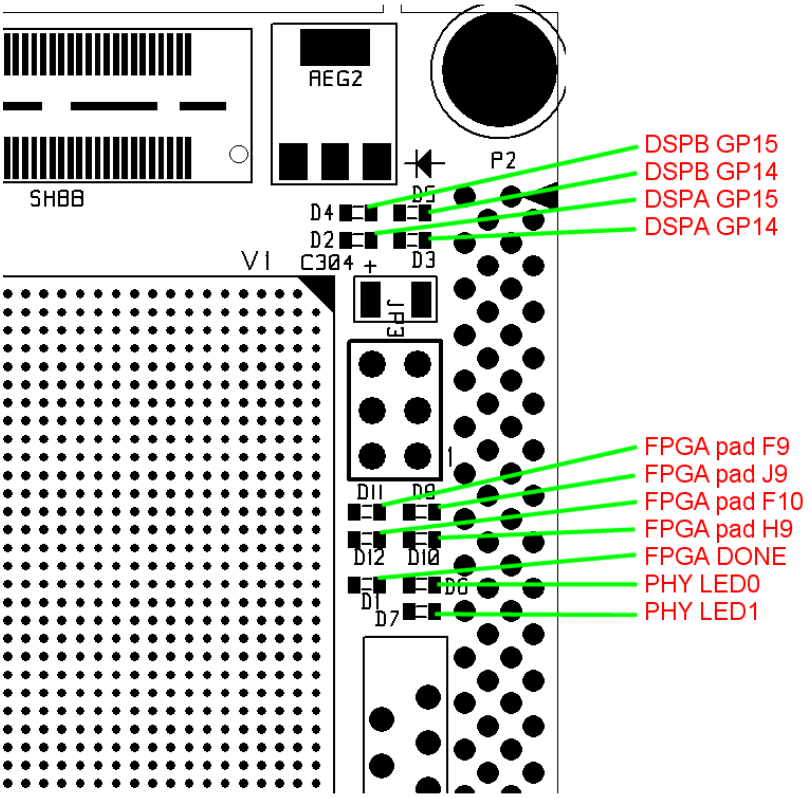
The above signals are independent between DSPs.

GPIO2, 12 and 13 are connected to the FPGA on DSPB (DSPB does not have access to a flash memory and cannot configure the FPGA).

4.2.9 LEDs

Eleven LEDs are present on the SMT362. Their function and position are shown here;

LED	Function
D1	FPGA DONE status (illuminates when the FPGA is configured)
D2	DSPA GP15
D3	DSPB GP14
D4	DSPB GP15
D5	DSPB GP14
D6	PHY LED0
D7	PHY LED1
D9	FPGA pad J9
D10	FPGA pad H9
D11	FPGA pad F9
D12	FPGA pad F10



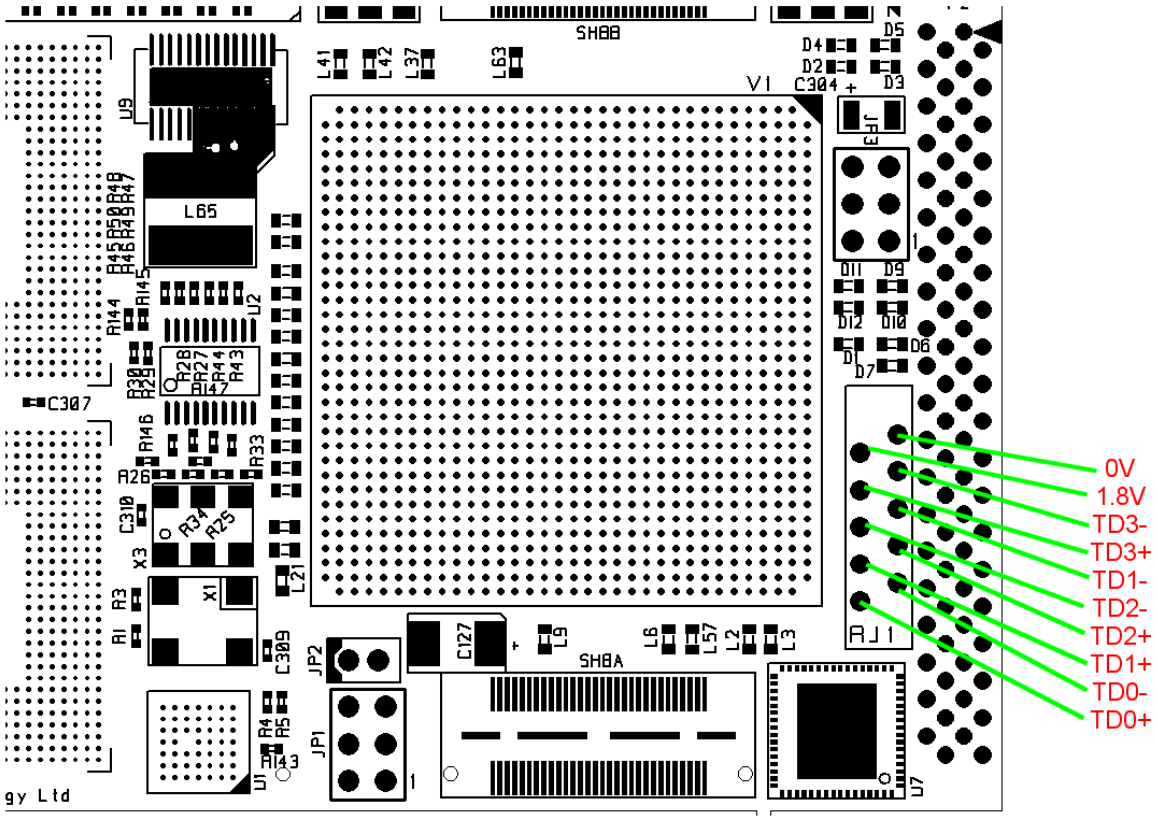
4.2.10 Ethernet

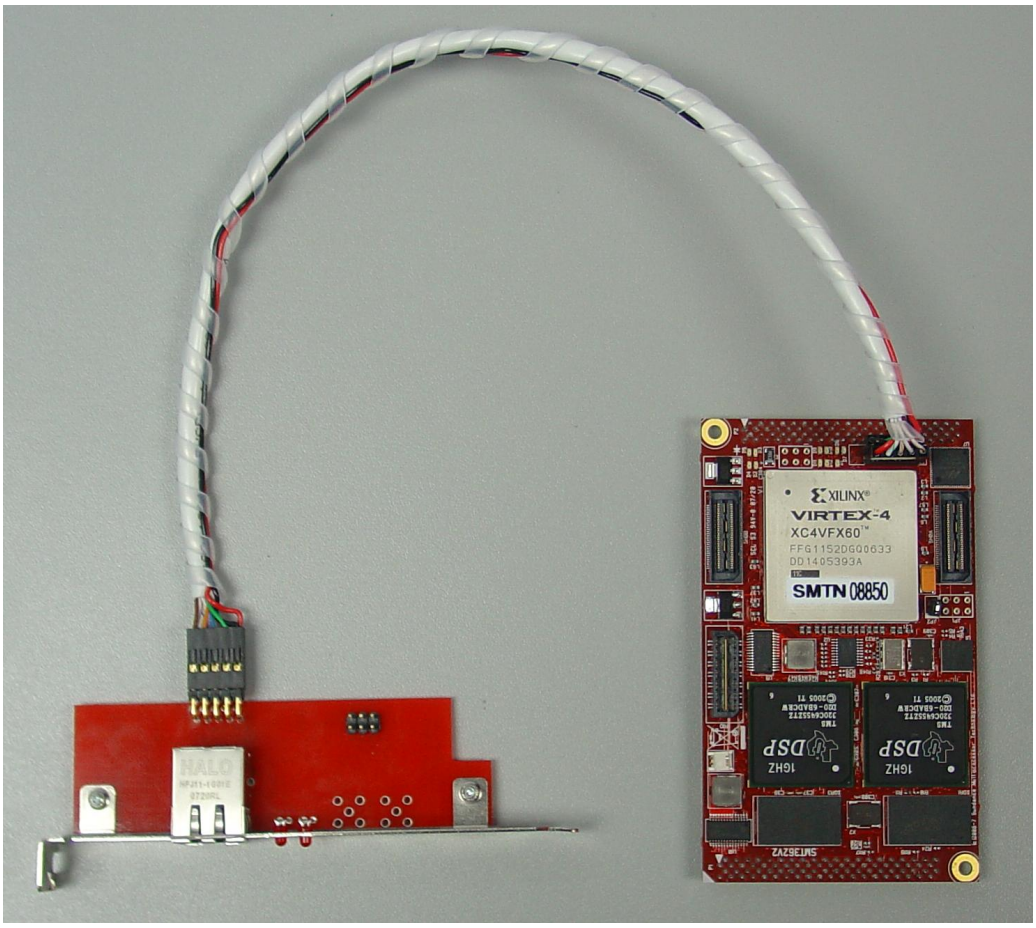
A Marvell 88E1116 PHY is connected to a 1.8V I/O bank of the FPGA. Each of the DSP Ethernet PHY interfaces are also connected to the FPGA. This connectivity should allow routing of data from either DSP to the RJ45 connector (optional).

On the SMT362 PCB, pin headers are provided to connect into the Ethernet system. We recommend the use of the Halo HFJ11-1G01E 'Fastjack' connector.

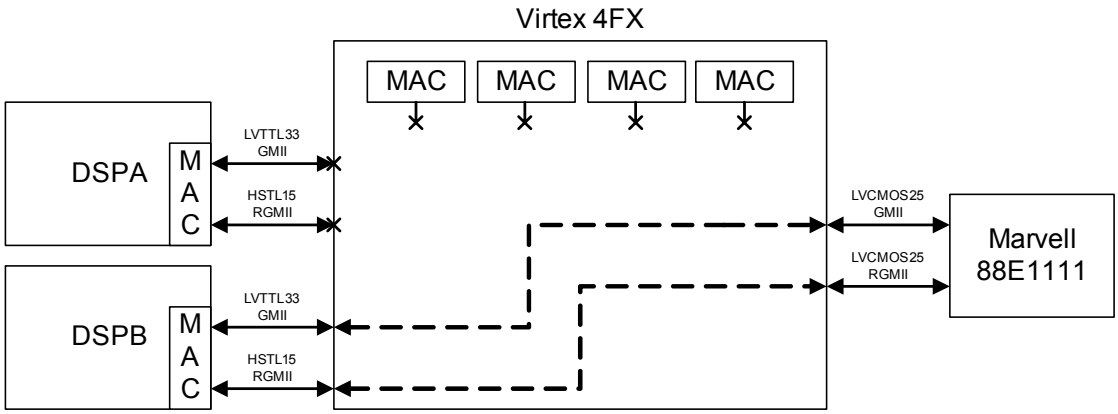
Sundance can supply the SMT562E PC rear panel which includes the RJ45 connector and a connecting cable (see picture on following page).

For non-gigabit applications, a twisted pair wired connection can be made from the RJ1 connector pins to a suitable panel mount socket.





SMT362 connected to the SMT562E for Gigabit Ethernet applications. Note the polarity of each end of the cable.



The default configuration of connecting DSPB's MAC directly to the 88E1116 PHY through the Virtex 4 is shown in the diagram above. In this configuration, the Virtex 4 is essentially acting as a voltage translator.

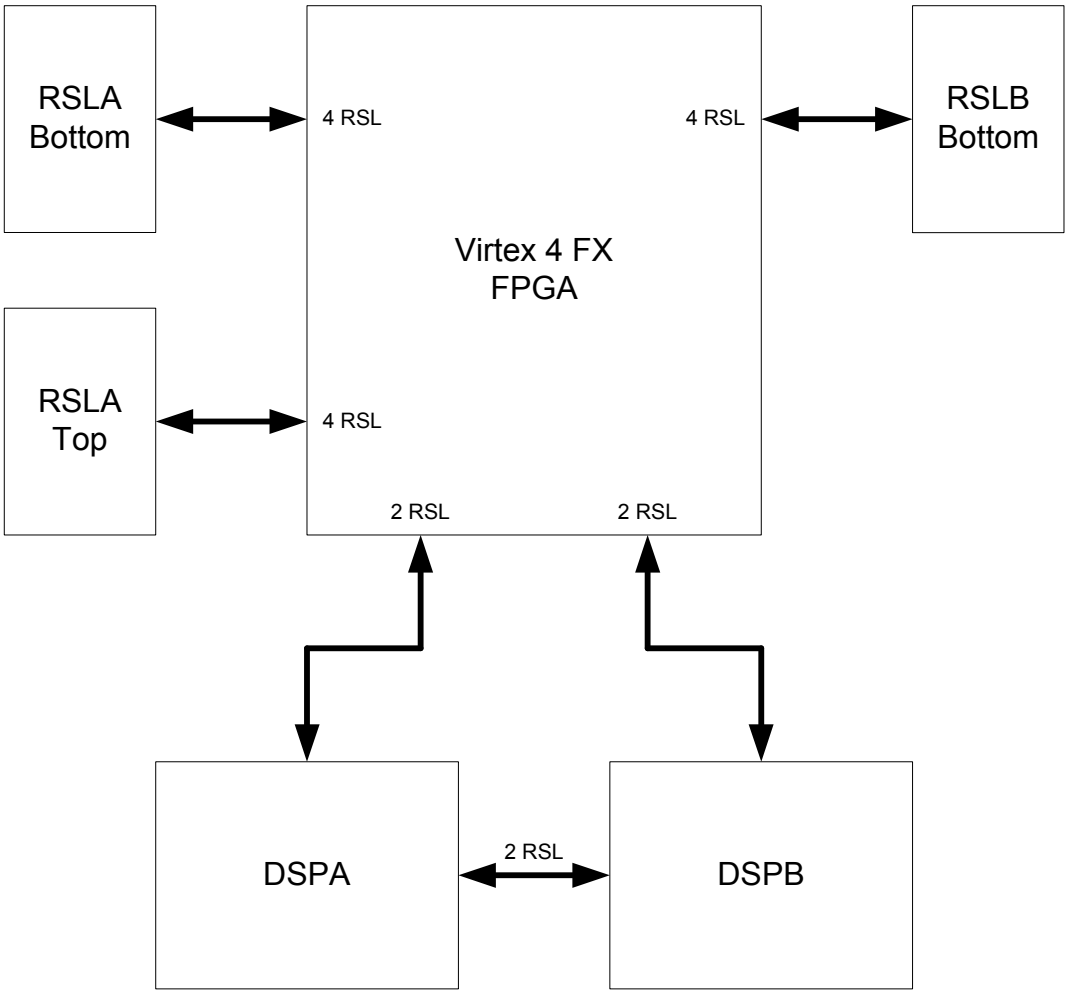
4.2.11 RapidIO and RSLs

The FPGA provides 16 RocketIO serial interfaces. These are normally run at 2.5Gbps.

Each DSP has 4 SRIO interfaces. Again, these are normally run at 2.5Gbps.

All of these serial interfaces are knows in Sundance as RSL (Rocket Serial Link).

The RSL connectivity is shown here;



4.2.12 McBSP & Timers

Each DSP has two McBSPs (multi-channel buffered serial port), 0 and 1.

McBSP1 from DSPA connected to McBSP1 on DSPB.

McBSP0 from each DSP is connected independently to the FPGA.

The full FPGA pin-out is given in the smt362_fpga_pinout.ucf file.

The following link covers the McBSP operation in detail:

http://focus.ti.com/lit/ug/spru580g/spru580g.pdf

Each DSP has two timers composed from two pins, TINP and TOUTP. All four of these pins (for each DSP) are connected to the FPGA.

4.2.13 Power Supplies

This module must have 5V supplied through the TIM connectors. In addition, a 3.3V supply is required and should be supplied through the TIM mounting holes. This is compatible with the all Sundance TIM carrier boards.

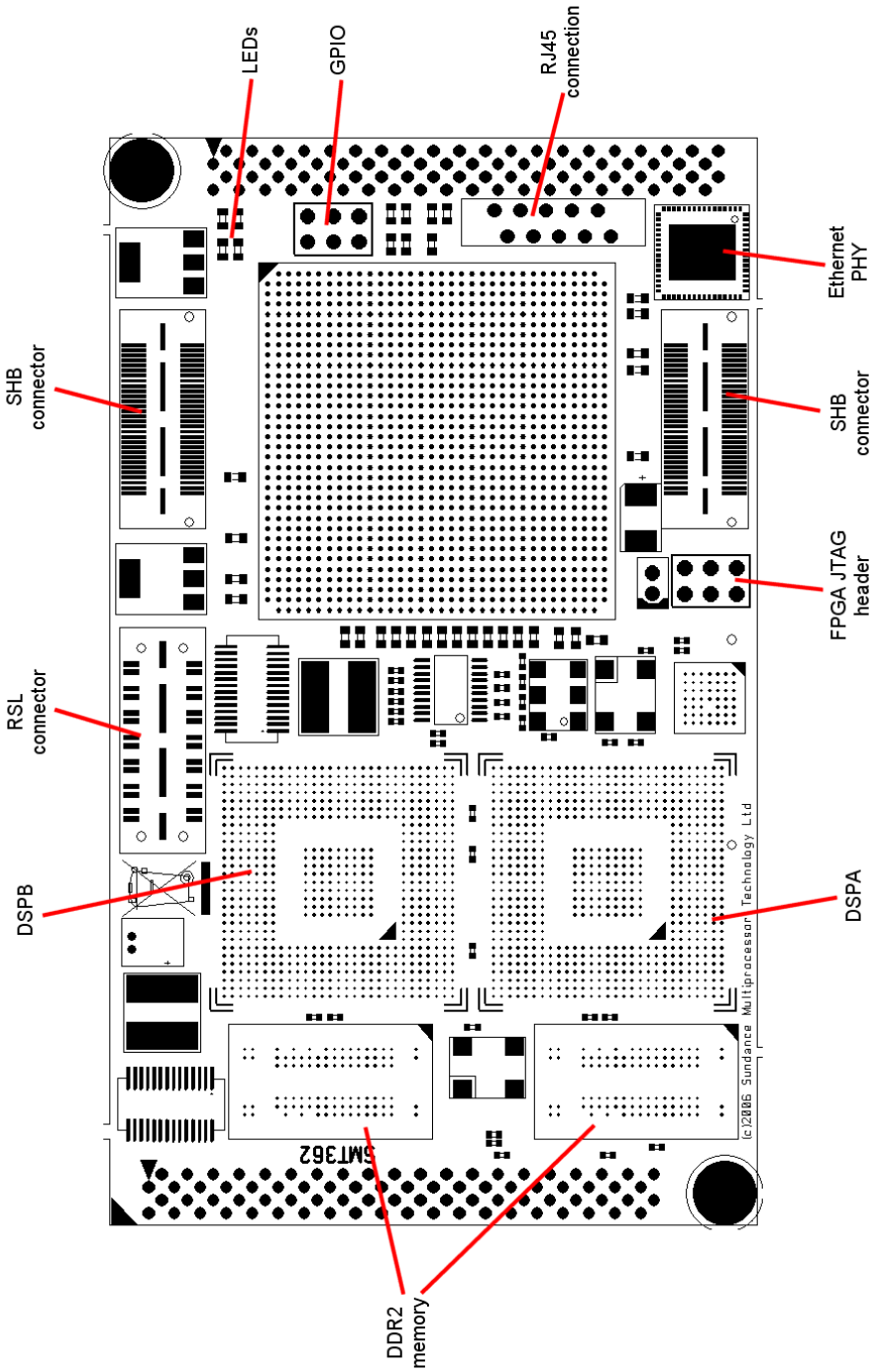
Contained on the module are switching regulators for the ‘C6455s, DDR2 and FPGA.

The RocketIO voltage is provided through a linear regulator from 3.3V.

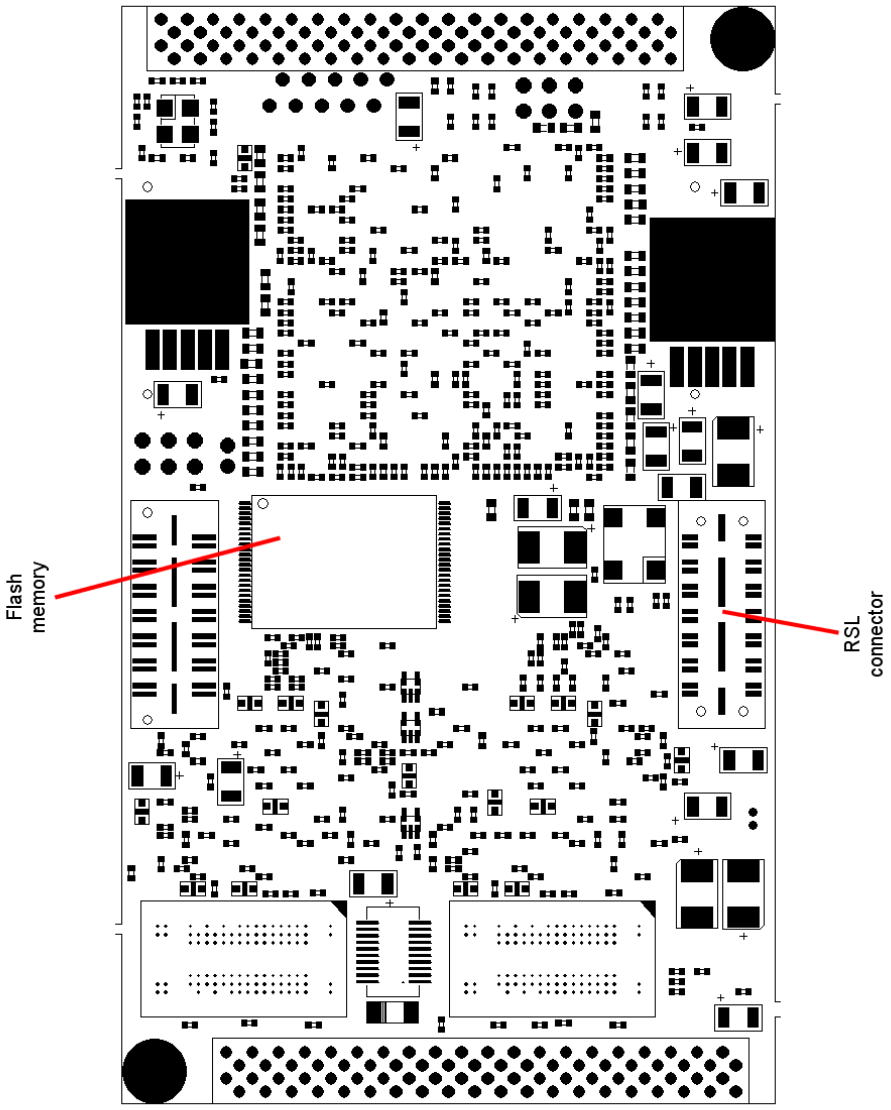
All supplies a guaranteed to meet the worst possible requirements of the FPGAs.

5 Footprint

5.1 Top View



5.2 Bottom View

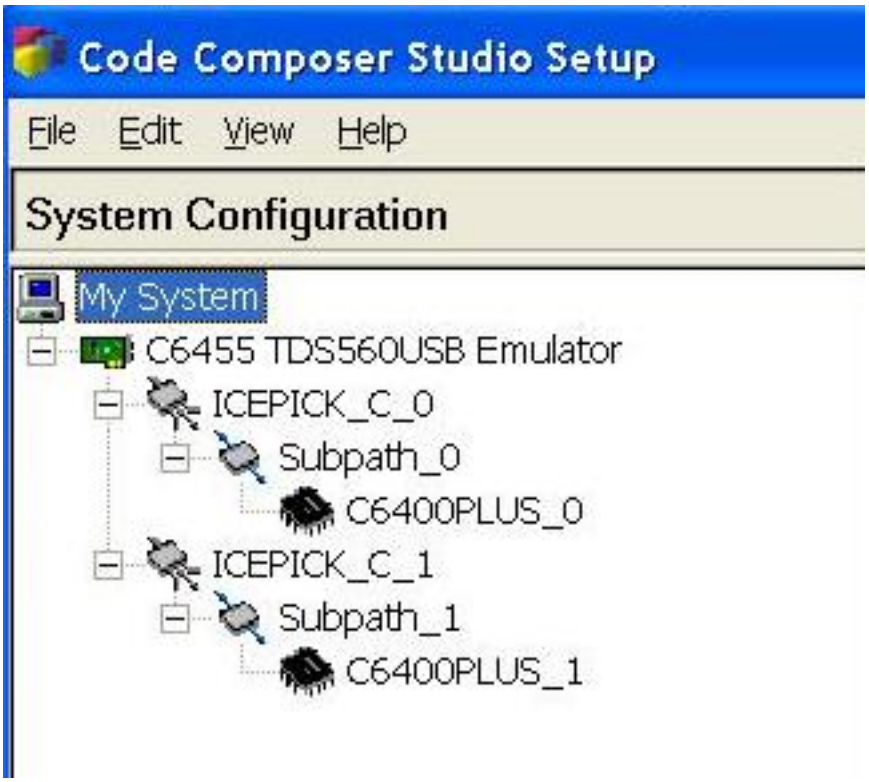


6 Support Packages

6.1 Code Composer Studio

The C6455 is supported under Texas Instrument's Code Composer Studio (http://focus.ti.com/dsp/docs/dspsupporto.tsp?sectionId=3&tabId=453) development tools.

For a single SMT362 system, the Code Composer Setup should show a system similar to this;



Both Subpath ports should be set to the value 0x10.

6.2 3L Diamond

A Diamond processor type is defined. Please consult the relevant 3L documentation.

7 Physical Properties

Dimensions	4.2”	2.5”
Weight		
Supply Voltages	+5, +3.3V	
Supply Current	+12V	0
	+5V	
	+3.3V	
	-5V	0
	-12V	0
MTBF		

8 FPGA Pin-out (ucf)

BOARDCLK	AG17
CP0_DATA<0>	W6
CP0_DATA<1>	W7
CP0_DATA<2>	AA4
CP0_DATA<3>	AA5
CP0_DATA<4>	V7
CP0_DATA<5>	V8
CP0_DATA<6>	W4
CP0_DATA<7>	W5
CP0_RDY	Y4
CP0_REQ	Y7
CP0_ACK	Y3
CP0_STB	Y8
CP1_DATA<0>	K8
CP1_DATA<1>	K9
CP1_DATA<2>	E12
CP1_DATA<3>	E13
CP1_DATA<4>	E6
CP1_DATA<5>	E7
CP1_DATA<6>	H12
CP1_DATA<7>	J12
CP1_RDY	H7
CP1_REQ	G7
CP1_ACK	K11
CP1_STB	L11
CP2_DATA<0>	K7
CP2_DATA<1>	J7
CP2_DATA<2>	G11
CP2_DATA<3>	G12
CP2_DATA<4>	H8
CP2_DATA<5>	G8
CP2_DATA<6>	J10
CP2_DATA<7>	J11

DSPB_EMIF_DATA<21>	AM8
DSPB_EMIF_DATA<22>	AB12
DSPB_EMIF_DATA<23>	AC12
DSPB_EMIF_DATA<24>	AH7
DSPB_EMIF_DATA<25>	AH8
DSPB_EMIF_DATA<26>	AA13
DSPB_EMIF_DATA<27>	AB13
DSPB_EMIF_DATA<28>	AJ7
DSPB_EMIF_DATA<29>	AK7
DSPB_EMIF_DATA<30>	AA11
DSPB_EMIF_DATA<31>	AB11
DSPB_EMIF_DATA<32>	AG5
DSPB_EMIF_DATA<33>	AG6
DSPB_EMIF_DATA<34>	AL6
DSPB_EMIF_DATA<35>	AM6
DSPB_EMIF_DATA<36>	AD6
DSPB_EMIF_DATA<37>	AD7
DSPB_EMIF_DATA<38>	AG7
DSPB_EMIF_DATA<39>	AG8
DSPB_EMIF_DATA<40>	AL3
DSPB_EMIF_DATA<41>	AM3
DSPB_EMIF_DATA<42>	AJ6
DSPB_EMIF_DATA<43>	AK6
DSPB_EMIF_DATA<44>	AH3
DSPB_EMIF_DATA<45>	AH4
DSPB_EMIF_DATA<46>	AE7
DSPB_EMIF_DATA<47>	AF8
DSPB_EMIF_DATA<48>	AF4
DSPB_EMIF_DATA<49>	AF5
DSPB_EMIF_DATA<50>	AK4
DSPB_EMIF_DATA<51>	AL4
DSPB_EMIF_DATA<52>	AB8
DSPB_EMIF_DATA<53>	AC7

CP2_RDY	F8
CP2_REQ	E8
CP2_ACK	C13
CP2_STB	C12
CP3_DATA<0>	W24
CP3_DATA<1>	W25
CP3_DATA<2>	U30
CP3_DATA<3>	V30
CP3_DATA<4>	U31
CP3_DATA<5>	U32
CP3_DATA<6>	V28
CP3_DATA<7>	V29
CP3_RDY	W26
CP3_REQ	V32
CP3_ACK	Y26
CP3_STB	W32
CP4_DATA<0>	C3
CP4_DATA<1>	C4
CP4_DATA<2>	M11
CP4_DATA<3>	M12
CP4_DATA<4>	E3
CP4_DATA<5>	E4
CP4_DATA<6>	L13
CP4_DATA<7>	M13
CP4_RDY	D4
CP4_REQ	D5
CP4_ACK	K13
CP4_STB	K12
CP5_DATA<0>	C5
CP5_DATA<1>	D6
CP5_DATA<2>	D15
CP5_DATA<3>	D16
CP5_DATA<4>	G6
CP5_DATA<5>	F6
CP5_DATA<6>	C14
CP5_DATA<7>	C15

DSPB_EMIF_DATA<54>	AL5
DSPB_EMIF_DATA<55>	AM5
DSPB_EMIF_DATA<56>	AE3
DSPB_EMIF_DATA<57>	AE4
DSPB_EMIF_DATA<58>	AK3
DSPB_EMIF_DATA<59>	AJ4
DSPB_EMIF_DATA<60>	AD4
DSPB_EMIF_DATA<61>	AD5
DSPB_EMIF_DATA<62>	AE6
DSPB_EMIF_DATA<63>	AF6
DSPB_GPIO_12	AA8
DSPB_GPIO_13	AA9
DSPB_GPIO_2	AC4
DSPB_GPIO_CLKR1	Y9
DSPB_GPIO_CLKX1	W9
DSPB_GPIO_DR1	AF3
DSPB_GPIO_DX1	AG3
DSPB_GPIO_FSR1	Y6
DSPB_GPIO_FSX1	AA6
MCBSPBCLKS	AC5
DSPB_INTS<0>	AB6
DSPB_INTS<1>	AK19
DSPB_INTS<2>	AJ19
DSPB_INTS<3>	AJ20
DSPB_INTS<4>	AJ21
DSPB_TIMER0<0>	AB7
DSPB_TIMER0<1>	AA3
DSPB_TIMER1<0>	AB3
DSPB_TIMER1<1>	AB5
DSPA_MDC	M23
DSPA_MDIO	N23
DSPA_RGMII_GREFCLK	J14
DSPA_RX_CTL	L25
DSPA_RXC	L15
DSPA_RXD<0>	N24
DSPA_RXD<1>	P24

CP5_RDY	D7
CP5_REQ	C7
CP5_ACK	E14
CP5_STB	D14
DSPA_EMIF_ADDR<0>	AJ25
DSPA_EMIF_ADDR<1>	AJ26
DSPA_EMIF_ADDR<2>	AF24
DSPA_EMIF_ADDR<3>	AF25
DSPA_EMIF_ADDR<4>	AM26
DSPA_EMIF_ADDR<5>	AL26
DSPA_EMIF_ADDR<6>	AH25
DSPA_EMIF_ADDR<7>	AG25
DSPA_EMIF_ADDR<8>	AE24
DSPA_EMIF_ADDR<9>	AD24
DSPA_EMIF_ADDR<10>	AG26
DSPA_EMIF_ADDR<11>	AF26
DSPA_EMIF_ADDR<12>	AM25
DSPA_EMIF_ADDR<13>	AL25
DSPA_EMIF_ADDR<14>	AJ27
DSPA_EMIF_ADDR<15>	AH27
DSPA_EMIF_ADDR<16>	AH24
DSPA_EMIF_ADDR<17>	AJ24
DSPA_EMIF_ADDR<18>	AK26
DSPA_EMIF_ADDR<19>	AK27
DSPA_EMIF_BE<0>	AK24
DSPA_EMIF_BE<1>	AL24
DSPA_EMIF_BE<2>	AE26
DSPA_EMIF_BE<3>	AE27
DSPA_EMIF_BE<4>	AJ30
DSPA_EMIF_BE<5>	AH30
DSPA_EMIF_BE<6>	AG30
DSPA_EMIF_BE<7>	AG31
DSPA_EMIF_CLK	AF20
DSPA_EMIF_CTRL<0>	AE23
DSPA_EMIF_CTRL<1>	AF23
DSPA_EMIF_CTRL<2>	AF28

DSPA_RXD<2>	N22
DSPA_RXD<3>	P22
DSPA_TX_CTL	E28
DSPA_TXC	L21
DSPA_TXD<0>	L24
DSPA_TXD<1>	K24
DSPA_TXD<2>	F19
DSPA_TXD<3>	E19
DSPB_MDC	F28
DSPB_MDIO	G20
DSPB_RGMII_GREFCLK	J16
DSPB_RX_CTL	L26
DSPB_RXC	H17
DSPB_RXD<0>	F20
DSPB_RXD<1>	J20
DSPB_RXD<2>	H20
DSPB_RXD<3>	C27
DSPB_TX_CTL	D21
DSPB_TXC	C28
DSPB_TXD<0>	K23
DSPB_TXD<1>	D27
DSPB_TXD<2>	E27
DSPB_TXD<3>	E21
LED<0>	J9
LED<1>	H9
LED<2>	F9
LED<3>	F10
LED<4>	C10
LED<5>	D10
LED<6>	H10
LED<7>	G10
PXI_CLK	AD21
PXI_TRIG1	E9
PXI_TRIG2	D9
PXI_TRIG3	E11
PXI_TRIG4	F11

DSPA_EMIF_CTRL<3>	AE28
DSPA_EMIF_CTRL<4>	AG23
DSPA_EMIF_CTRL<5>	AH23
DSPA_EMIF_CTRL<6>	AG27
DSPA_EMIF_CTRL<7>	AG28
DSPA_EMIF_DATA<0>	AK22
DSPA_EMIF_DATA<1>	AK23
DSPA_EMIF_DATA<2>	AL28
DSPA_EMIF_DATA<3>	AK28
DSPA_EMIF_DATA<4>	AL23
DSPA_EMIF_DATA<5>	AM23
DSPA_EMIF_DATA<6>	AM27
DSPA_EMIF_DATA<7>	AM28
DSPA_EMIF_DATA<8>	AD22
DSPA_EMIF_DATA<9>	AE22
DSPA_EMIF_DATA<10>	AH28
DSPA_EMIF_DATA<11>	AH29
DSPA_EMIF_DATA<12>	AM21
DSPA_EMIF_DATA<13>	AM22
DSPA_EMIF_DATA<14>	AK29
DSPA_EMIF_DATA<15>	AJ29
DSPA_EMIF_DATA<16>	AK21
DSPA_EMIF_DATA<17>	AL21
DSPA_EMIF_DATA<18>	AL29
DSPA_EMIF_DATA<19>	AM30
DSPA_EMIF_DATA<20>	AL20
DSPA_EMIF_DATA<21>	AM20
DSPA_EMIF_DATA<22>	AL30
DSPA_EMIF_DATA<23>	AL31
DSPA_EMIF_DATA<24>	AC22
DSPA_EMIF_DATA<25>	AC23
DSPA_EMIF_DATA<26>	AM31
DSPA_EMIF_DATA<27>	AM32
DSPA_EMIF_DATA<28>	AL18
DSPA_EMIF_DATA<29>	AL19
DSPA_EMIF_DATA<30>	AK31

RESET	AG18

RGMII_COMA	J22
RGMII_MDC	K26
RGMII_MDIO	G21
RGMII_RESETB	F21
RGMII_RX_CTL_0	D25
RGMII_RXC_0	K18
RGMII_RXD_0<0>	D26
RGMII_RXD_0<1>	E26
RGMII_RXD_0<2>	K21
RGMII_RXD_0<3>	J21
RGMII_TX_CTL_0	C24
RGMII_TXC_0	D22
RGMII_TXD_0<0>	G25
RGMII_TXD_0<1>	H22
RGMII_TXD_0<2>	G22
RGMII_TXD_0<3>	H25

SHBA_ACK1	L28
SHBA_ACK4	L29
SHBA_CLK0	P30
SHBA_CLK3	P32
SHBA_D0<0>	U27
SHBA_D0<1>	U28
SHBB_CLK0	V5
SHBB_CLK3	T6
SHBB_D0<0>	U6
SHBB_D0<1>	U7
SHBB_D0<2>	T10
SHBB_D0<3>	T11
SHBB_D0<4>	V3
SHBB_D0<5>	V4
SHBB_D0<6>	R9
SHBB_D0<7>	T9
SHBB_D0<8>	R7

DSPA_EMIF_DATA<31>	AK32
DSPA_EMIF_DATA<32>	AJ31
DSPA_EMIF_DATA<33>	AJ32
DSPA_EMIF_DATA<34>	AF29
DSPA_EMIF_DATA<35>	AE29
DSPA_EMIF_DATA<36>	AD25
DSPA_EMIF_DATA<37>	AC25
DSPA_EMIF_DATA<38>	AF30
DSPA_EMIF_DATA<39>	AF31
DSPA_EMIF_DATA<40>	AD26
DSPA_EMIF_DATA<41>	AD27
DSPA_EMIF_DATA<42>	AE31
DSPA_EMIF_DATA<43>	AE32
DSPA_EMIF_DATA<44>	AH32
DSPA_EMIF_DATA<45>	AG32
DSPA_EMIF_DATA<46>	AC27
DSPA_EMIF_DATA<47>	AC28
DSPA_EMIF_DATA<48>	AD29
DSPA_EMIF_DATA<49>	AD30
DSPA_EMIF_DATA<50>	AD31
DSPA_EMIF_DATA<51>	AD32
DSPA_EMIF_DATA<52>	AB25
DSPA_EMIF_DATA<53>	AB26
DSPA_EMIF_DATA<54>	AB27
DSPA_EMIF_DATA<55>	AB28
DSPA_EMIF_DATA<56>	AC29
DSPA_EMIF_DATA<57>	AC30
DSPA_EMIF_DATA<58>	AA25
DSPA_EMIF_DATA<59>	AA26
DSPA_EMIF_DATA<60>	AB30
DSPA_EMIF_DATA<61>	AB31
DSPA_EMIF_DATA<62>	AA28
DSPA_EMIF_DATA<63>	AA29
DSPA_GPIO_CLKR1	AC32
DSPA_GPIO_CLKX1	AB32
DSPA_GPIO_DR1	AA30

SHBA_D0<2>	R26
SHBA_D0<3>	T26
SHBA_D0<4>	T28
SHBA_D0<5>	T29
SHBA_D0<6>	T30
SHBA_D0<7>	T31
SHBA_D0<8>	R27
SHBA_D0<9>	R28
SHBA_D0<10>	P29
SHBA_D0<11>	R29
SHBA_D0<12>	R31
SHBA_D0<13>	R32
SHBA_D0<14>	N32
SHBA_D0<15>	P26
SHBA_D1<0>	M31
SHBA_D1<1>	M32
SHBA_D1<2>	M30
SHBA_D1<3>	N30
SHBA_D1<4>	M28
SHBA_D1<5>	N27
SHBA_D1<6>	N28
SHBA_D1<7>	N29
SHBA_D1<8>	H32
SHBA_D1<9>	J32
SHBA_D1<10>	L30
SHBA_D1<11>	L31
SHBA_D1<12>	M25
SHBA_D1<13>	M26
SHBA_D1<14>	K31
SHBA_D1<15>	K32
SHBA_REQ1	H29
SHBA_REQ4	H30
SHBA_WEN1	P31
SHBA_WEN4	P27
SHBB_ACK1	L5
SHBB_ACK4	L6

DSPA_GPIO_DX1	AA31
DSPA_GPIO_FSR1	AA24
DSPA_GPIO_FSX1	Y24
MCBSPACLKS	28
DSPA_HINT	AK18
DSPA_INTS<0>	Y27
DSPA_INTS<1>	AH18
DSPA_INTS<2>	AH19
DSPA_INTS<3>	AH20
DSPA_INTS<4>	AG20
DSPA_TIMER0<0>	W31
DSPA_TIMER0<1>	V27
DSPA_TIMER1<0>	W27
DSPA_TIMER1<1>	W29
DSPB_EMIF_ADDR<0>	AL13
DSPB_EMIF_ADDR<1>	AK13
DSPB_EMIF_ADDR<2>	AL14
DSPB_EMIF_ADDR<3>	AK14
DSPB_EMIF_ADDR<4>	AM12
DSPB_EMIF_ADDR<5>	AM13
DSPB_EMIF_ADDR<6>	AH12
DSPB_EMIF_ADDR<7>	AG12
DSPB_EMIF_ADDR<8>	AE9
DSPB_EMIF_ADDR<9>	AF9
DSPB_EMIF_ADDR<10>	AG11
DSPB_EMIF_ADDR<11>	AF11
DSPB_EMIF_ADDR<12>	AK12
DSPB_EMIF_ADDR<13>	AJ12
DSPB_EMIF_ADDR<14>	AH13
DSPB_EMIF_ADDR<15>	AG13
DSPB_EMIF_ADDR<16>	AK11
DSPB_EMIF_ADDR<17>	AJ11
DSPB_EMIF_ADDR<18>	AJ14
DSPB_EMIF_ADDR<19>	AH14
DSPB_EMIF_BE<0>	AM11
DSPB_EMIF_BE<1>	AL11

SHBB_D0<9>	R8
SHBB_D0<10>	T8
SHBB_D0<11>	U8
SHBB_D0<12>	T3
SHBB_D0<13>	U3
SHBB_D0<14>	U5
SHBB_D0<15>	R6
SHBB_D1<0>	P6
SHBB_D1<1>	P7
SHBB_D1<2>	T4
SHBB_D1<3>	T5
SHBB_D1<4>	R3
SHBB_D1<5>	R4
SHBB_D1<6>	P9
SHBB_D1<7>	P10
SHBB_D1<8>	P4
SHBB_D1<9>	P5
SHBB_D1<10>	N4
SHBB_D1<11>	N5
SHBB_D1<12>	N3
SHBB_D1<13>	M3
SHBB_D1<14>	M5
SHBB_D1<15>	M6
SHBB_REQ1	L3
SHBB_REQ4	L4
SHBB_WEN1	R11
SHBB_WEN4	P11

TIM_CONFIG	C8
TIM_NMI	C9
TIM_TIMER0	D11
TIM_TIMER1	D12
TIMIACK	AK17

DSPB_EMIF_BE<2>	AJ15
DSPB_EMIF_BE<3>	AH15
DSPB_EMIF_BE<4>	AH5
DSPB_EMIF_BE<5>	AJ5
DSPB_EMIF_BE<6>	AC9
DSPB_EMIF_BE<7>	AC10
DSPB_EMIF_CLK	AF16
DSPB_EMIF_CTRL<0>	AG10
DSPB_EMIF_CTRL<1>	AF10
DSPB_EMIF_CTRL<2>	AK16
DSPB_EMIF_CTRL<3>	AJ16
DSPB_EMIF_CTRL<4>	AJ10
DSPB_EMIF_CTRL<5>	AH10
DSPB_EMIF_CTRL<6>	AG15
DSPB_EMIF_CTRL<7>	AF15
DSPB_EMIF_DATA<0>	AM10
DSPB_EMIF_DATA<1>	AL10
DSPB_EMIF_DATA<2>	AF13
DSPB_EMIF_DATA<3>	AE13
DSPB_EMIF_DATA<4>	AH9
DSPB_EMIF_DATA<5>	AJ9
DSPB_EMIF_DATA<6>	AF14
DSPB_EMIF_DATA<7>	AE14
DSPB_EMIF_DATA<8>	AD9
DSPB_EMIF_DATA<9>	AD10
DSPB_EMIF_DATA<10>	AE11
DSPB_EMIF_DATA<11>	AD11
DSPB_EMIF_DATA<12>	AK9
DSPB_EMIF_DATA<13>	AL9
DSPB_EMIF_DATA<14>	AE12
DSPB_EMIF_DATA<15>	AD12
DSPB_EMIF_DATA<16>	AK8
DSPB_EMIF_DATA<17>	AL8
DSPB_EMIF_DATA<18>	AC13
DSPB_EMIF_DATA<19>	AD14
DSPB_EMIF_DATA<20>	AM7

9 Safety

This module presents no hazard to the user when in normal use.

10 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.