Sundance Multiprocessor Technology Limited **Design Specification**	Form : QCF51 Dated : 20 December 2001 Revision : 5.1 Approved : Mark Ainsworth

Unit / Module Name:	Quad 14-bit ADC – 105MSPS
Unit / Module Number:	SMT364
Used On:	SMT320, SMT310Q, SMT327, SMT300Q
Document Issue:	1.6
Date:	

CONFIDENTIAL

Approvals		Date
Managing Director		
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Certificate Number FM 55022

Revision History

	Changes Made	Issue	Initials
21/05/02	First release	1.0	PSR
11/06/02	Main feature table completed	1.1	PSR
17/06/02	Description of the AD6645 added	1.2	PSR
11/11/02	XC17v04 replaced by XC18v04	1.3	PSR
31/03/03	Power supply reviewed and modified; Block diagram updated; FPGA pinout modified.	1.4	PSR
28/04/03	CommPort 1 and 4 added; JTAG pinout corrected; micro-switch removed	1.5	PSR
02/07/03	PCB Layout modified; FPGA speed grade changed to –4; Input and Output characteristics detailed; CommPort 4 set as default control word CommPort.	1.6	PSR

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1 Introduction

1.1 Overview

The *SMT364* is a single width TIM, which converts up to 4 analogue signals into 14-bit digital data flows, using four Analog Devices AD6645s.

They are 5 Volts devices, 14-bit data and able to output samples at up to 105 MSPS.

Digital data is output to a Xilinx Virtex-II FPGA (XC2V1000-4 FG456), which controls transfers via CommPorts and **S**undance **H**igh-speed **B**us (*SHB*). These buses are compatible with a wide range of Sundance processor and I/O modules. 4 Communication ports and 2 SHB are available on the board.

An on-board In-System Programmable Configuration XC18V04 Xilinx PROM loads into the FPGA a configuration at start-up. The user has access to it via the JTAG connector and can reconfigure it.

Configuration, sampling and transferring modes are set via internal control register.

1.2 Related Documents

AD6645 Datasheet - Analog Devices:

http://www.analog.com/productselection/descriptions/AD6645.html

Sundance **H**igh-speed **B**us (*SHB*) specifications – Sundance.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification_v1_0.pdf

TIM specifications.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf

Xilinx Virtex-II FPGA.

http://www.xilinx.com/partinfo/ds031.pdf

2 Functional Description

In this part, we will see the general block diagram and some comments on each of its entities.

2.1 Block Diagram

The following picture shows the block diagram of the *SMT364*.

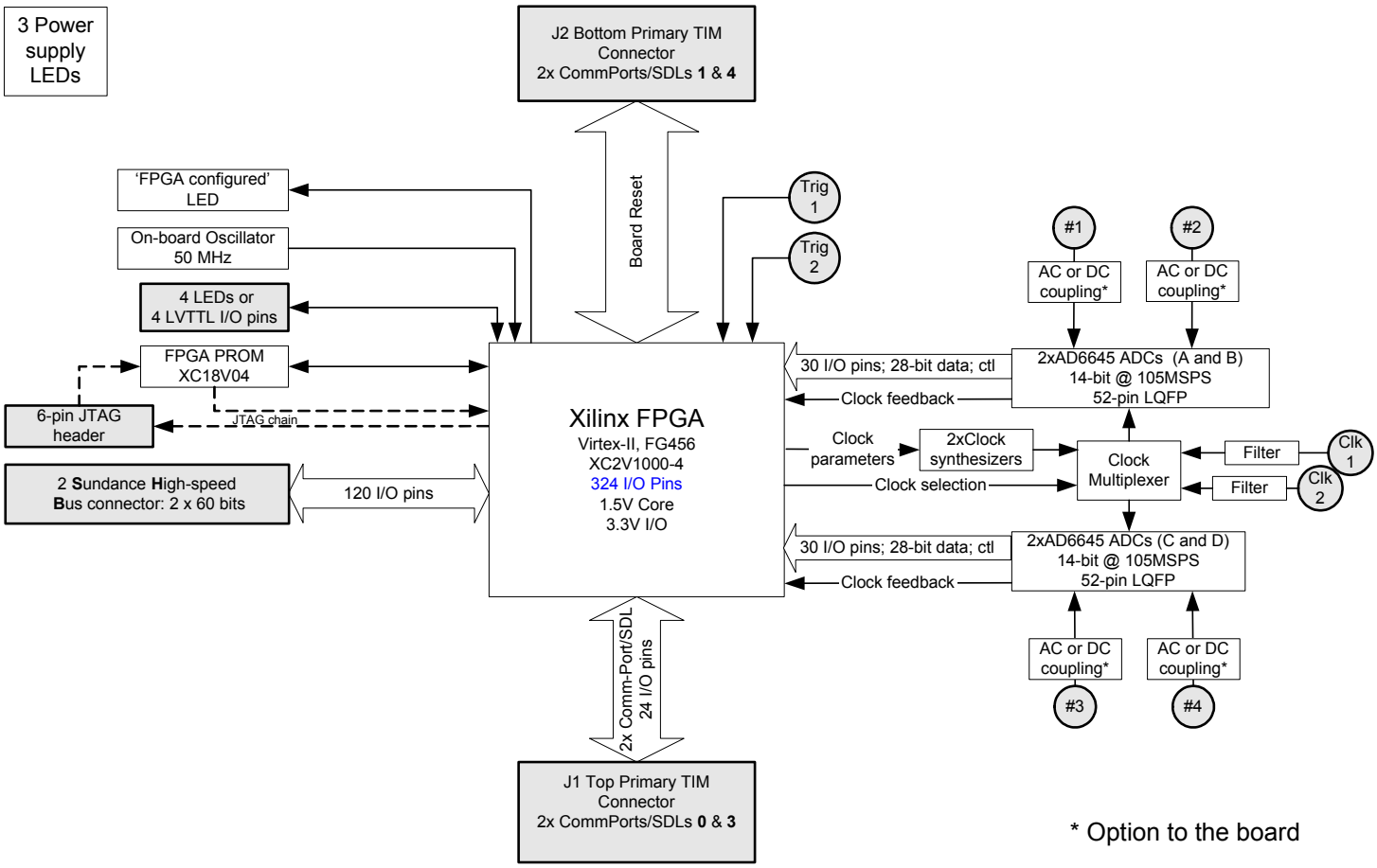

Figure 1 - General block diagram.

Connections to the outside world are greyed out.

Main parts of the board are described in the next part of this document.

2.2 Inputs and outputs main characteristics.

The main features of the *SMT364* are gathered into the following table.

Analogue inputs	
Input voltage range	● 1.1 Volts peak-to-peak (AC coupling). ● 2.2 Volts peak-to-peak (DC coupling – Gain 1). (Specify ADC coupling when placing an order)
Impedance	50Ω
Bandwidth	● No anti-aliasing filter on the board. It is to the user to set one up if required. ● Input transformers (AC option): 2-775 MHz. ● Input opamps (DC option): 0-320 MHz ● A-to-D converters: 0-250 MHz.
External sampling clock inputs	
Minimum voltage	● 0.2V p-p ● 3.3 Volts maximum ● -3.3 Volts minimum
Impedance	50Ω
Frequency range	30MHz to 105MHz
External Trigger inputs	
Frequency range	30 to 105MHz
Signal format	LVTTL (3.3 Volts) format – connected to 3.3V FPGA – Clamp diodes to 3.3V and Ground.
***SMT364* Output**	
ADC Resolution	14-Bits
Output Data Format	Binary or 16-bit extended two's complement.
SFDR	Up to 70dB
SNR	Up to 80dB
Maximum Sampling Frequency	105MHz

Figure 2 - Main features.

2.3 Module Description

The module mainly consists of a Xilinx Virtex-II FPGA and four Analog Devices AD6645 14-bit monolithic sampling analog-to-digital converters. The chip provides CMOS-compatible

digital outputs. It is the Analog Devices' fourth generation of wideband ADCs. The *AD6645* maintains 100dB multi-tone, spurious-free dynamic range (SFDR) through the second Nyquist band. Its typical signal-to-noise ratio is 74.5dB through the first Nyquist band.

The *AD6645* maintains outstanding AC performance up to input frequencies of 200 MHz, which makes it suitable for multi-carrier 3G applications.

A parallel bus connects ADCs to the FPGA, which is responsible for transferring the output samples (2's complement or binary format). The FPGA feeds the ADCs with a differential encode via clock multiplexer, which allows the selection between on-board or external clock for full performance operation. Each analogue input signal goes through an input stage (AC coupling i.e. RF Transformer or DC coupling i.e. opamp – on option). ADCs are coupled by pairs. Each couple can run independently, i.e. they have their own sampling clock (on-board from clock synthesizer or external) and enable (internal via control register or external trigger) signals. Clock, trigger and analogue input signals are all single-ended and 50-Ohm terminated.

The Xilinx FPGA Virtex-II is configured via a 6-pin JTAG header or from the on-board Xilinx PROM (XC18V04) at startup. The default configuration mode is from an In-system PROM, which contains the standard modes of operation (as described in this document).

Four LEDs can be driven by the FPGA. Extra signals can be mapped or externally connected to the 4-pin header. They are all directly connected to the FPGA. Care must be taken when connecting incoming signals to this header.

Two full (60-pin) *SHB* connectors are available from the FPGA. They are to be set as output only to send out digital samples to an other module. Please refer to the SHB specifications for more details about ways connectors can be configured.

Four Communication (CommPort0, 1, 3 and 4) links following the Texas Instrument C4x standard are connected to the FPGA and will be used to receive control words. By default, CommPort 4 is used for sending control words.

A global reset signal is mapped to the FPGA from the top TIM connector.

2.4 Interface Description

2.4.1 Mechanical Interface

2.4.1.1 EMI protection.

This module is provided with an EMI box, which avoids unwanted generation or reception of interferences from and to the analogue part of the board.

2.4.1.2 3.3 Volts power supply.

This module conforms to the TIM standard for single with modules. It requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards), which must be provided by the two diagonally opposite mounting holes.

2.4.1.3 Analogue connectors.

Analogue external signals are all connected to the *SMT364* via MMBX connectors.

Surface mount connectors are used for each MMBX, i.e. external clock, triggering and analogue signal inputs. The external trigger connector has got clamp diodes (on Vcc and Gnd) to avoid high voltage to damage the FPGA.

A cable holder could be used to maintain all the external cables coming on the board. It could be attached to the PCB.

2.4.1.4 Digital connectors and cables.

2.4.1.4.1 Electric fan.

A fan (ARX Ball Bearing Cooler – BP0535SA7-1) on the ADCs is required to cool them down. It can be connected to a 5-Volt 2-pin Molex right angle connector, or any other external 5-Volt source. The *SMT364* is mounted in factory with a fan.

2.4.1.4.2 SHB.

The *SMT364* includes two 60-pin connectors to send sampled data out to another TIM module. All the pins are directly connected to the Virtex-II FPGA.

Samtec manufactures the on-board connectors. It is a high-speed socket strip: QSH-030-01-L-D-A-K. Both connectors are identical and have a centreline of 0.5mm (0.0197").

The external *SHB* cables are custom made by *Precision Interconnect* and a cable assembly solution builder can be found at: http://www.precisionint.com/tdibrsb/content/howtouse.asp. They are micro-coax cables and can achieve high-speed data transfer between TIM modules. As a result, no differential lines are required to transfer data on long distance and at up to 100Mhz, which allows the full use of the *SHB* 60-pin connectors.

2.4.1.4.3 TTL I/Os.

The *SMT364* has a 6-pin header (0.1") connected to the FPGA. It is composed of one Ground, one Vcc and 4 TTL signals connected directly to the FPGA.

2.4.1.5 Configuration connector.

The *SMT364* includes a 6-pin JTAG header (2mm DIL header), which allows reconfiguring the FPGA and re-programming the PROM from an external cable such as Xilinx Parallel III or Parallel IV cables.

Here is the pinout of the 6-pin JTAG header:

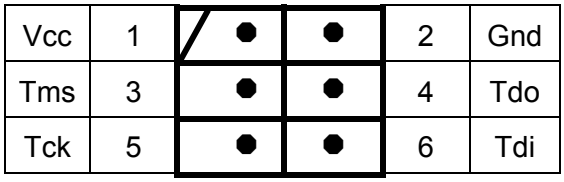

Figure 3 - JTAG Header pinout.

2.4.1.6 On-board oscillator.

The on-board oscillator is 50 MHz. It is only used to synchronise interfaces (CommPort, SHB, memory and converters) implemented into the FPGA. Internal DLLs are used to generate appropriate clock rates.

2.4.1.7 On-Board Clock Synthesizers.

A dedicated frequency synthesiser (ICS8432-01) is used to generate a low jitter clock to feed into the converters. It is important to have a high-quality clock to get good sampling results. The minimum frequency that this frequency synthesizer can generate is 20.83 MHz.

The clock synthesizer is followed by a clock multiplexer (ICS85356), which has negligible jitter.

2.4.2 Electrical Interface

The board consists of 4 fast ADCs. Each channel is connected to the FPGA via a parallel bus. The Virtex-II controls every single operation related to the ADCs. It also manages output data transfers onto both *SHBs*.

2.4.2.1 CommPort interface.

CommPorts (Communication ports) links follow Texas Instrument C4x standard. They are 8-bit parallel inter-processor ports of the 'C4x processors.

The *SMT364* provides 4 links. These are given the numbers 0, 1, 3 and 4. In the default firmware, CommPort 4 is dedicated for receiving control words.

The CommPorts drive at 3.3v signal levels.

The FPGA can implement up to three FIFO buffered CommPort interfaces fully compliant with the TIM standard. They are guaranteed for a transfer rate of 20MB/s.

The FIFOs are useful to maintain a maximum bandwidth and to enable parallel transfers.

Therefore, as an example, each CommPort can be associated with two 15x32-bit unidirectional FIFOs; one for input and one for output. An additional one-word buffer makes them appear as 16x32-bit FIFOs.

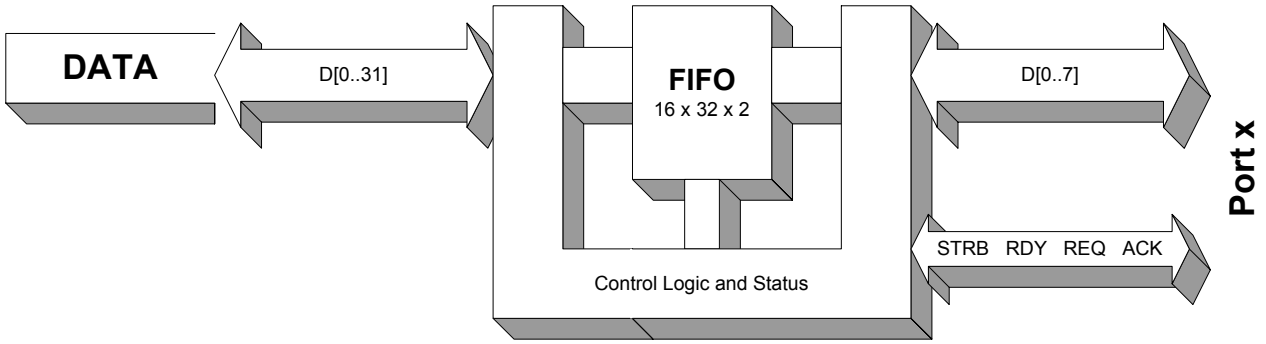

Figure 4 - CommPort interface data path.

Control words can be loaded via only one CommPort; the one selected using the on-board jumpers.

2.4.2.2 *SHB* interface.

Both *SHB* buses are identical and 60-bit wide.

SHBs are parallel communication links for synchronous transmissions. Each *SHB* can be divided into five independent 8-bit buses. Each 8-bit bus includes a clock and three control signals: write enable, request and acknowledge. An *SHB* bus can also be divided into two 16-bit buses and one 8-bit bus.

Here is the architecture of the *SHB* interface implemented into the FPGA:

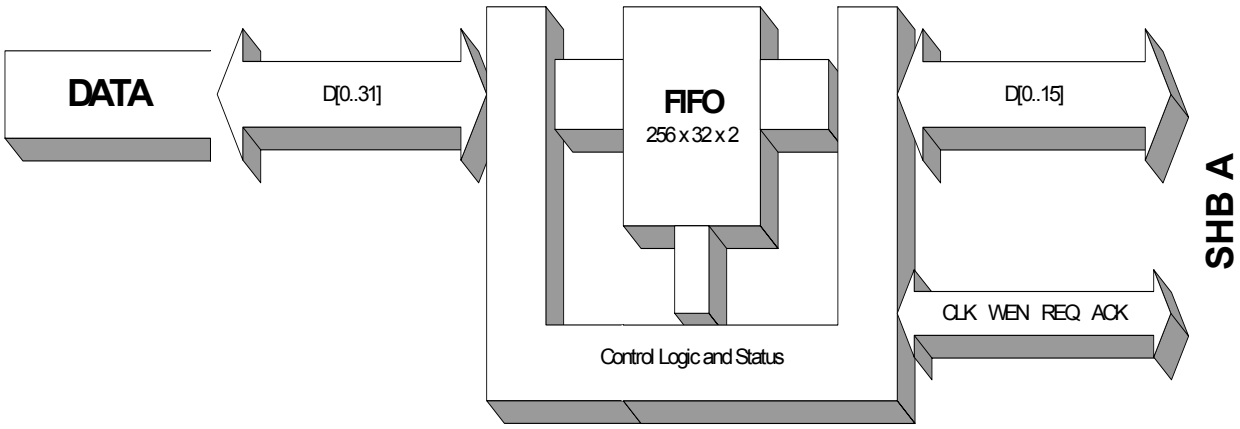

Figure 9 - *SHB* interface structure.

On the *SMT364*, both SHB connector are linked to a pair of ADCs: SHBA connector carries samples coming from ADC A and B and SHBB carries samples coming from ADC C and D.

2.4.2.3 ADC interface.

The Virtex-II FPGA generates signals to drive both Analogue-to-Digital converters, depending on the control words received. It manages sampling clock and triggering signals; both can be internal or single-ended external.

The default sample format is binary.

There are two clock synthesizers (one for each pair of channels: AB and CD), which are loaded and controlled by the FPGA, is charge of generating low-jitter sampling clocks.

Changes take place as soon as a new control word is being received.

2.4.2.4 Control words format.

As said previously, there are four ADCs on the board, coupled by pairs. Each couple is independent and named either ChannelA&B or ChannelC&D.

Bit number	Description
Bit 31	0
Bit 30	0
Bit 29	0
Bit 28	0
Bit 27-26	
Bit 25	Clock Selection ADC-CD (‘0’=Internal; ‘1’=External)
Bit 24	Clock Selection ADC-AB (‘0’=Internal; ‘1’=External)
Bit 23	Clock synthesizer – N (divider) Bit2 – ADC-CD
Bit 22	Clock synthesizer – N (divider) Bit1 – ADC-CD
Bit 21	Clock synthesizer – N (divider) Bit0 – ADC-CD
Bit 20	Clock synthesizer - M Bit8 – ADC-CD
Bit 19	Clock synthesizer – M Bit7 – ADC-CD
Bit 18	Clock synthesizer - M Bit6 – ADC-CD
Bit 17	Clock synthesizer - M Bit5 – ADC-CD
Bit 16	Clock synthesizer - M Bit4 – ADC-CD
Bit 15	Clock synthesizer - M Bit3 – ADC-CD
Bit 14	Clock synthesizer - M Bit2 – ADC-CD
Bit 13	Clock synthesizer - M Bit1 – ADC-CD
Bit 12	Clock synthesizer - M Bit0 – ADC-CD
Bit 11	Clock synthesizer – N (divider) Bit2 - ADC-AB
Bit 10	Clock synthesizer – N (divider) Bit1 - ADC-AB
Bit 9	Clock synthesizer – N (divider) Bit0 - ADC-AB
Bit 8	Clock synthesizer - M Bit8 – ADC-AB
Bit 7	Clock synthesizer - M Bit7 – ADC-AB
Bit 6	Clock synthesizer - M Bit6 – ADC-AB
Bit 5	Clock synthesizer - M Bit5 – ADC-AB
Bit 4	Clock synthesizer - M Bit4 – ADC-AB
Bit 3	Clock synthesizer - M Bit3 – ADC-AB
Bit 2	Clock synthesizer - M Bit2 – ADC-AB
Bit 1	Clock synthesizer - M Bit1 – ADC-AB
Bit 0	Clock synthesizer - M Bit0 – ADC-AB

Figure 5 - Control Word 0x0.

Bit number	Description
Bit 31	0
Bit 30	0
Bit 29	0
Bit 28	1
Bit 27	
Bit 26	
Bit 25	
Bit 24	Decimation Factor ADC-CD – Bit 4
Bit 23	Decimation Factor ADC-CD – Bit 3
Bit 22	Decimation Factor ADC-CD – Bit 2
Bit 21	Decimation Factor ADC-CD – Bit 1
Bit 20	Decimation Factor ADC-CD – Bit 0
Bit 17-19	
Bit 16	Decimation Factor ADC-AB – Bit 4
Bit 15	Decimation Factor ADC-AB – Bit 3
Bit 14	Decimation Factor ADC-AB – Bit 2
Bit 13	Decimation Factor ADC-AB – Bit 1
Bit 12	Decimation Factor ADC-AB – Bit 0
Bit 11	ADC-CD External Trigger Level (‘0’=Active low; ‘1’=Active high)
Bit 10	ADC-CD External Trigger Enable (‘0’=External Trigger Disabled; ‘1’=Enabled)
Bit 9	ADC-AB External Trigger Level (‘0’=Active low; ‘1’=Active high)
Bit 8	ADC-AB External Trigger Enable (‘0’=External Trigger Disabled; ‘1’=Enabled)
Bit 7	
Bit 6	ADC-CD Selection Enable – Bit 2.
Bit 5	ADC-CD Selection Enable – Bit 1.
Bit 4	ADC-CD Selection Enable – Bit 0.
Bit 3	
Bit 2	ADC-AB Selection Enable – Bit 2.
Bit 1	ADC-AB Selection Enable – Bit 1.
Bit 0	ADC-AB Selection Enable – Bit 0.

Figure 6 - Control word 0x1.

Note1: Bits0-2 and bits4-6 select the output sample format: 2’s complement, binary or counter.

Control words can be received by any of the available CommPorts.

2.4.2.5 Power supplies.

Devices fitted on the *SMT364* have different power voltage requirements. Some have to be isolated and some have to provide high current. Here is how power supplies are organised on the board.

- **5 Volts** (analogue – ADCs): each ADC requires 320mA; that's 1.28A in total. Analogue Devices recommends a low-noise regulator. Linear Technology produces such components. The LT1764 can provide up to 3 Amps with 40uV of noise. To avoid noise and heat problems, the *SMT364* has two linear regulators, one for each couple of ADCs. A DC-DC switcher supplied in 12 Volts, will provide both regulators with a lower voltage. Micrel produces such a switcher: MIC4684.
- **3.3 Volts** (digital – ADCs, PROM and FPGA I/Os): currents required is low: 45mA per ADC, few mA for the PROM and around 500mA for the FPGA (estimation). This will be drawn from both 3.3-Volt mounting holes.
- **1.5 Volts** (FPGA core): estimation has been done and shows a requirement of a maximum of 5 Amps (full FPGA working at 200MHz). No linear regulator can provide such a current without dissipating a lot amount of heat and the use of a heat sink. The solution adopted for the *SMT364* is to have a synchronous switcher to generate 1.5 Volts from the TIM 5-Volt power supply; it is a TI part: TPS54810 *(or* TPS54610), which can provide up to 8 Amps (or 6 Amps). The output ripple is around 10mV, which meets Xilinx requirements for Virtex-II (40 mV max.).

2.4.2.6 Clock management.

Dedicated multiplexers and low-jitter buffers (PECL) are responsible for the clock selection. They ensure a good sampling signal for accurate conversions.

3 Verification Procedures

The specifications will be tested using the following:

1) CommPorts: CommPort transfers between a SMT365 and the SMT364.
2) SHB: *SMT364*-SHB----SHB-*SMT364*. Loop and continuous data going through.
3) ADCs: external clocks and analogue input signals from signal generator. Data packed on SHB to an *SMT365* via an SHD to SDB converter board.

4 Review Procedures

Reviews will be carried out as indicated in design quality document QCF14 and in accordance with Sundance's ISO9000 procedures.

5 Validation Procedures

6 Timing Diagrams

7 Circuit Diagrams

8 PCB Layout Details

8.1 Component Side

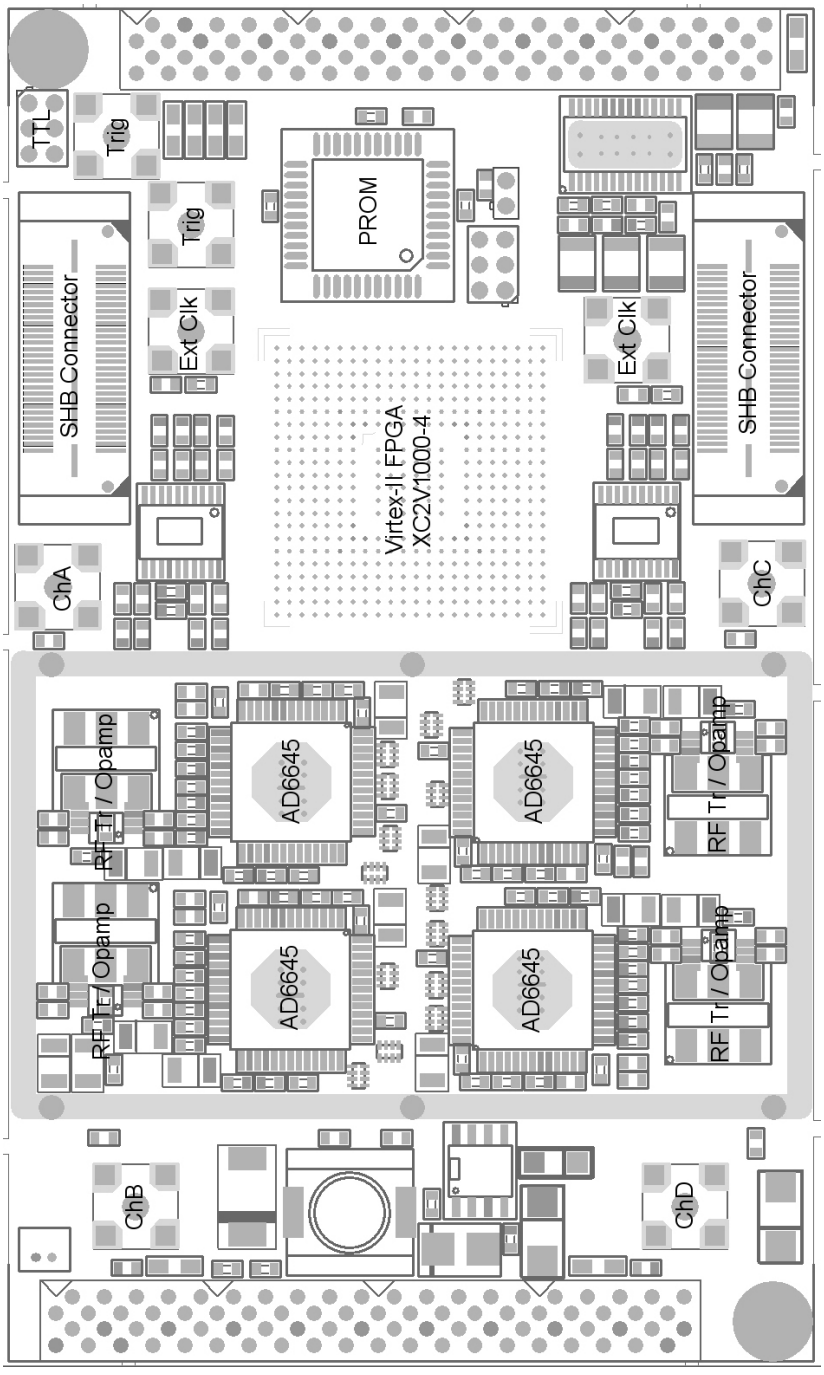

Figure 7 - PCB Layout - Component side.

8.2 Solder Side

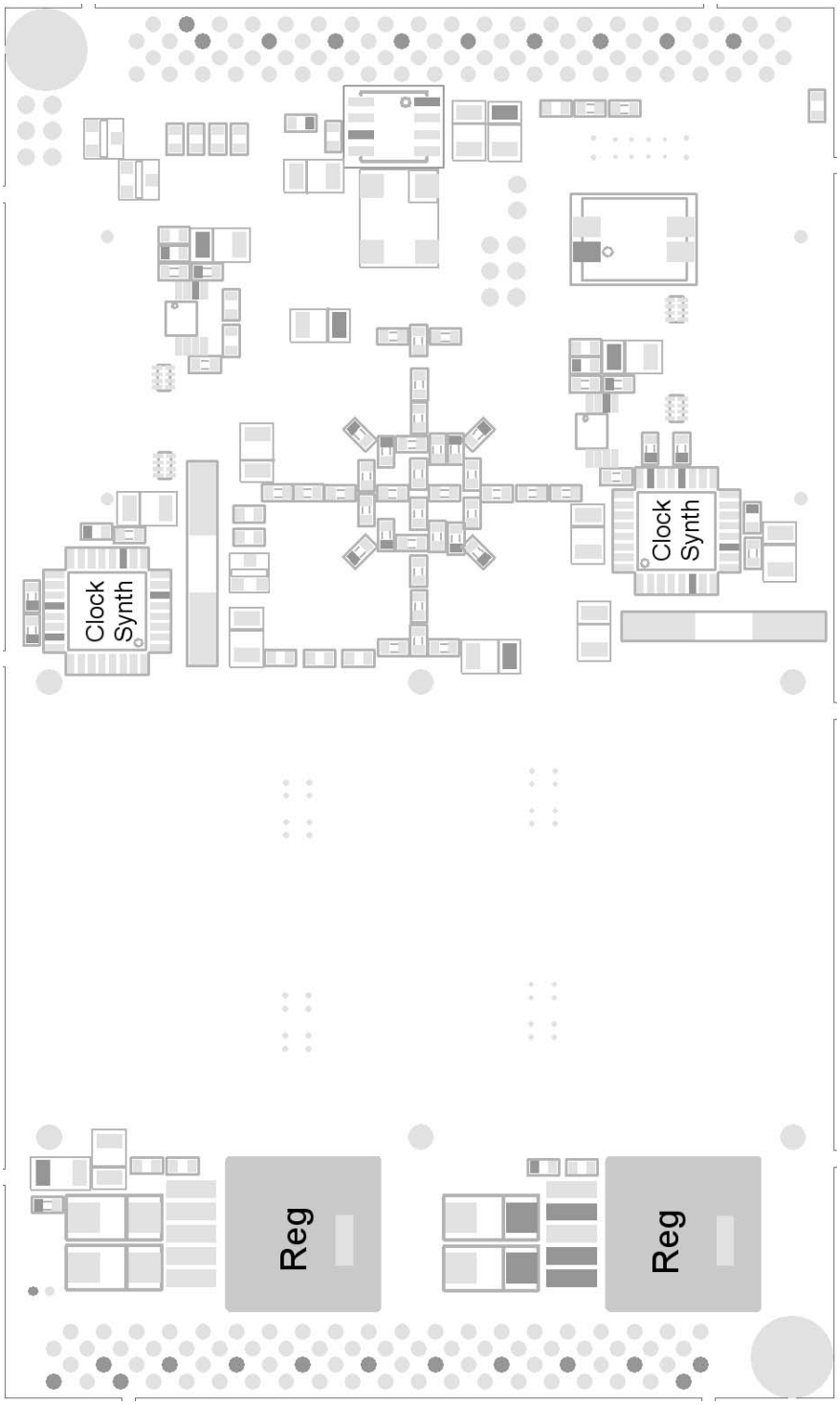

Figure 8 - PCB Layout - Solder side.

9 Pinout and Package Requirements

```
# ########################################
#                                        #
# Constraint File Virtex II for SMT364   #
#                                        #
# Author: Philippe ROBERT                #
# $Date: 23.07.2002                      #
# $Version: 1.0 - Original draft         #
# $Date: 09.09.2002                      #
# $Version: 1.1 - CP1 removed and Clock synthesizer changed#
# $Date: 23.07.2002                      #
#$Version 1.0 generated with FloorPlanner #
# $Version 1.1 01/04/03 - pinout reviewed #
# (c) Sundance Multiprocessor Technology #
########################################
# Start of Constraints extracted by Floorplanner from the Design
# ADCD
NET "adcd_rdy_gclk" LOC = "AB12" ;
NET "adcd_rdy" LOC = "AA16" ;
NET "adcd_ovr" LOC = "V17" ;
NET "adcd_data<13>" LOC = "AB16" ;
NET "adcd_data<12>" LOC = "W16" ;
NET "adcd_data<11>" LOC = "Y16" ;
NET "adcd_data<10>" LOC = "V16" ;
NET "adcd_data<9>" LOC = "V15" ;
NET "adcd_data<8>" LOC = "AA17" ;
NET "adcd_data<7>" LOC = "AB17" ;
NET "adcd_data<6>" LOC = "AA18" ;
NET "adcd_data<5>" LOC = "AB18" ;
NET "adcd_data<4>" LOC = "W17" ;
NET "adcd_data<3>" LOC = "Y17" ;
NET "adcd_data<2>" LOC = "W18" ;
NET "adcd_data<1>" LOC = "Y18" ;
NET "adcd_data<0>" LOC = "AB19" ;
# ADCC
NET "adcc_rdy_gclk" LOC = "Y12" ;
NET "adcc_rdy" LOC = "AA13" ;
NET "adcc_ovr" LOC = "Y15" ;
NET "adcc_data<13>" LOC = "AB13" ;
NET "adcc_data<12>" LOC = "U13" ;
NET "adcc_data<11>" LOC = "V13" ;
NET "adcc_data<10>" LOC = "W13" ;
NET "adcc_data<9>" LOC = "Y13" ;
NET "adcc_data<8>" LOC = "AA14" ;
NET "adcc_data<7>" LOC = "AB14" ;
NET "adcc_data<6>" LOC = "W14" ;
NET "adcc_data<5>" LOC = "Y14" ;
NET "adcc_data<4>" LOC = "U14" ;
NET "adcc_data<3>" LOC = "V14" ;
NET "adcc_data<2>" LOC = "AA15" ;
NET "adcc_data<1>" LOC = "AB15" ;
NET "adcc_data<0>" LOC = "W15" ;
# ADCB
NET "adcb_rdy_gclk" LOC = "V11" ;
NET "adcb_rdy" LOC = "AB7" ;
NET "adcb_ovr" LOC = "V9" ;
NET "adcb_data<13>" LOC = "AA7" ;
NET "adcb_data<12>" LOC = "U9" ;
NET "adcb_data<11>" LOC = "V8" ;
NET "adcb_data<10>" LOC = "Y8" ;
NET "adcb_data<9>" LOC = "W8" ;
NET "adcb_data<8>" LOC = "AB8" ;
NET "adcb_data<7>" LOC = "AA8" ;
NET "adcb_data<6>" LOC = "Y9" ;
NET "adcb_data<5>" LOC = "W9" ;
NET "adcb_data<4>" LOC = "AB9" ;
NET "adcb_data<3>" LOC = "AA9" ;
NET "adcb_data<2>" LOC = "Y10" ;
NET "adcb_data<1>" LOC = "W10" ;
NET "adcb_data<0>" LOC = "V10" ;
# ADCA
NET "adca_rdy_gclk" LOC = "Y11" ;
NET "adca_rdy" LOC = "AB4" ;
NET "adca_ovr" LOC = "W7" ;
NET "adca_data<13>" LOC = "AA4" ;
NET "adca_data<12>" LOC = "Y4" ;
NET "adca_data<11>" LOC = "AA3" ;
NET "adca_data<10>" LOC = "Y5" ;
NET "adca_data<9>" LOC = "W5" ;
NET "adca_data<8>" LOC = "V7" ;
NET "adca_data<7>" LOC = "V6" ;
NET "adca_data<6>" LOC = "AB5" ;
NET "adca_data<5>" LOC = "AA5" ;
NET "adca_data<4>" LOC = "Y6" ;
```

```
NET "adca_data<3>" LOC = "W6" ;
NET "adca_data<2>" LOC = "AB6" ;
NET "adca_data<1>" LOC = "AA6" ;
NET "adca_data<0>" LOC = "Y7" ;
# CLOCK SYNTHESIZERS
NET "freq_s_load_adc23" LOC = "C17" ;
NET "freq_s_load_adc01" LOC = "A18" ;
NET "freq_s_data_adc23" LOC = "B17" ;
NET "freq_s_data_adc01" LOC = "B19" ;
NET "freq_s_clock_adc23" LOC = "A17" ;
NET "freq_s_clock_adc01" LOC = "A19" ;
NET "freq_np_load_adc23" LOC = "D17" ;
NET "freq_np_load_adc01" LOC = "B18" ;
NET "freq_master_reset" LOC = "C16" ;
NET "freq_clk_sel_adc23<1>" LOC = "E17" ;
NET "freq_clk_sel_adc23<0>" LOC = "E16" ;
NET "freq_clk_sel_adc01<1>" LOC = "F18" ;
NET "freq_clk_sel_adc01<0>" LOC = "D21" ;
# MISC
NET "ttls<3>" LOC = "A15" ;
NET "ttls<2>" LOC = "D15" ;
NET "ttls<1>" LOC = "C15" ;
NET "ttls<0>" LOC = "E15" ;
NET "pxi_trig4" LOC = "D18" ;
NET "pxi_trig3" LOC = "C21" ;
NET "pxi_trig2" LOC = "C22" ;
NET "pxi_trig1" LOC = "E18" ;
NET "pxi_clk" LOC = "C18" ;
NET "nreset" LOC = "V12" ;
NET "leds<3>" LOC = "F14" ;
NET "leds<2>" LOC = "B16" ;
NET "leds<1>" LOC = "A16" ;
NET "leds<0>" LOC = "D16" ;
NET "iiofs<2>" LOC = "Y21" ;
NET "iiofs<1>" LOC = "AA20" ;
NET "iiofs<0>" LOC = "W20" ;
NET "conf_init" LOC = "AA19" ;
NET "conf_din" LOC = "V18" ;
NET "clock" LOC = "D11" ;
NET "adc23_trig" LOC = "T21" ;
NET "adc01_trig" LOC = "T2" ;
# COMMPORT 4
NET "cp4_stb" LOC = "A7" ;
NET "cp4_req" LOC = "B7" ;
NET "cp4_rdy" LOC = "D7" ;
NET "cp4_data<7>" LOC = "D8" ;
NET "cp4_data<6>" LOC = "C8" ;
NET "cp4_data<5>" LOC = "B8" ;
NET "cp4_data<4>" LOC = "A8" ;
NET "cp4_data<3>" LOC = "E9" ;
NET "cp4_data<2>" LOC = "F9" ;
NET "cp4_data<1>" LOC = "D9" ;
NET "cp4_data<0>" LOC = "C9" ;
NET "cp4_ack" LOC = "C7" ;
# COMMPORT 3
NET "cp3_stb" LOC = "V19" ;
NET "cp3_req" LOC = "V22" ;
NET "cp3_rdy" LOC = "V20" ;
NET "cp3_data<7>" LOC = "T20" ;
NET "cp3_data<6>" LOC = "T19" ;
NET "cp3_data<5>" LOC = "U22" ;
NET "cp3_data<4>" LOC = "U21" ;
NET "cp3_data<3>" LOC = "U20" ;
NET "cp3_data<2>" LOC = "U19" ;
NET "cp3_data<1>" LOC = "T18" ;
NET "cp3_data<0>" LOC = "U18" ;
NET "cp3_ack" LOC = "V21" ;
# COMMPORT 1
NET "cp1_stb" LOC = "C12" ;
NET "cp1_req" LOC = "B13" ;
NET "cp1_rdy" LOC = "B12" ;
NET "cp1_data<7>" LOC = "C13" ;
NET "cp1_data<6>" LOC = "D13" ;
NET "cp1_data<5>" LOC = "E13" ;
NET "cp1_data<4>" LOC = "E14" ;
NET "cp1_data<3>" LOC = "A14" ;
NET "cp1_data<2>" LOC = "B14" ;
NET "cp1_data<1>" LOC = "C14" ;
NET "cp1_data<0>" LOC = "D14" ;
NET "cp1_ack" LOC = "A13" ;
# COMMPORT 0
NET "cp0_stb" LOC = "T3" ;
NET "cp0_req" LOC = "T5" ;
NET "cp0_rdy" LOC = "T4" ;
NET "cp0_data<7>" LOC = "U1" ;
NET "cp0_data<6>" LOC = "U2" ;
NET "cp0_data<5>" LOC = "V1" ;
NET "cp0_data<4>" LOC = "V2" ;
NET "cp0_data<3>" LOC = "U3" ;
NET "cp0_data<2>" LOC = "U4" ;
NET "cp0_data<1>" LOC = "W1" ;
NET "cp0_data<0>" LOC = "W2" ;
```

```
NET "cp0_ack" LOC = "R5" ;
# SHBA
NET "shba_clk1" LOC = "D12" ;
NET "shba_clk0" LOC = "E12" ;
NET "shba<59>" LOC = "T1" ;
NET "shba<58>" LOC = "R4" ;
NET "shba<57>" LOC = "R3" ;
NET "shba<56>" LOC = "R2" ;
NET "shba<55>" LOC = "R1" ;
NET "shba<54>" LOC = "P6" ;
NET "shba<53>" LOC = "P5" ;
NET "shba<52>" LOC = "P4" ;
NET "shba<51>" LOC = "P3" ;
NET "shba<50>" LOC = "P2" ;
NET "shba<49>" LOC = "P1" ;
NET "shba<48>" LOC = "N6" ;
NET "shba<47>" LOC = "N5" ;
NET "shba<46>" LOC = "N4" ;
NET "shba<45>" LOC = "N3" ;
NET "shba<44>" LOC = "N2" ;
NET "shba<43>" LOC = "N1" ;
NET "shba<42>" LOC = "M6" ;
NET "shba<41>" LOC = "M5" ;
NET "shba<40>" LOC = "M4" ;
NET "shba<39>" LOC = "M3" ;
NET "shba<38>" LOC = "M2" ;
NET "shba<37>" LOC = "M1" ;
NET "shba<36>" LOC = "L2" ;
NET "shba<35>" LOC = "L3" ;
NET "shba<34>" LOC = "L4" ;
NET "shba<33>" LOC = "L5" ;
NET "shba<32>" LOC = "K1" ;
NET "shba<31>" LOC = "K2" ;
NET "shba<30>" LOC = "K3" ;
NET "shba<29>" LOC = "K4" ;
NET "shba<28>" LOC = "L6" ;
NET "shba<27>" LOC = "K6" ;
NET "shba<26>" LOC = "K5" ;
NET "shba<25>" LOC = "J5" ;
NET "shba<24>" LOC = "J1" ;
NET "shba<23>" LOC = "J2" ;
NET "shba<22>" LOC = "J3" ;
NET "shba<21>" LOC = "J4" ;
NET "shba<20>" LOC = "H1" ;
NET "shba<19>" LOC = "H2" ;
NET "shba<18>" LOC = "H3" ;
NET "shba<17>" LOC = "H4" ;
NET "shba<16>" LOC = "J6" ;
NET "shba<15>" LOC = "H5" ;
NET "shba<14>" LOC = "G1" ;
NET "shba<13>" LOC = "G2" ;
NET "shba<12>" LOC = "G3" ;
NET "shba<11>" LOC = "G4" ;
NET "shba<10>" LOC = "F1" ;
NET "shba<9>" LOC = "F2" ;
NET "shba<8>" LOC = "F3" ;
NET "shba<7>" LOC = "F4" ;
NET "shba<6>" LOC = "G5" ;
NET "shba<5>" LOC = "F5" ;
NET "shba<4>" LOC = "E1" ;
NET "shba<3>" LOC = "E2" ;
NET "shba<2>" LOC = "E3" ;
NET "shba<1>" LOC = "E4" ;
NET "shba<0>" LOC = "D1" ;
# SHBB
NET "shbb_clk1" LOC = "F13" ;
NET "shbb_clk0" LOC = "B11" ;
NET "shbb<59>" LOC = "T22" ;
NET "shbb<58>" LOC = "P17" ;
NET "shbb<57>" LOC = "R18" ;
NET "shbb<56>" LOC = "R19" ;
NET "shbb<55>" LOC = "R20" ;
NET "shbb<54>" LOC = "R21" ;
NET "shbb<53>" LOC = "R22" ;
NET "shbb<52>" LOC = "P19" ;
NET "shbb<51>" LOC = "P20" ;
NET "shbb<50>" LOC = "P21" ;
NET "shbb<49>" LOC = "P22" ;
NET "shbb<48>" LOC = "P18" ;
NET "shbb<47>" LOC = "N18" ;
NET "shbb<46>" LOC = "N19" ;
NET "shbb<45>" LOC = "N20" ;
NET "shbb<44>" LOC = "N21" ;
NET "shbb<43>" LOC = "N22" ;
NET "shbb<42>" LOC = "N17" ;
NET "shbb<41>" LOC = "M17" ;
NET "shbb<40>" LOC = "M18" ;
NET "shbb<39>" LOC = "M19" ;
NET "shbb<38>" LOC = "M20" ;
NET "shbb<37>" LOC = "M21" ;
NET "shbb<36>" LOC = "L22" ;
NET "shbb<35>" LOC = "L21" ;
```

```
NET "shbb<34>" LOC = "L20" ;
NET "shbb<33>" LOC = "L19" ;
NET "shbb<32>" LOC = "L18" ;
NET "shbb<31>" LOC = "L17" ;
NET "shbb<30>" LOC = "K22" ;
NET "shbb<29>" LOC = "K21" ;
NET "shbb<28>" LOC = "K20" ;
NET "shbb<27>" LOC = "K19" ;
NET "shbb<26>" LOC = "K18" ;
NET "shbb<25>" LOC = "K17" ;
NET "shbb<24>" LOC = "J22" ;
NET "shbb<23>" LOC = "J21" ;
NET "shbb<22>" LOC = "J20" ;
NET "shbb<21>" LOC = "J19" ;
NET "shbb<20>" LOC = "J18" ;
NET "shbb<19>" LOC = "J17" ;
NET "shbb<18>" LOC = "H22" ;
NET "shbb<17>" LOC = "H21" ;
NET "shbb<16>" LOC = "H20" ;
NET "shbb<15>" LOC = "H19" ;
NET "shbb<14>" LOC = "G22" ;
NET "shbb<13>" LOC = "G21" ;
NET "shbb<12>" LOC = "G20" ;
NET "shbb<11>" LOC = "G19" ;
NET "shbb<10>" LOC = "H18" ;
NET "shbb<9>" LOC = "G18" ;
NET "shbb<8>" LOC = "F22" ;
NET "shbb<7>" LOC = "F21" ;
NET "shbb<6>" LOC = "F20" ;
NET "shbb<5>" LOC = "F19" ;
NET "shbb<4>" LOC = "E22" ;
NET "shbb<3>" LOC = "E21" ;
NET "shbb<2>" LOC = "E20" ;
NET "shbb<1>" LOC = "E19" ;
NET "shbb<0>" LOC = "D22" ;
```

10 Safety

This module presents no hazard to the user.

11 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.