SUNDANCE

SMT377

User Manual

Certificate Number FM 55022

Revision History

Date	Comments	Engineer	Version
16/05/02	First release	PSR	0.9
08/11/03	Update for SMT377v2 PCB and dimension added	PSR	1.0
18/12/03	LEDs location and function added	PSR	1.1

Table of Contents

Table of figures.

Contacting Sundance

You can contact Sundance for additional information by sending email to **support@sundance.com**

Outline Description

The *SMT377* (377) is a single width TIM, which provides 8 channels of DAC output using two Burr Brown *DAC7634* devices. It is offering the following features:

- 8 channels of DAC outputs, using 16-bit Burr Brown *DAC7634* devices, with a settling time of 10us to 0.003%.
- Single width module
- On-board CPLD for reconfiguration via ComPort
- External Clock and Trigger
- Programmable sample/selectable clock
- Three ‘C4x type comm-ports (1, 3 and 4)
- One SHB interface (Sundance High-speed Bus)
- Up to 1 MWord of 16 bits of ZBTRAM for pattern storage (2 independent banks)
- Xilinx Virtex-II FPGA for user defined output waveforms
- TIM standard compatible
- 12 month warranty

Block Diagram.

The following diagram shows interconnections between main blocks of the *SMT377*. Greyed out blocks represent the main devices fitted on the board. Other blocks are on-board connectors or secondary devices.

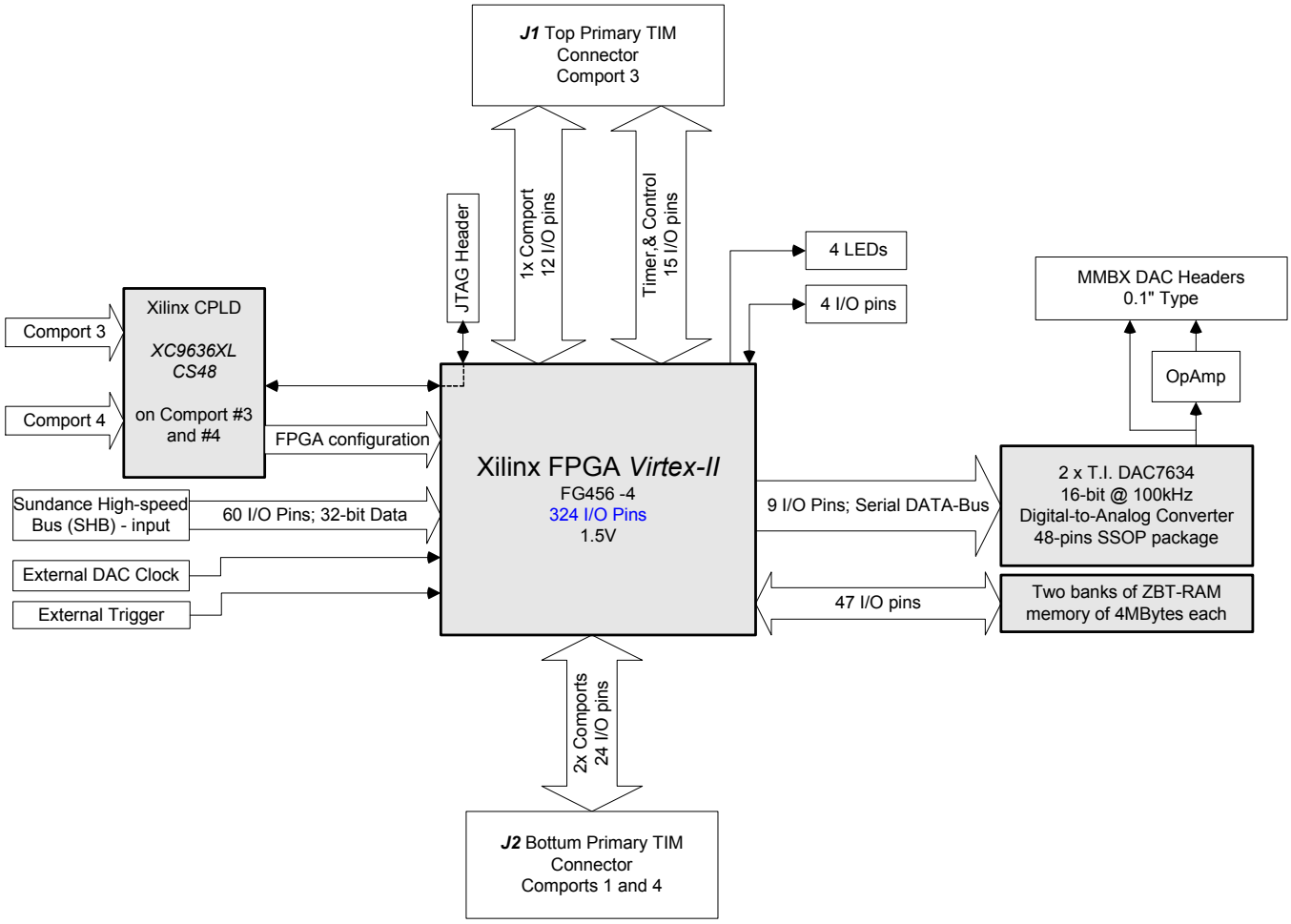

Figure 1 - Block diagram.

SMT377 Connectors.

The following diagram shows the location and the pinout of the connectors:

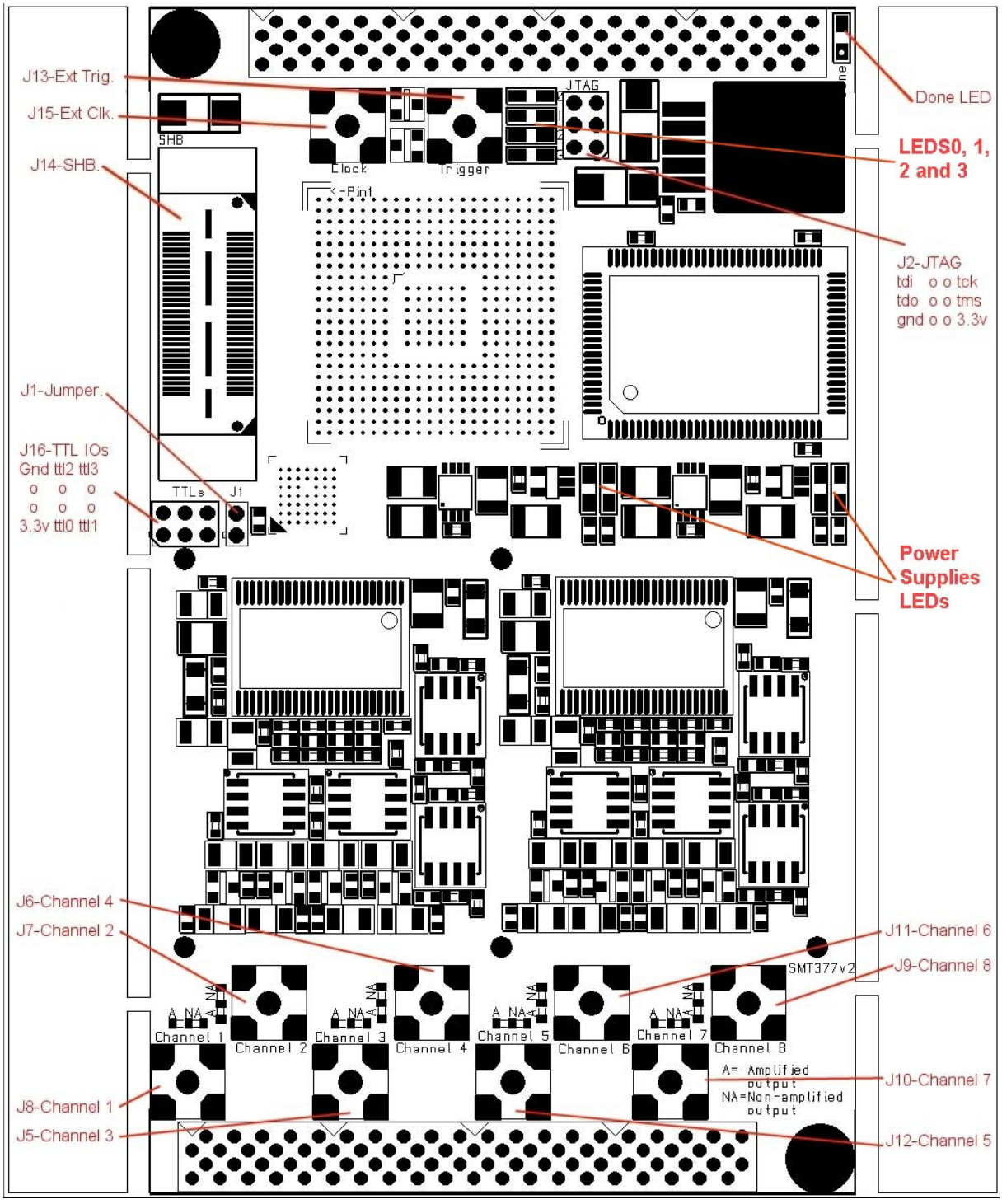

Figure 2 - SMT377 Connectors.

Architecture description.

The module consists of two *DAC7634*-quad digital to analogue converters (DAC). They are serially connected to a *Xilinx* Virtex-II FPGA, which is responsible for transferring the output samples to the DACs.

DAC output range is +/-2.5V. Output channels (***1 to 8; J5-J12***) are either available directly from the DAC chips (***NA***) or a buffered (***A***) output – via output opamps (Selection on hardware – to be specified on order). The selection is made via dual-position resistors on the board.

The *Xilinx* Virtex-II FPGA is configured from a ComPort – 3 or 4 (3 by default) – via a CPLD. FPGA (re)configuration is allowed only prior to a module (TIM) reset or at anytime using the JTAG connector (***J2***) and a Xilinx programming cable (Parallel III or IV).

The on-board memory can be externally accessed. Some waveform patterns can be stored, read back and converted into analogue signals – Pattern generator mode.

DAC output samples are input to the FPGA from one of following sources: Comport or SHB. The current default firmware implement only the Comport option. DAC samples can by routed to the memory for *Pattern Generator* mode or straight to the DACs for *Direct Transfer* mode

DAC7634, 16 bit, quad voltage output Digital-to-Analog converter.

The *DAC7634* is a 16-bit, quad voltage output, Digital-to-Analog Converter with guaranteed 15-bit monotonic performance over the specified temperature range. It accepts 24-bit serial input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a serial data output for daisy chaining multiple DACs. Programmable asynchronous reset clears all registers to a mid-scale code of 8000H or to a zero-scale of 0000H.

The *DAC7634* is a low power device (10mW) with a **10**μs settling time to 0.003%.

It operates from a +5 Volts and –5 Volts supplies and +2.5 Volts and –2.5 Volts as reference voltages, which means that the output range is –2.5 to +2.5 Volts.

The following link gives more details about the DAC7634:

http://focus.ti.com/docs/prod/productfolder.jhtml?genericPartNumber=DAC7634

Xilinx Virtex-II FPGA.

The *Virtex-II* family is a platform FPGA developed for high frequency clocking. The leading-edge 0.15µm / 0.12µm CMOS 8-layer metal process and the *Virtex-II* architecture are optimized for high speed with low power consumption (1.5 Volts core voltage).

Virtex-II devices are user-programmable gate arrays with various configurable elements. The *Virtex-II* is comprised of

- input/output blocks (IOBs), which can be configured as LVTTL, LVDS (2.5 and 3.3 Volts), DDR and many other formats.
- internal configurable logic blocks (CLBs). provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive.
- Block SelectRAM memory modules provide large 18-Kbit storage elements of True Dual-Port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse and fine-grained clock phase shifting, and electromagnetic interference (EMI) reduction.

You can find more details about Xilinx FPGAs on the following link:

http://www.xilinx.com/xlnx/xil_prodcat_product.jsp?title=v2_features

ZBT-RAM Memory.

The *SMT377* is populated with 2 independent banks of pipelined ZBT-RAM (Zero Bus Turnaround), which means that it is optimised for a 100 percent bus utilisation, eliminating any cycle when transitioning from READ to WRITE or vice versa.

Each bank of memory is 16-bit wide and can store 512Kwords. Both banks are independently driven by the FPGA, which makes the board capable to store 1 Mega words of 16 bits.

The default FPGA firmware implement only one ZBTRAM interface.

More information about ZBTRAM on:

http://www.micronsemi.com/products/category.jsp?path=/SRAM/ZBT+SRAM&ct=hp.pl

LEDs.

There 9 green LEDs on the board (see Figure 2 - SMT377 Connectors. for location on the board):

- LEDs labelled 0, 1, 2 and 3 on the silkscreen are driven by the FPGA. LED0 flashes at a sub-frequency of the internal 20MHz clock. LED1 flashes at a sub frequency of the internal 50MHz clock. LED2 reflects bit 16 is the latest control word received. LED3 reflects bit 17 of the latest control word received.
- DONE LED (top left corner) is ON when the FPGA is configured.
- Two groups of two LEDs in the middle of the board (along the edge of the metal can) shows the presence of the dual + and – 5Volt power supplies.

Communication ports (ComPorts).

The *SMT377* provides three 8-bit, data-parallel (1, 3 and 4), inter-processor links that follow Texas Instruments' TMS320C4x Communication Port standard. Additional information on the standard is available in the TMS320C4x User's Guide chapter 12: *Communication ports and the Texas Instrument Module Specification*.

The standard gives a TIM six links numbered from 0 to 5. Each link can be a transmitter or a receiver, and will switch automatically between these states depending on the way you use it. Writing to a receiver or reading from a transmitter will cause a hardware negotiation (token exchange) that will reverse the state of both ends of the link.

One the *SMT377*, only ComPorts 1, 3 and 4 are available.

Following a processor reset, the first three links (0, 1, and 2) initialise as transmitters and the remainder (3, 4, and 5) initialise as receivers. When you wire TIMs together you *must* make sure that you only ever connect links initialising as transmitters to links initialising as receivers; never connect two transmitters or two receivers. For example, connecting link 0 of one TIM to link 4 of another is safe; connecting link 0 of one TIM to link 2 of another could damage the hardware.

Always connect comports 0, 1, or 2 to comports 3, 4, or 5.

On the *SMT320* carrier board the physical connection between ComPorts is made with FMS cables (Ref. SMT3xx-FMS). You must be careful when connecting the cables the make sure that one end is inserted in the opposite sense to the other. One end must have the *blue* backing facing out and the other must have the *silver* backing facing out.

The *SMT320* motherboard communicates with the host PC using ComPort 3 of the site 1 TIM. You should not make any other connections to this ComPort.

To have details on the ComPort interface, refer to:

http://www.sundance.com/docs/TIM_Spec_v1_12.pdf

SHB.

The *SMT377* provides one **S**undance **H**igh-speed **B**us (SHB). These 16-bit data parallel links for synchronous transmission can achieve high-speed data transfer across 60-way flat ribbon cables with ground-interlaced 3.3v signals

To have details on the SHB, refer to:

http://www.sundance.com/docs/SHB Technical Specification.pdf

External Clock – External Trigger.

The current version of the firmware does not implement these features.

Installation.

The minimum system requirements needed to run an *SMT377* on a PC is a carrier board providing + and –12 Volts and at least one C6x TIM transmitter at reset ComPort (CommPort 0,1 or 2) to allow configuration of the SMT377.

Follow these steps to install the *SMT377* module onto a carrier board:

- Place the *SMT377* module into the second, third or fourth TIM sites on the carrier board.
- Make sure that the board is firmly seated. Add a bold and a screw on both mounting holes, located on two opposite corners. Tight them to make a good connection and provide 3.3 Volts to the module.
- Place a C6x TIM board in the first TIM site (PCI connector side), by following the instructions specified in the relevant document.
- Connect CommPort3 of the *SMT377* to a transmitter at reset CommPort on the C6x module (0, 1 or 2).

The following example shows the example of an SMT376 and an SMT377v2 on an SMT310Q PCI carrier board:

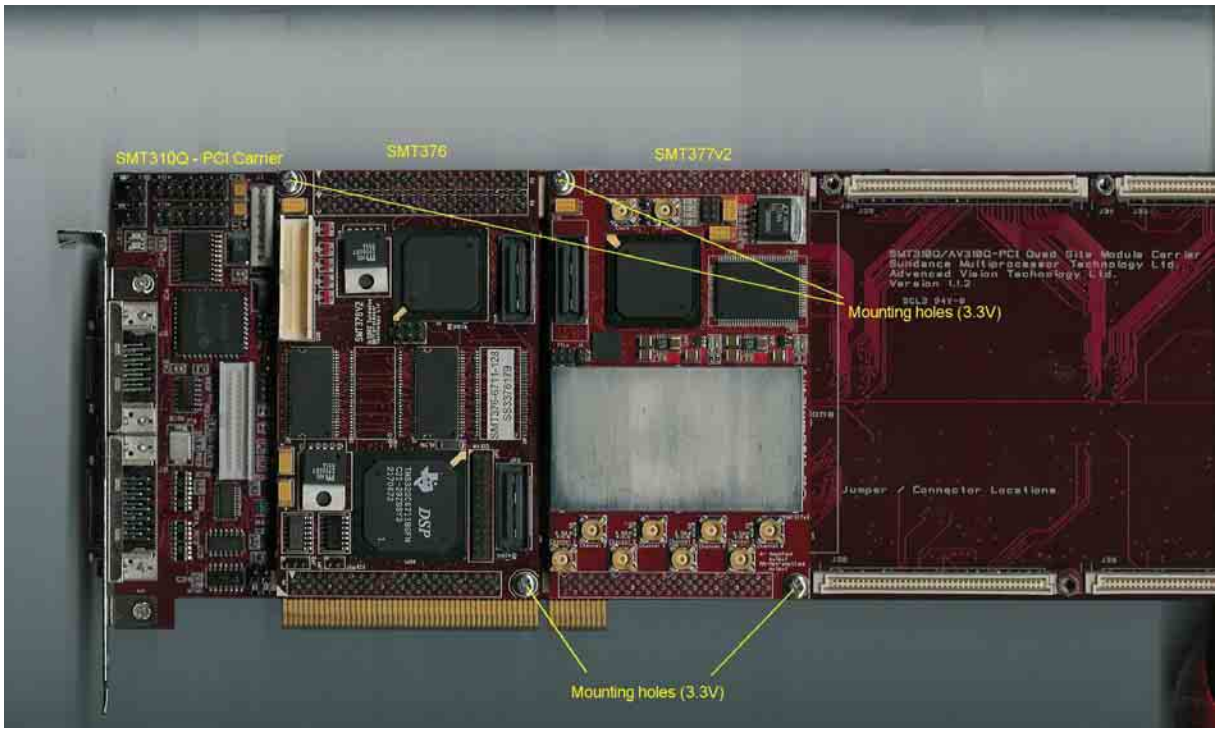

Figure 3 - Example of installation on an *SMT310Q*.

The next picture shows the example of CommPort connection of an *SMT376* to an *SMT377* at the back of an *SMT310Q*:

Figure 4 - Example of installation - ComPort connection.

Configuration

There are two ways to configure or re-configure the FPGA: via ComPort3 (only after a TIM reset) or JTAG using a Xilinx Programming Parallel III or IV cable.

The board is provided with a C routine and its 3L matching application to configure the FPGA via ComPort 3.

Getting control of the *SMT377*.

The *SMT377* once configured needs to receive control words via CommPort 3 to start converting digital data into analogue.

The board consists of 8 DAC channels. Each channel is interfaced with one FIFO all implemented in the Virtex-II FPGA. It allows compensating speed changes between the receiving and transmitting part. The programmable device slows down automatically the transfer when necessary.

The eight channels are independent in terms of data. A digital data can be sent at anytime to any of the eight channels or to four or eight channels at a time, by loading a control word into the internal control register.

The *SMT377* includes two Sample Rate Generators (SRGs), which can be loaded independently at anytime, by sending a control word to the internal register. The first SRG deals with Channel 1, 2, 3 and 4 and the second one with Channels 5, 6, 7 and 8.

The control register also allows the users to write/read into/from the on-board ZBTRAM memory. Each memory address points on a 16-bit sample. Writing is always made in burst mode, i.e. a Start Address is loaded first, then a burst size and then data are sent one by one. Data can then be read back and either be sent back to the host or to the DACs as samples, which makes it behaving as a pattern generator.

Internal registers can be reset via the control register.

All these functions are detailed in the following table:

	Control bits				
	31	30	29	28	
DAC control	0	0	0	0	DAC output
	0	0	0	1	Load SRG0 and SRG1
Memory control	0	1	0	0	Load Start Address
	0	1	0	1	Size burst
	0	1	1	0	Load Data for Memory
	0	1	1	1	Read from Memory (address)
Miscellaneous	1	0	0	0	Start Pattern generator
	1	0	0	1	Stop Pattern generator
	1	1	1	1	Internal register Reset

Figure 5 - Control register.

Bits 31-28 determine the function of the bits 27-0. Here is the detail of all the functions available to control the *SMT377*.

DAC Control – DAC output.

27…21	20	19	18…16	15…0
Not used	Quick Load – Ch. 4,5,6 and 7	Quick Load – Ch. 0,1,2 and 3	Channel number (000-111)	Sample Data

Note: Quick Load, means that the DAC output value of the current control word will be loaded into four or eight channels at the same time. In the case of a quick load, bits 16 to 18 are ignored.

DAC Control – Load SRG0 and SRG1 – minimum value 200.

27…14	13…0
SRG1	SRG0

Each Shift Register is 14-bit wide. The sampling clock is derived from an internal 20MHz (20,000KHz) clock and the value of the shift register is the divider. The minimum value is 200 (matching with the maximum sampling frequency if the DAC –

100KHz). The maximum value of the shift register is 16383, giving a sampling frequency of 1.22 KHz.

For instance, to generate a 50KHz clock, you need to load the shift register with the following value: 20,000 / 50 = 400.

The shift register can be reloaded at any time. It is internally updated after the completion of an entire cycle of the previous value, in order to avoid jumps or un-wanted output value. It can also be updated while the *Pattern Generator* is running.

Shift Register 0 (Channels 1, 2, 3 and 4) and 1 (Channels 5, 6, 7 and 8) can be loaded with different value when using the *Direct Transfer* mode (samples received by ComPort routed directly to DAC). When using the *Pattern Generator* mode, it is required to have the same value for both Shift Register, if not, Shift Register 1 is ignored and is overridden by Shift Register 0. This is due to the current version of the firmware that implements only one ZBTRAM interface.

Memory Control – Load start address.

27…21	20…0
Not used.	Start address

Memory Control – Size burst.

27…21	20…0
Not used.	Burst size

Memory Control – Load data for memory.

27…16	15…0
Not used.	Sample data

Memory Control – Read from memory (address).

27…21	20…0
Not used.	Read address

When sending an address in this mode, the sample data stored at this location is sent back via the control CommPort 3.

Miscellaneous – Start pattern generator.

27…0
Not used.

There is nothing to pass on to the Control Register in this mode; it is only triggering the pattern generator, which then starts read back from the memory '*Burst Size*' (current value of the register) data samples starting from the current '*Start Address*' and sends them to all the DACs at the same time. This operation is repeated until a '*Stop pattern generator*' control word is received.

It is to the used not to send any other control word while the pattern generator is being running.

Miscellaneous – Stop pattern generator.

27…0
Not used.

There is no parameter to pass on to the Control Register in this mode.

Miscellaneous – Internal Register Reset.

27…0
Not used.

There is no parameter for this command; it resets all internal registers.

DAC Analogue outputs.

The SMT377 has 8 analogue outputs. Each of them can be independently non-amplified or amplified by an output op-amp.

Output mode: Amplified, Non-Amplified.

0-Ohm resistors located next to the output connectors are used to do a hardware selection between both modes, as shown on the following picture:

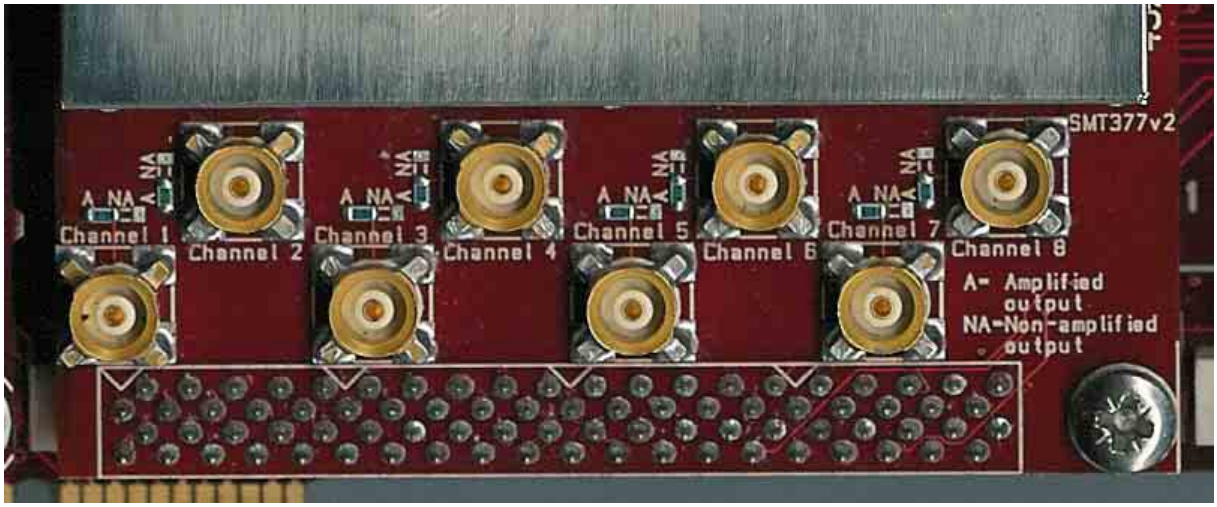

Figure 6 - Output hardware configuration.

Output signal - dynamic.

DAC7634s have a settling time of 10µs; therefore, the maximum sampling frequency is 100KHz. It also means that the maximum frequency that can be generated is 50KHz (Nyquist theory).

Output signal – Static.

DAC7634s are 16-bit DACs for a scale of 5 Volts (-2.5V -> +2.5V). They can be used for example for position regulation. A bit of a sample data represents 76 µVolts.

Module dimensions.

SMT377