HARDWARE SPECIFICATION

FOR

SMT398VP

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APPROVAL PAGE

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29/01/05	E.P	1.0	New document
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1. SCOPE

This document specifies the requirements for The SMT398VP FPGA Tim module

1.1. INTRODUCTION

The SMT398-VP is a TIM module aimed at completing the range of Sundance Virtex II-Pro FPGA modules like SMT351, SMT338-VP, SMT387 and SMT395.

It provides a communications platform between a 2VP50 or 2VP70 Virtex-II Pro FPGA and

- On-board Double Data Rate Dual Port QDR II memory at frequencies of up to 200Mhz.
- Rocket IOs for high speed serial connections capable of various high-speed serial standards.
- LVDS connections for high speed parallel connections
- LVTTL connections and connectors.

This variety of connectors and interfaces provides a wide range of development options for designers to explore the capabilities of the comprehensive Sundance TIM modules family.

1.2. PURPOSE

The SMT398VP must:

- Provide high-speed interface to Sundance ADC/DAC modules
- Provide high-speed interface to Sundance DSP modules.
- Provide high-speed serial or parallel interface to the outside world.
- In any configuration on Sundance carriers, i.e on its own, on a stand-alone carrier or in a Host as part of a system.
-

1.3. APPLICABILITY

Interface to other FPGA, DSP, ADC/DAC modules and in stand alone systems.

2. APPLICABLE DOCUMENTS AND REFERENCES

2.1. APPLICABLE DOCUMENTS

2.1.1. External Documents

TI TIM specification & user's guide.

Samtec QSH Catalogue page

Samsung QDR II Datasheet

Virtex II Pro Datasheet

2.1.2. Internal documents

SUNDANCE SDB specification.

SUNDANCE SHB specification

SUNDANCE SLB specification

SUNDANCE RSL specification

2.1.3. Project Documents

DXXXXH-SPEC.mpp Software Planning Document for … labelled xxxx in Source Safe

2.2. REFERENCES

2.2.1. External documents

N.A

2.2.2. Internal documents

N.A

2.2.3. Project documents

N.A

2.3. PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

3. ACRONYMS, ABBREVIATIONS AND DEFINITIONS

3.1. ACRONYMS AND ABBREVIATIONS

TIM	Texas Instruments Module

3.2. DEFINITIONS

4. REQUIREMENTS

4.1. PRIME ITEM DEFINITION

This module conforms to the TIM standard (**T**exas **I**nstrument **M**odule, See TI TIM specification & user's guide) for single width modules.

It sits on a carrier board.

The carrier board provides power, Ground, communication links (Comport links) between all the modules fitted and a pathway to the host, for a non stand-alone system.

The SMT398-VP requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards), which must be provided by the two diagonally opposite mounting holes.

4.1.1. Prime Item Diagrams

Figure 1 shows a simplified version of the SMT398-VP module

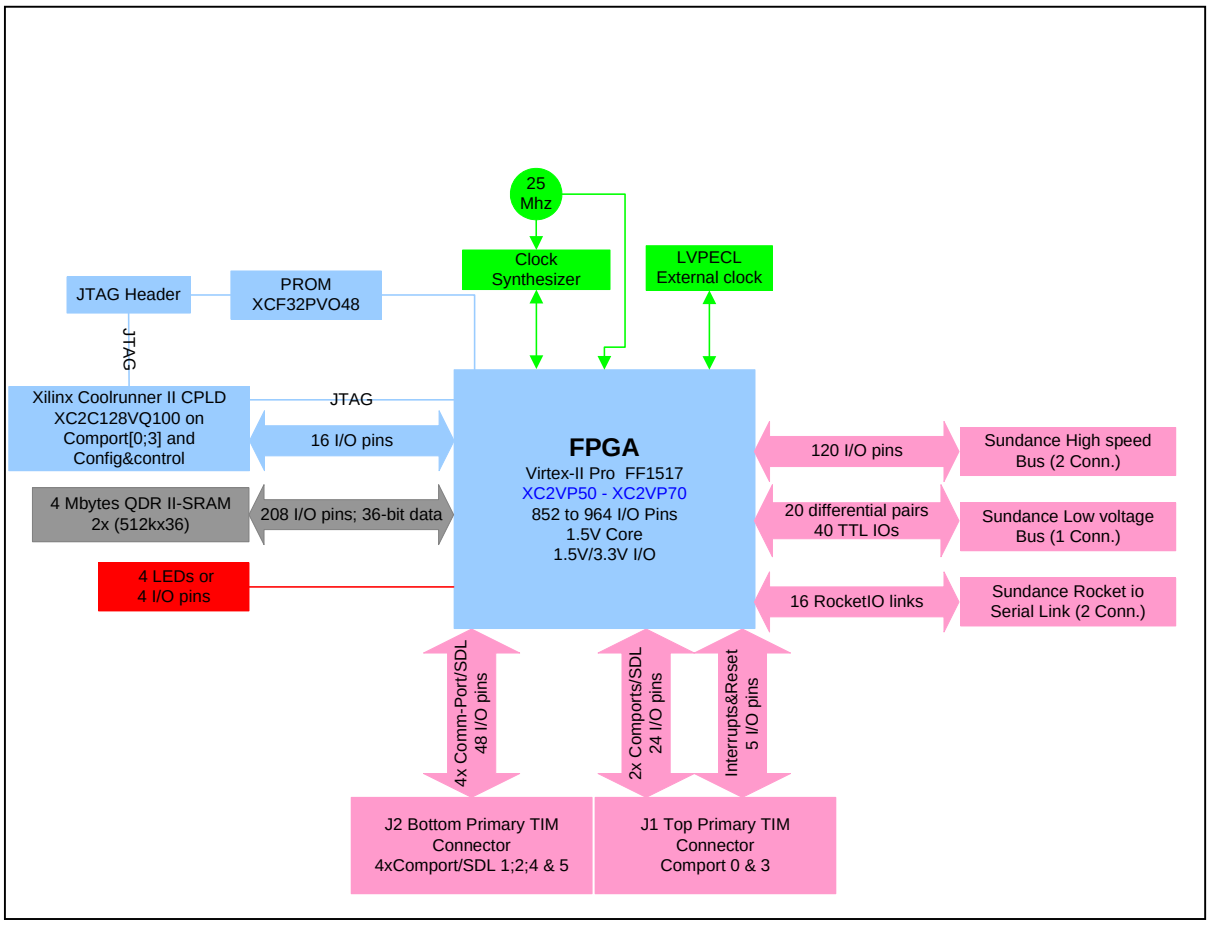


Figure 1: Block Diagram

4.1.2. Interface Definition

For the TIM to carrier board or external world interfacing, see in Sundance Help file (that you can download from this link)

4.1.3. Major Component List

- Block1: Xilinx Virtex II PRO XC2VP50 or XC2VP70 and configuration scheme.
- Block2: QDR II SRAM memory.
- Block3: IO connectors for general purpose or dedicated interfaces.
- Block4: Clocking scheme performing from 25 MHz up to 700MHz.
- Block5: Leds for development and in-use monitoring and general purpose use.

4.1.4. Prime Item Characteristics

4.1.4.1. FPGA

Xilinx Virtex II Pro XC2VP50 or XC2VP70FF1517 FPGA.

This device is packaged in a 1517-pin BGA package with a -6 or -7 speed grade. It contains 2 PowerPC 405s and up to 16 Rocket-I/Os.

4.1.4.2. CPLD

Xilinx Coolrunner II device XC2C128-6VQ100C This device is packaged in a 100-pin very Thin QFP package with a -6 speed grade.

It can be used to configure the FGPA via Comport 0 or 3.

4.1.4.3. PROM

Xilinx Flash PROM device XCF32PVO48.

Accessed via JTAG to load an FPGA configuration bitstream.

Then, it can be used to configure the FPGA at power up.

Parallel FPGA configuration interface (up to 33 MHz)

Design revision technology enables storing and accessing multiple design revisions for configuration.

Built-in data decompressor compatible with Xilinx advanced compression technology.

4.1.4.4. JTAG Header

The JTAG header is compatible with Xilinx Parallel-IV cable signals.

It supports code download (for the FPGA Power PC), FPGA configuration, Hardware and Software Debugging tools for the Virtex-II Pro.

This cable connects the parallel port of an engineer's Workstation/PC to the JTAG chain of the SMT398VP Module.

All the devices from block1 are chained and accessible via this JTAG header.

4.1.4.5. FPGA Configuration schemes

Different schemes are available to provide maximum flexibility in systems where the SMT398-VP is involved:

The FPGA configuration bitstream source is

- one of the 2 Comports:

The CPLD is connected to 2 Comport links of the SMT398-VP TIM connector. A switch is used to select the configuration Comport that will be used to receive the bitstream.

The CPLD allows for FPGA configuration in slave SelectMap mode.

- Using the on-board Flash PROM.

The CPLD monitors the configuration data between the Xilinx Flash PROM and the FPGA. The FPGA configuration is operated in Master SelectMap mode.

- Using the on-board JTAG header and Xilinx JTAG programming tools.

The JTAG header is a Parallel-IV Header.

4.1.4.6. QDR II SRAM

Up to 4 Mbytes of QDR II SRAM

The memory is available as 2 independent banks of QDRII. Each bank is arranged as follows:

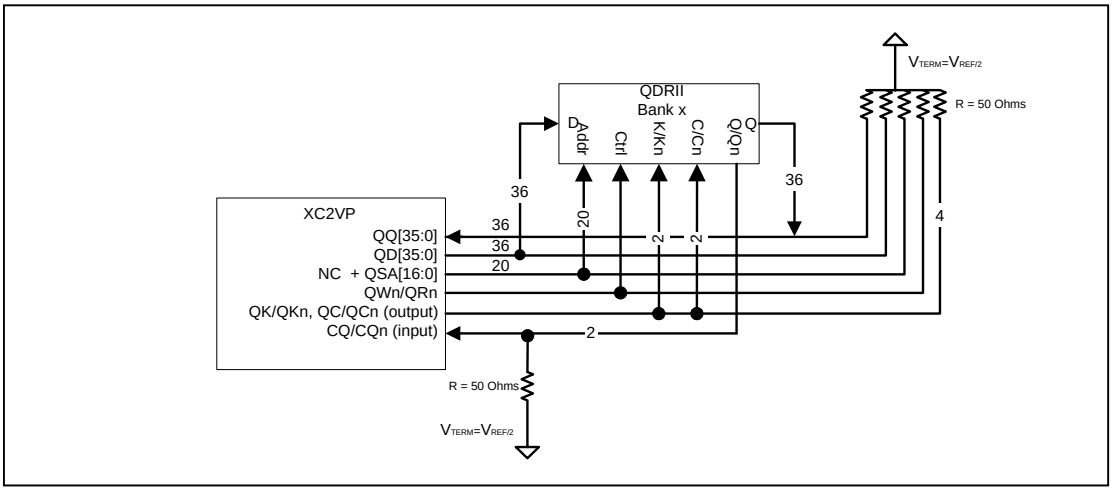


Figure 2: FPGA connections to Bank1 of QDRII

4 word burst-QDR II at 200MHz in 2 independent banks of 36-bits wide data busses. The aggregate throughput for data transfers with the QDR II is 28.8 Gb/s, or 400 Mb/s per pin for a 36-bit write bus and a 36-bit read bus operating in DDR mode at 200 MHz.

Each bank is fully independent with separate address, control and data busses.

The 2 devices used are Samsung K7R163684B-FC30. Alternative part numbers, fully compatible can be fitted depending on availability at time of order.

Alternative part numbers are: Cypress CY7C1315AV18-200BZC or NEC μPD44165364F5-E50-EQ1

4.1.4.7. Sundance High speed Bus

2 x 60 pins connectors provide 120 io connections between the FPGA and the outside word.

They allow interfacing to other Sundance modules providing that you implement an SHB interface in the FPGA. (See 2.1.2.)

The SHB interface is available in Sundance SMT6500 support package.

They allow interfacing to the outside world by implementing your own interface in the FPGA.

The FPGA io banks hosting the SHB signals are powered using Vcco = 3.3v.

4.1.4.8. Sundance Low voltage Bus

1 x 60 LVDS pairs io connections between the FPGA and the outside world.

They allow interfacing to Sundance mezzanine modules providing that you implement an SLB interface in the FPGA. (See 2.1.2.)

They allow interfacing to the outside world by implementing your own LVDS interface in the FPGA.

The FPGA io banks hosting the SLB signals are powered using Vcco = 2.5v.

4.1.4.9. Sundance Rocket io Serial Link

Each MGT (part of the VII PRO FPGA silicon) has separate transmit and receive functions (full-duplex) and can be operated at baud rates from 600 Mb/s to 3.125 Gb/s.

Additionally, every RocketIO MGT block is fully independent and contains a complete set of common SerDes (serializer/deserializer) functions.

This allows Virtex-II Pro devices to support many existing and emerging serial I/O standards at data rates up to 10 Gb/s (when cumulating 4 channels)

- Up to 16 Rocket I/O transceivers are available in the XC2VP50 -70.
- The SMT398-VP provides 14 MGTs that can be configured to implement different MGT interfaces. A mezzanine board which can plug on the SMT398-VP RSL connectors could provide the right connectors to implement the required serial IO standard, for instance: Infiniband (SMT145) channels, Serial ATA channels and Ethernet channels.
- The minimum transfer rate is 2.5Gbits/s on a Virtex II Pro –6 part.
- 14 DC coupled Rocket I/Os are available on our 2 RSL connectors.

Mode	Channels	IO bit rate (Gb/s)
Fiber Channel	1	1.06
		2.12
Gigabit Ethernet	1	1.25
XAUI (10 Gbit Ethernet)	4	3.125
Infiniband	1, 4, 12	2.5
Aurora	1, 2, 3, 4	0.600-3.125
Custom	1, 2, 3, 4	0.600-3.125

Table 1: Communication standard supported by Rocket IO transceivers

4.1.4.10. TIM Connectors

TIM connectors provide 6 communication links (Comports) to the FPGA.

They allow interfacing to Sundance TIM modules or to a Host PC providing that you implement Comport Interface inside the FPGA. (See 2.1.2.)

The Comport interface is available in Sundance SMT6500 support package.

The FPGA io banks hosting the Comport signals are powered using Vcco = 3.3v.

The TIM connectors also provide power/ground, reset and various control signals.

References and specifications for these connectors are available on Sundance Web site

4.1.4.11. DIP Switches

- One four-position DIP switch is connected to the FPGA I/Os for general purpose use in an FPGA design.
- One four-position DIP switch is connected to the CPLD to provide control over the selection of the configuration bitstream source and a special reset feature called “TIM Confign”.

JPC 4	TIM Confign
ON	ENABLED
OFF	DISABLED

Table 2: DIP switch for special reset feature

JPC 3,2, 1	JPC3	JPC2	JPC1
C0P	ON	ON	ON
C3P	OFF	OFF	OFF
PROM	OFF	OFF	ON

Table 3: DIP switch for the selection of the configuration bitstream source

4.1.4.12. Clocking scheme

The SMT398-VP module contains a 25MHz LVTTL clock, a clock synthesiser and 1 connector for external LVPECL clock input/output.

- 25 MHz LVTTL oscillator: Main system clock. Can be input in a DCM.
- ICS clock synthesizer 8442, used to generate any frequencies between 31.25 MHz up to 700MHz with a jitter lower than 40ps required for the Rocket I/O transceiver REFCLK input.
- An external differential clock input is provided to the Virtex II Pro FPGA via 2 connectors. The traces from the connectors are run as a pair to the FPGA where they are terminated with a 100-ohm resistor.

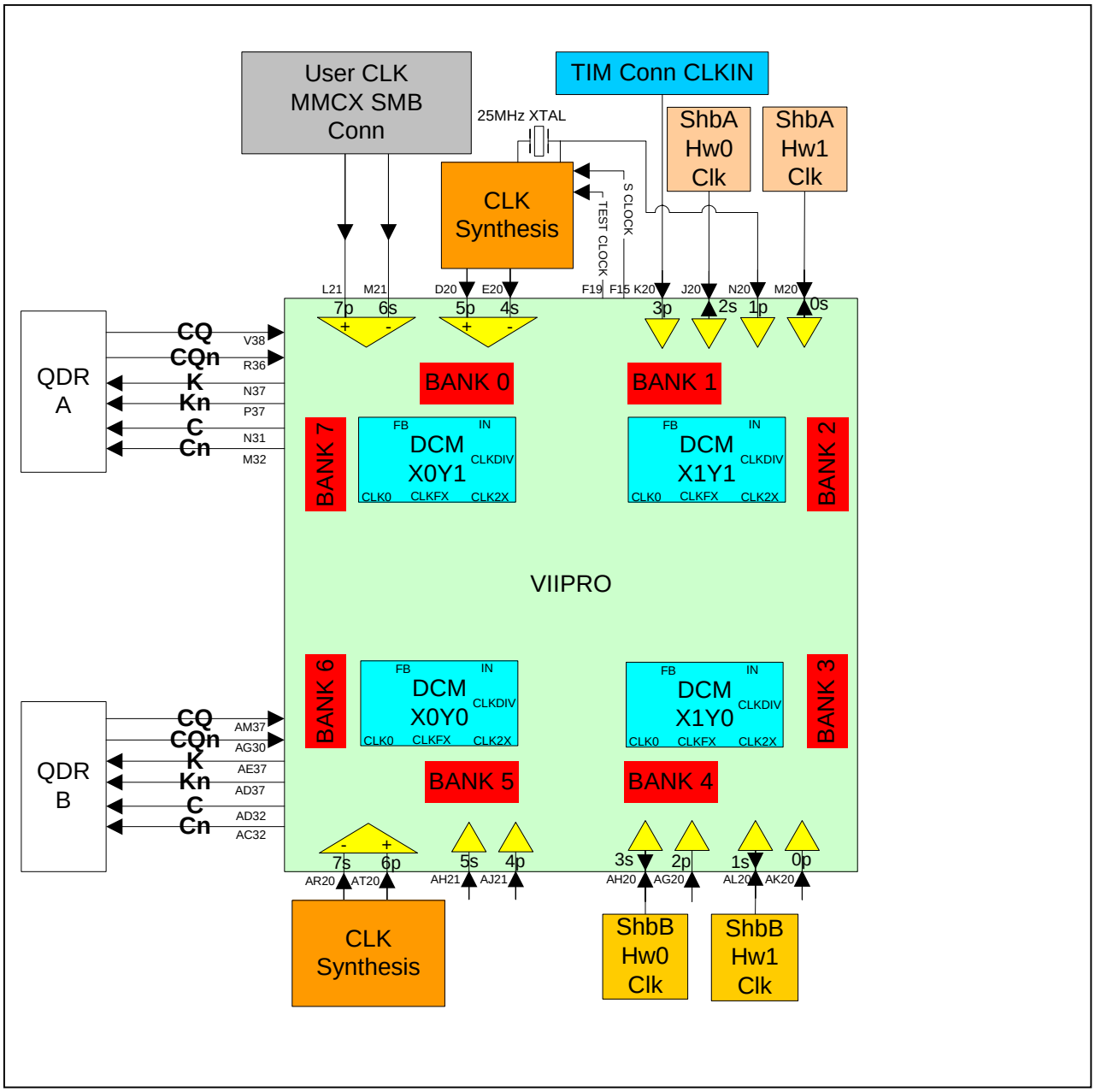


Figure 3: Clocking distribution diagram

Mode	Frequency (MHz)	ICS8442 output frequency to SERDES (MHz)	IO bit rate (Gb/s)
Fiber Channel	25	53.125	1.06
		106.25	2.12
Gigabit Ethernet	25	125	1.25
		250	2.5
		156.25	3.125
Infiniband	25	250	2.5
Aurora	Custom	Custom	0.600-3.125
Custom	Custom	Custom	0.600-3.125

Table 4: Clock synthesizer Configurations for Rocket IO standard application

4.1.4.13. Leds

- 4 Red Leds connect to the FPGA and are available to the User.
- 1 Green Led connects to the DONE pin of the FPGA to show FPGA is configured. The Led Is turned on when the FPGA is configured.
- 1 Red Led for temperature treshold

4.1.5. Performance

The FPGA features like speed grade and density dictate most performances.

The performances achievable by the other components are given in the 4.1.4. Prime Item Characteristics chapter.

4.1.6. Physical Characteristics

4.1.6.1. Power budget

Table 5: Power budget.

Device		Quantity	Voltage(V)	Current(mA)	Power(W)	Source
Static Power on termination resistor (50 ohms) (See details)		200	1.8	16.0	5.76	Virtex II PRO (ds083 module 3 table 6) HSTL II current specification
Samsung QDR II burst 4 (36-bit interface)		2	1.8	550	1.98	Micron DDRSDRAM Datasheet
25 Mhz Clock oscillator		1	3.3	10	0.033	Jauch VX3 Quartz crystal oscillators datasheet
Clock synthesizer	Digital	1	3.3	155	0.5115	ICS 8442 hih frequency synthesizer
	Analog		3.3	20	0.066	
LEDs		5	3.3	25	0.4125	
DIP Switch		1	2.5	2.1	0.005	Four 4.7 Kohm pullup
XC2V50 or 70 FPGA		1	Must be calculated based on design			
Coolrunner II CPLD (See details)		1	1.8	17mA	0.031	CPLD power calculator

Details:

Coolrunner II CPLD power requirement based on design:

During FPGA configuration only, the Coolrunner CPLD power consumption is at its maximum:

- Macrocells used: 40
- Macrocells used as outputs or bidirectional: 26
- Fmax:100Mhz
- The average toggle rate of all flip-flops:40%
- Number of product terms:69

For 1 QDR II Bank the termination at the memory is:

- QQ[35:0] : 36 termination resistors
- QD[35:0] : 36 termination resistors
- QSA[19:0] : 20 termination resistors
- QWn, QRn 2 termination resistors
- QK, QKn: 2 termination resistors
- QC, QCn: 2 termination resistors
- CQ, CQn: 2 termination resistors

So a total of 100 termination resistors per bank.

Please refer to the various specifications.

Links to these specifications can be found at: 2.1.2.

4.1.6.2. Termination and transmission lines

	Signal	At the FPGA	Terminations at the FPGA	Termination at memory
1	Write Data to memory(QD)	OBUF_HSTL_II_18	SSTL2_II_DCI	HSTL_II_18 Split termination
2	Read Data from memory(QQ)	IBUF_HSTL_I_DCI_18	HSTL_II_18	100 ohm pull-up to 1.3v
3	Data Strobe(CQ, CQn)	HSTL_II_18	SSTL2_II_DCI	50 ohm pull-up to 1.3v
4	Clock(QC, QCn, QK, QKn,)	HSTL_II_18	SSTL2_II_DCI	50 ohm pull-up to 1.3v
5	Address(QSA)	HSTL_II_18	SSTL2_II_DCI	50 ohm pull-up to 1.3v
6	Control(QWn, QRn)	HSTL_II_18	SSTL2_II_DCI	50 ohm pull-up to 1.3v

Table 6: QDR II termination scheme

No more than 1 split termination type allowed per bank

5. FOOTPRINT

5.1. TOP VIEW

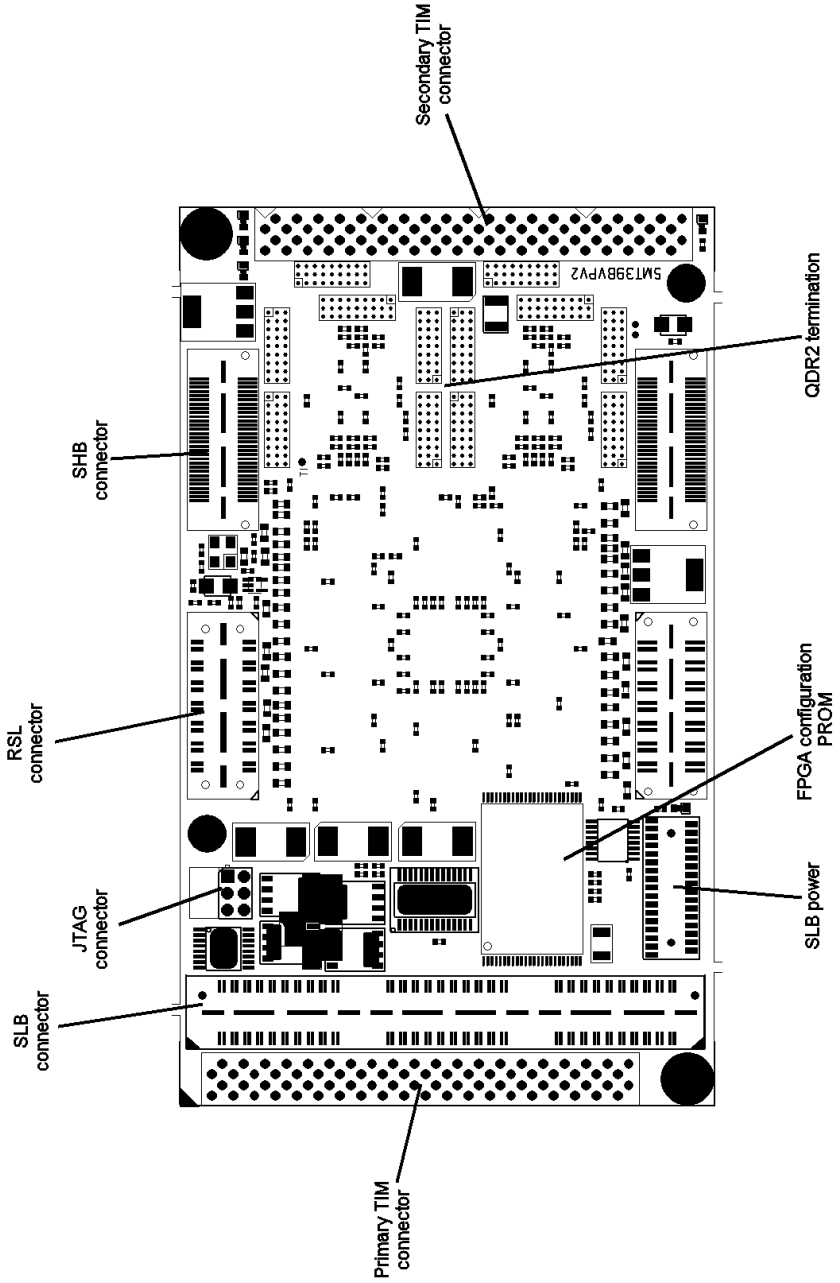


Figure 4: Top View

5.2. BOTTOM VIEW

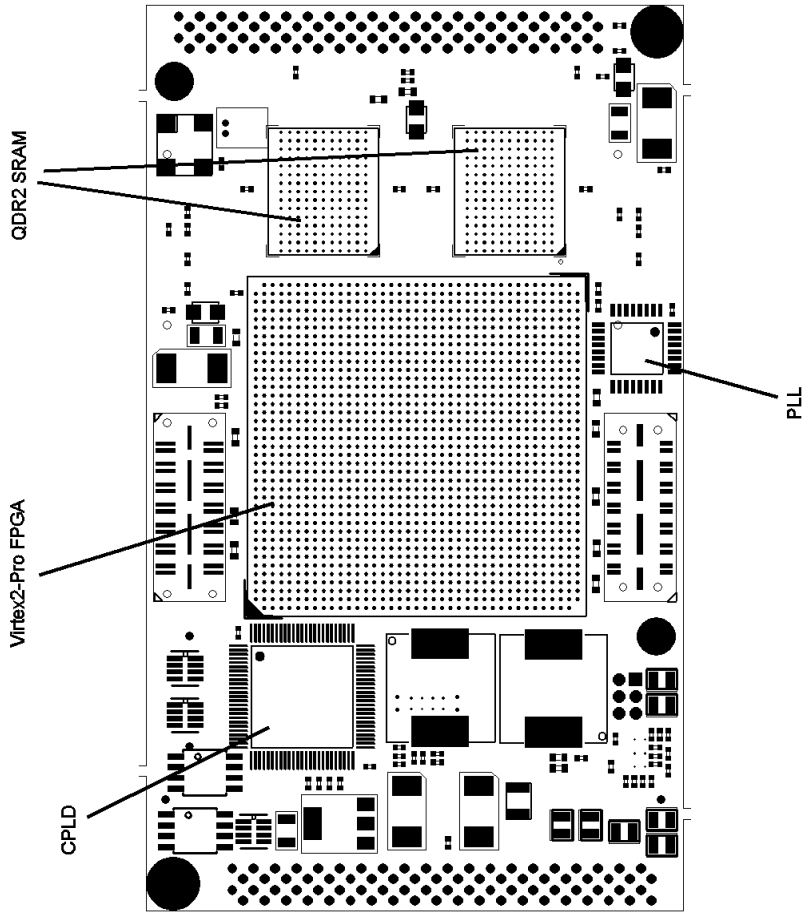


Figure 5: Bottom View

6. PINOUT

6.1. FPGA

6.2. SHB

SUNDANCE SHB specification

6.3. SLB

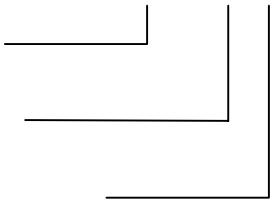
SUNDANCE SLB specification

6.4. RSL

SUNDANCE RSL specification

7. ORDERING INFORMATION

Speed grade		-6	-7
Fpga	XC2VP50FF1517	SMT398-VP50-6	SMT398-VP50-7
	XC2VP70FF1517	SMT398-VP70-6	SMT398-VP70-7



8. QUALIFICATION REQUIREMENTS

8.1. QUALIFICATION TESTS

8.1.1. Meet Sundance standard specifications

- Meet the Tim standard specifications
- Meet the RSL specifications.
- Meet the SLB specifications (LVDS standard).
- Meet the SHB specifications.

8.1.2. Speed qualification tests

- QDRII memory accesses at 200MHz.
- RSL Tx/Rx at 2.5Gbits/s

8.1.3. Integration qualification tests

- Must work on ALL Sundance platforms as a root TIM module or as part of a network of TIMs on carriers.
- Must be able to work stand-alone.