Unit / Module Name:	
Unit / Module Number:	SMT398-VP
Used On:	All Sundance carriers
Document Issue:	1.0.7
Date:	25.10.2004

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Revision History

Issue	Changes Made	Date	Initials
1.0.0	**Initial specifications**	**10.06.2004**	**E.P**
1.0.1	**Corrections of minor presentation details**	**11.06.2004**	**E.P**
1.0.2	**Improved specifications**	**22.07.2004**	**E.P**
1.0.3	**Small modifications**	**16.08.2004**	**E.P**
1.0.4	**Addition of PROM specs.** **Clocking distribution Figure** **Removed some Comports from CPLD**	**02.09.2004**	**E.P**
1.0.5	**Modification of clock synthesizer and addition of tables about serial standards.**	**02.09.2004**	**E.P**
1.0.6	**Update of footprints. Addition of power budget, but incomplete table needs to be finished.** ***In section 3.1.2.1.2* wrong package for the CPLD corrected** ***In section 3.1.2.1.4*, addition of alternative part numbers for the QDRs** ***In section 3.1.2.1.7 clarified that AC coupled links are on SLB bus*** ***In section 3.1.2.1.10* extra red LED to show that the temperature is to high.** **New sections 3.1.2.1.11 and 3.1.2.1.12**	**03.09.2004**	**E.P**
1.0.7	***Correction of CPLD part number in Block Diagram*** ***In section 3.1.2.1.7 AC coupled links.*** ***Update with latest footprints.***	**25.10.2004**	**E.P**

Table of Contents

Table of Figures

Table of Tables

1 Introduction

The SMT398-VP is a TIM module aimed at completing the range of Sundance Virtex II-Pro FPGA modules like SMT351, SMT338-VP, SMT387 and SMT395.

It provides a communications platform between a 2VP50 or 2VP70 Virtex-II Pro FPGA and

- On-board Double Data Rate Dual Port QDR II memory at frequencies of up to 200Mhz.
- Rocket IOs for high speed serial connections capable of various high-speed serial standards.
- LVDS connections for high speed parallel connections
- LVTTL connections and connectors.

This variety of connectors and interfaces provides a wide range of development options for designers to explore the capabilities of the comprehensive Sundance TIM modules family.

Related Documents

SUNDANCE SDB specification.

SUNDANCE SHB specification

SUNDANCE SLB specification

SUNDANCE RSL specification

TI TIM specification & user's guide.

Samtec QSH Catalogue page

Samsung QDR II Datasheet

Virtex-II Pro datasheet

2 Functional Description

2.1 Block Diagram

Figure 1 shows a simplified version of the SMT398-VP module.

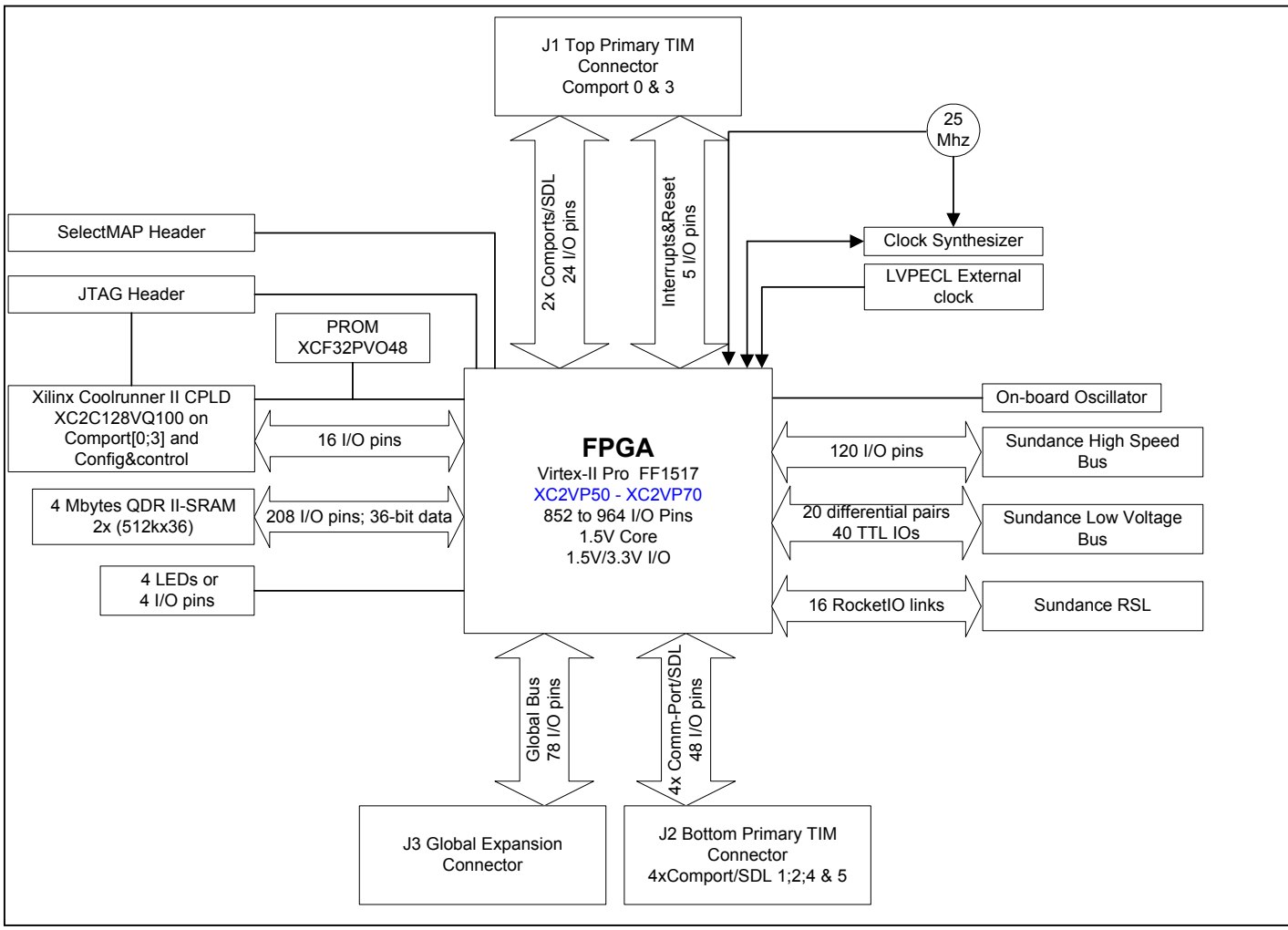

Figure 1: Block Diagram

3 Interface Description

3.1.1 Mechanical Interface

3.1.1.1 TIM Standard

This module conforms to the TIM standard (**T**exas **I**nstrument **M**odule, See TI TIM specification & user's guide) for single width modules.

It sits on a carrier board.

The carrier board provides power, Ground, communication links (Comport links) between all the modules fitted and a pathway to the host, for a non stand-alone system.

The SMT398-VP requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards), which must be provided by the two diagonally opposite mounting holes.

3.1.1.2 TIMs and carrier board.

See in Sundance Help file (that you can download from this link.

3.1.2 Electrical Interface

3.1.2.1 Board Functionality

3.1.2.1.1 FPGA

Xilinx XC2VP50 or XC2VP70FF1517C Virtex-II Pro device. This device is packaged in a 1517-pin BGA package with a -6 or –7 speed grade. It contains 2 PowerPC 405s and up to 16 Rocket-I/Os.

3.1.2.1.2 CPLD

Xilinx Coolrunner II device XC2C128-6VQ100C This device is packaged in a 100-pin very Thin QFP package with a -6 speed grade.

3.1.2.1.3 PROM

Xilinx Flash PROM device XCF32PVO48.

Parallel FPGA configuration interface (up to 33 MHz)

Design revision technology enables storing and accessing multiple design revisions for configuration.

Built-in data decompressor compatible with Xilinx advanced compression technology.

3.1.2.1.4 QDR II SRAM

Up to 4 Mbytes of QDR II SRAM

The memory is available as 2 independent banks of QDRII. Each bank is arranged as follows:

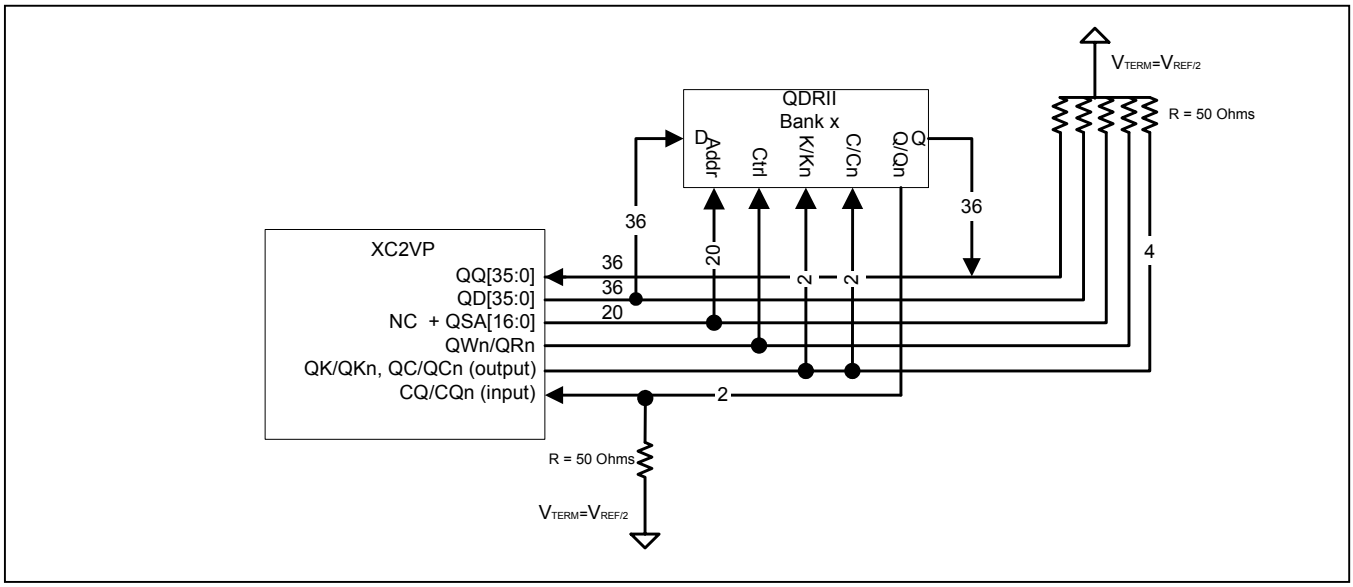

Figure 2: FPGA connections to 1 Bank of QDRII.

4 word burst-QDR II at 200MHz in 2 independent banks of 36-bits wide data busses. The aggregate throughput for data transfers with the QDR II is 28.8 Gb/s, or 400 Mb/s per pin for a 36-bit write bus and a 36-bit read bus operating in DDR mode at 200 MHz.

Each bank is fully independent with separate address, control and data busses. The 2 devices used are Samsung K7R163684B-FC30. Alternative part numbers, fully compatible can be fitted depending on availability at time of order.

Alternative part numbers are: Cypress CY7C1315AV18-200BZC or NEC μPD44165364F5-E50-EQ1

3.1.2.1.5 Reset

- TIM Global Reset

The CPLD is connected to a TIM global Reset signal provided to the SMT398-VP via its TIM Top primary connector pin 30.

The TIM global Reset signal is also available for the FPGA but the CPLD provides another signal called **FPGAResetn** that offers a better Reset control over the FPGA.

At power up or on reception of a low TIM global Reset pulse, the CPLD drives the FPGAResetn signal low and keeps it low.

- TIM Config

On The CPLD is connected a TIM CONFIG signal provided to the SMT398-VP via its TIM Top primary connector pin 74.

CONFIG falling has the same effect on the SMT398-VP CPLD as a TIM global Reset pulse.

On detection of a falling edge on the CONFIG line, the CPLD drives the FPGAResetn signal low and keeps it low.

CONFIG provides a means of reprogramming the FPGA without having to drive the TIM Global Reset signal.

CONFIG is driven from another TIM site on the carrier board, for instance, from a DSP module running an application.

3.1.2.1.6 Clocks

The SMT398-VP module contains a 25MHz LVTTL clock, a clock synthesiser and 1 connector for external LVPECL clock input/output.

- 25 MHz LVTTL oscillator: Main system clock. Can be input in a DCM.
- ICS clock synthesizer 8442, used to generate any frequencies between 31.25 MHz up to 700MHz with a jitter lower than 40ps required for the Rocket I/O transceiver REFCLK input.
- An external differential clock input is provided to the Virtex II Pro FPGA via 2 CONNECTORS differential clock. The traces from the connectors are run as a pair to the FPGA where they are terminated with a 100 ohm resistor.

Mode	Frequency (MHz)	ICS8442 output frequency to SERDES (MHz)	IO bit rate (Gb/s)
Fiber Channel	25	53.125	1.06
		106.25	2.12
Gigabit Ethernet	25	125	1.25
		250	2.5
		156.25	3.125
Infiniband	25	250	2.5
Aurora	Custom	Custom	0.600-3.125
Custom	Custom	Custom	0.600-3.125

Table 1: : Clock synthesizer Configurations for Rocket IO standard application.

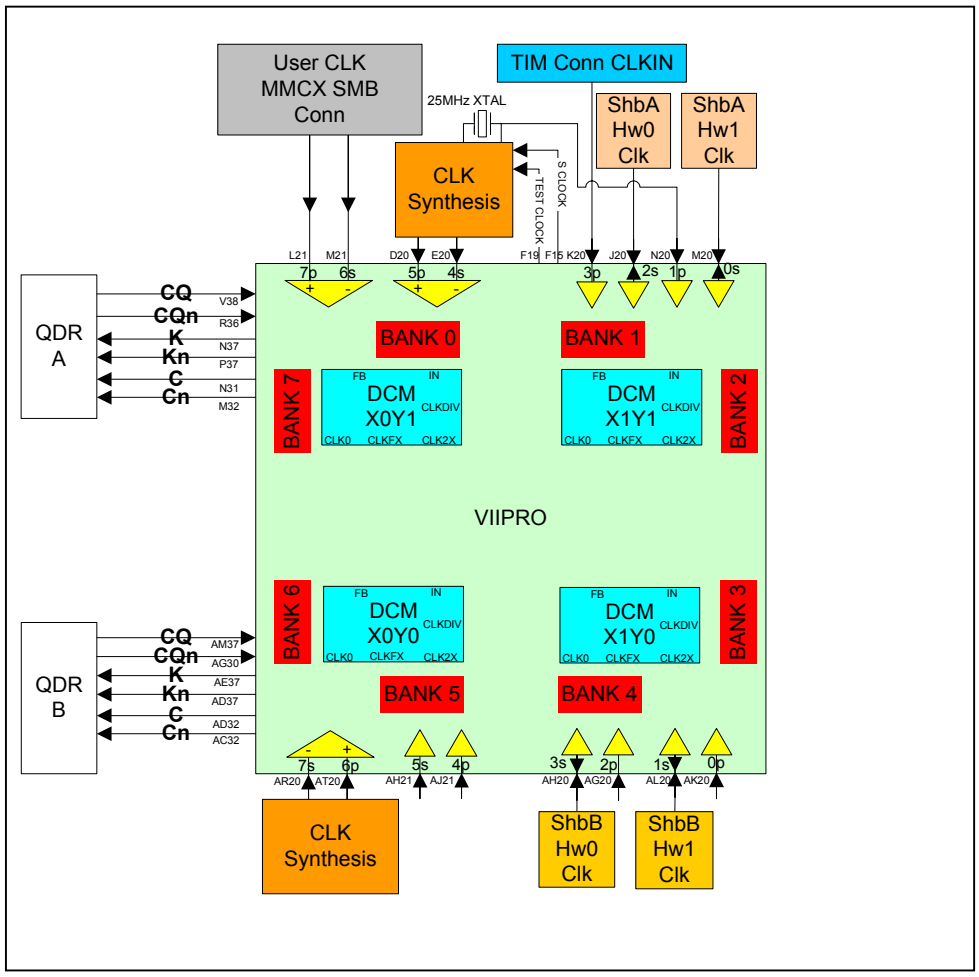

Figure 3: Clocking distribution diagram

3.1.2.1.7 Rocket I/Os

Each MGT has separate transmit and receive functions (full-duplex) and can be operated at baud rates from 600 Mb/s to 3.125 Gb/s.

Additionally, every RocketIO MGT block is fully independent and contains a complete set of common SerDes (serializer/deserializer) functions.

This allows Virtex-II Pro devices to support many existing and emerging serial I/O standards at data rates up to 10 Gb/s (when cumulating 4 channels)

- Up to 16 Rocket I/O transceivers are available in the XC2VP50 -70.
- The SMT398-VP provides 14 MGTs that can be configured to implement different MGT interfaces. A mezzanine board which can plug on the SMT398-VP RSL connectors could provide the right connectors to implement the required serial IO standard, for instance: Infiniband (SMT145) channels, Serial ATA channels and Ethernet channels.
- The minimum transfer rate is 2.5Gbits/s on a Virtex II Pro –6 part.
- 14 DC coupled Rocket I/Os are available on our 2 RSL connectors.

Mode	Channels	IO bit rate (Gb/s)
Fiber Channel	1	1.06
		2.12
Gigabit Ethernet	1	1.25
XAUI (10 Gbit Ethernet)	4	3.125
Infiniband	1, 4, 12	2.5
Aurora	1, 2, 3, 4	0.600-3.125
Custom	1, 2, 3, 4	0.600-3.125

Table 2: Communication standard supported by Rocket IO transceivers

3.1.2.1.8 User I/Os

- 2 SHB connectors
- 2 RSL connectors
- 1 SLB connector

3.1.2.1.9 2 DIP switches

- One four-position DIP switch is connected to the FPGA I/Os for debugging purposes of an FPGA design.
- One four-position DIP switch is connected to the CPLD to provide control over the selection of a Comport or the Xilinx Flash PROM device for configuration and the "TIM Confign" use.

JPC 3,2, 1	JPC3	JPC2	JPC1
C0P	ON	ON	ON
C3P	OFF	OFF	OFF
Flash	Any combination other than above		

JPC 4	TIM Confign
ON	ENABLED
OFF	DISABLED

Table 3: DIP switches

3.1.2.1.10 Leds

- 4 Red Leds connect to the FPGA and are available to the User.
- 1 Green Led connects to the DONE pin of the FPGA to show FPGA is configured. The Led Is turned on when the FPGA is configured.
- 1 Red Led for temperature treshold

3.1.2.1.11 Fan

A fan coupled with a heatsink can be mounted on the Virtex II to provide heat dissipation but a permanent airflow should always be maintained inbox to provide enough cooling for your system. Please ask Sundance when ordering.

3.1.2.1.12 Temperature sensor

The temperature sensor is a LM83 from National semi-conductors

The digital temperature sensor accurately senses its own temperature as well as the temperature of the Virtex-II Pro with a 1 °C resolution.

Coupled with the CPLD it flashes a red Led above a high threshold and shuts down the FPGA power supply in case of overheating.

The threshold temperature is fixed by the CPLD at 85 degrees and the FPGA power is shutdown at 125 degrees. (Maximum Junction temperature. See Virtex-II Pro datasheet module 3 table 1)

3.1.2.1.13 FPGA Configuration

The FPGA can be configured in 3 different ways selectable via switch :

- Using one of the 2 Comports to provide the bitstream:
  - The CPLD is connected to 2 Comport links of the SMT398-VP TIM connector. A switch is used to select the configuration Comport that will be used to transfer the bitstream.
  - The CPLD allows for FPGA configuration in slave SelectMap mode.
- Using the on-board Flash PROM.
  - The CPLD monitors the configuration data between the Xilinx Flash PROM and the FPGA. Xilinx application note xapp693 is used as a reference design.
- Using the on-board JTAG header and Xilinx JTAG programming tools.
  - The JTAG header is a Parallel-IV Header.

3.1.2.2 Power Budget

Device		Quantity	Voltage(V)	Current(mA)	Power(W)	Source
Static Power on termination resistor (50 ohms)		200	1.8	16.0	5.76	Virtex II PRO (ds083 module 3 table 6) HSTL II current specification
Samsung QDR II burst 4 (36-bit interface)		2	1.8	550	1.98	Micron DDRSDRAM Datasheet
25 Mhz Clock oscillator		1	3.3	10	0.033	Jauch VX3 Quartz crystal oscillators datasheet
Clock synthesizer	Digital	1	3.3	155	0.5115	ICS 8442 hih frequency synthesizer
	Analog		3.3	20	0.066	
LEDs		5	3.3	25	0.4125	
DIP Switch		1	2.5	2.1	0.005	Four 4.7 Kohm pullup

For 1 QDR II Bank the termination at the memory is:

1. QQ[35:0] : 36 termination resistors
2. QD[35:0] : 36 termination resistors
3. QSA[19:0] : 20 termination resistors
4. QWn, QRn 2 termination resistors
5. QK, QKn: 2 termination resistors
6. QC, QCn: 2 termination resistors
7. CQ, CQn: 2 termination resistors

So a total of 100 termination resistors per bank.

3.1.2.3 Termination and transmission lines :

No more than 1 split termination type allowed per bank

	Signal	At the FPGA	Terminations at the FPGA	Termination at memory
1	Write Data to memory(QD)	OBUF_HSTL_II_18	SSTL2_II_DCI	HSTL_II_18 Split termination
2	Read Data from memory(QQ)	IBUF_HSTL_I_DCI_18	HSTL_II_18	100 ohm pull-up to 1.3v
3	Data Strobe(CQ, CQn)	HSTL_II_18	SSTL2_II_DCI	50 ohm pull-up to 1.3v
4	Clock(QC, QCn, QK, QKn,)	HSTL_II_18	SSTL2_II_DCI	50 ohm pull-up to 1.3v
5	Address(QSA)	HSTL_II_18	SSTL2_II_DCI	50 ohm pull-up to 1.3v
6	Control(QWn, QRn)	HSTL_II_18	SSTL2_II_DCI	50 ohm pull-up to 1.3v

4 Verification Procedures

5 Review Procedures

6 Validation Procedures

7 Timing Diagrams

7.1 QDRII Memory Timing Diagrams

8 Circuit Diagrams

9 Footprint

9.1 Top View

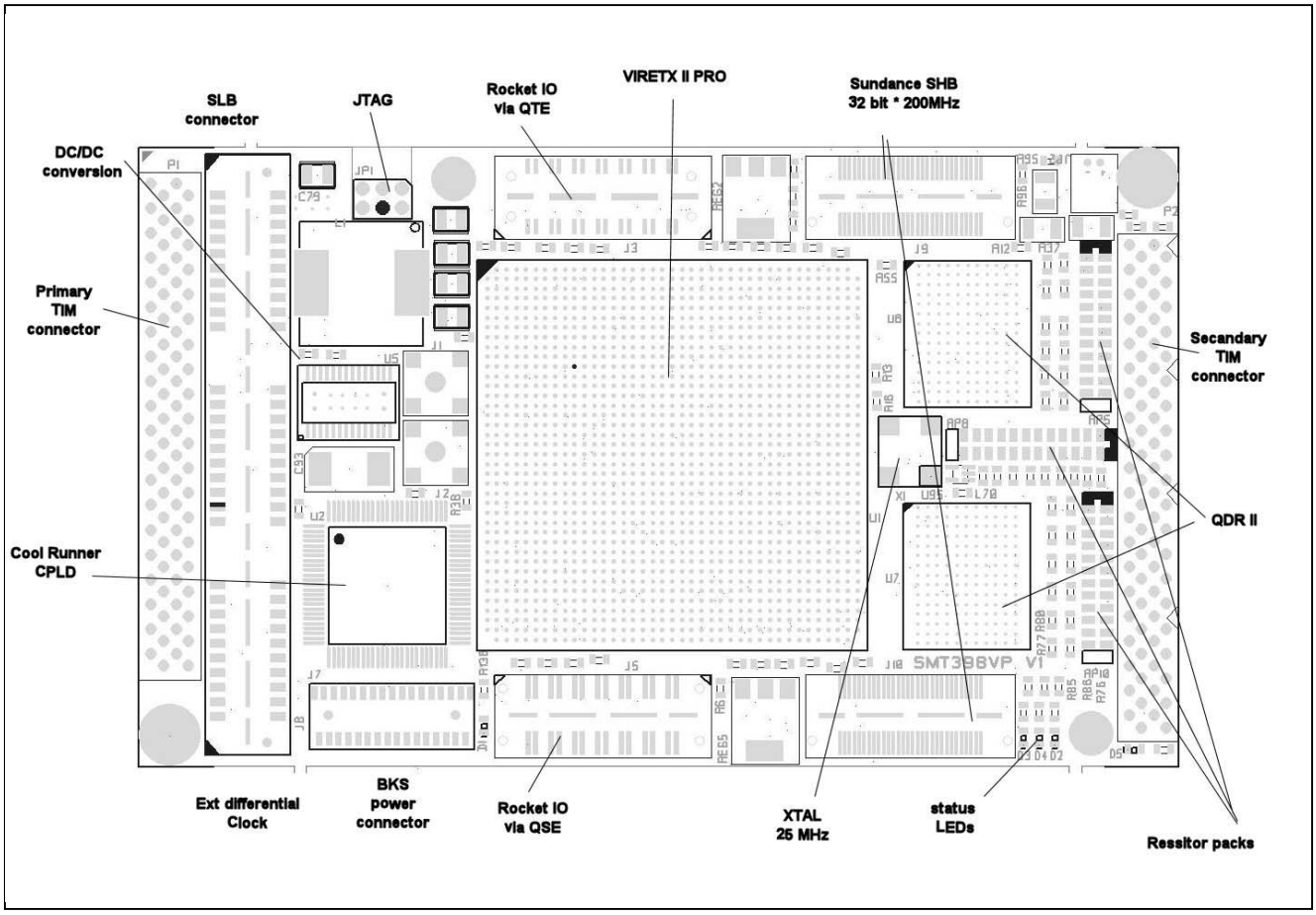

Figure 4: Top View

9.2 Bottom View

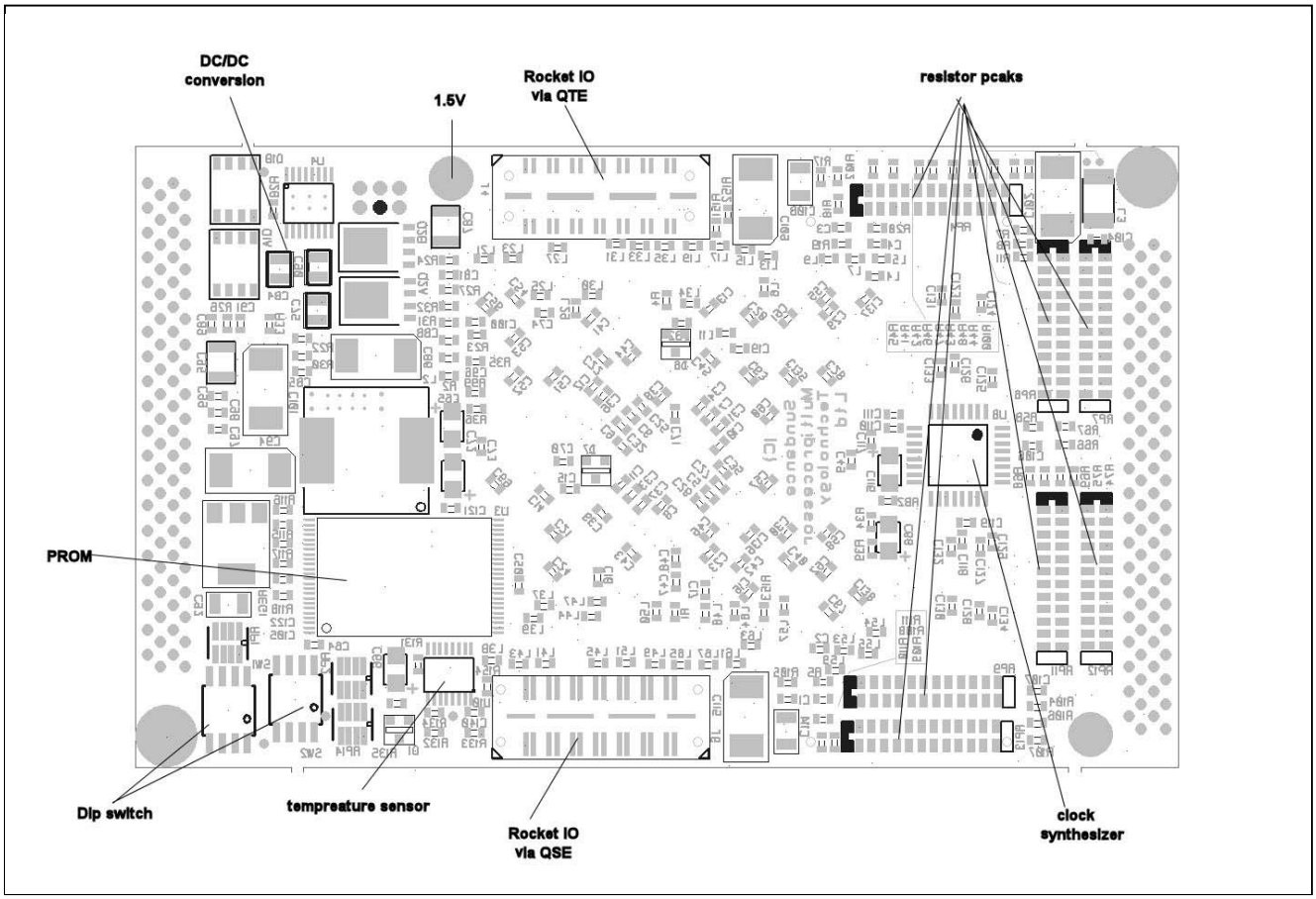

Figure 5: Bottom View

10 PCB Layout Details

10.1 Board layout guidelines:TBD

- Decoupling guidelines.

10.2 Providing additional ground pins

10.3 Component Side

10.4 Solder Side

11 Pinout and Package Requirements

11.1 FPGA Pinout: TBD

11.2 User I/Os

11.2.1 2 SHB connectors

See SUNDANCE SHB specification

11.2.2 2 RSL connectors

See SUNDANCE RSL specification

11.2.3 1 SLB connector

SUNDANCE SLB specification

11.2.4 2 DIP switches:TBD

11.2.5 4 Leds:TBD

12 Safety

This module presents no hazard to the user.

13 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

14 Ordering Information

	Speed grade	-6	-7
Foga	XC2VP50FF1517	SMT398-VP50-6	SMT398-VP50-7
	XC2VP70FF1517	SMT398-VP70-6	SMT398-VP70-7