Unit / Module Name:	Multi-output Clock Generator
Unit / Module Number:	SMT399-160
Used On:	SMT338-VP, SMT398-VP, SMT368, other SLB modules.
Document Issue:	1.0
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Revision History

Issue	Changes Made	Date	Initials
1.0	**Original Document completed based on SMT399PB document**	**24/02/2004**	**PSR**

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1 Introduction

1.1 Overview

The *SMT399-160* is a multi-output mezzanine single width module, which is able to generate sine waves at up to 160MHz. This mezzanine board is to be fitted on one of Sundance SLB (**S**undance **L**VDS **B**us) base modules, such as *SMT338-VP* or *SMT398-VP* or *SMT368* and cannot be used on its own. It is built around two AD9954s, Direct Digital Synthesizer (DDS – Analog Devices) featuring 14-bit DAC operating/sampling at up to 400 MHz. Both devices are separately programmable, can contain up to 4 profiles and have the possibility of being synchronised. The architecture allows generating single-tone or dual-tone signals.

A Xilinx FPGA Virtex-II Pro (or Virtex4) from the base module, is used to control DDSs and Variable Gain Amplifiers (VGAs) of the *SMT399-160*, after receiving command words via a Comport.

SMT399-160 modules can be cascaded and work into the AD9954 Master/Slave mode.

PCB connectors are MMCXs from Hubert Suhner.

It can used in the following application:

- Radio systems, as a clock generator (fine tuning),
- Test systems (dual tone and fast hopping),
- Programmable system (software programmable),
- Etc…

1.2 Related Documents

❍ AD9954 Datasheet - Analog Devices:

http://www.analog.com/Analog_Root/productPage/productHome/0,2121,AD9954,00.html

❍ **S**undance **H**igh-speed **B**us (*SHB*) specifications – Sundance.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification.pdf

❍ **S**undance **L**VDS **B**us (*SLB*) – Sundance.

http://www.sundance.com/docs/SLB%20-%20Technical%20Specifications.pdf

❍ TIM specifications - TI.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf

❍ Xilinx Virtex-II PRO FPGA - Xilinx.

http://direct.xilinx.com/bvdocs/publications/ds083.pdf

❍ MMCX Connectors – Hubert Suhner.

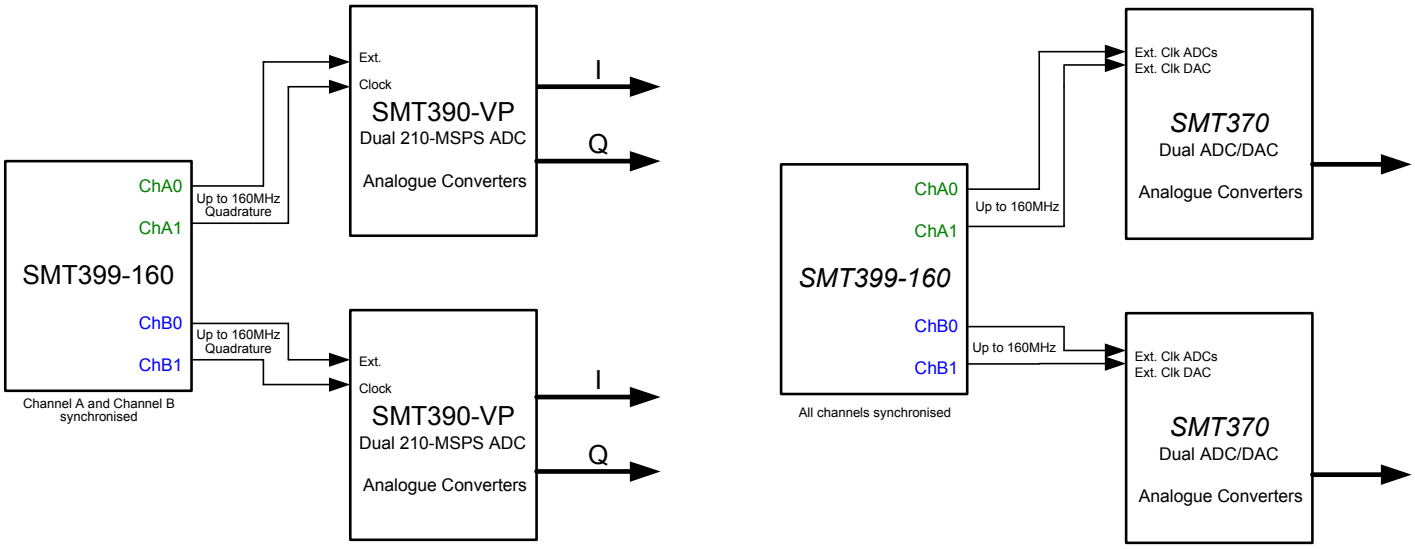
MMCX Connectors

1.3 Examples of application.

The *SMT399-160* module can be used in the following application:

- Radio systems. Compatible with Sundance's TIM Modules, it can be combined with DAQ modules such as ADCs and DACs, as a clock generator. The *SMT399-160* fine-tuning makes it even more suitable for such platform to generate up-to-four synchronised and/or quadrature signals.
- Test systems. It is sometimes very helpful to have a signal generator capable of generators various frequencies to evaluate some radio system. Fast hopping is the key word here. Dual tone signals are useful to characterise a receiver system to evaluate its capabilities of receiving signals close to each other in frequency. DDSs also to generate a ramp, a pattern or a frequency sweep.
- Programmable system. As most of system, it a very important top control every part of a system. The *SMT399-160* is fully controllable via software.
- Etc…

As both pairs of DDSs are synchronised and coupled master/slave, the module can generate 90-degree phase shift signals and be part of a quadrature modulator system.



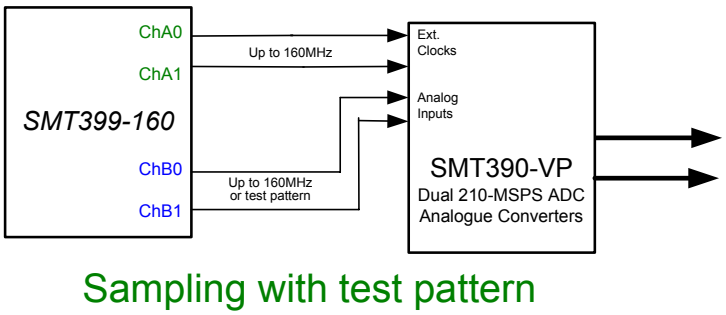


Figure 1 - Examples of applications.

2 Functional Description

In this part, we will see the general block diagram and some comments on the main entities.

2.1 Block Diagram

The following diagram shows the block diagram of the *SMT399-160*.

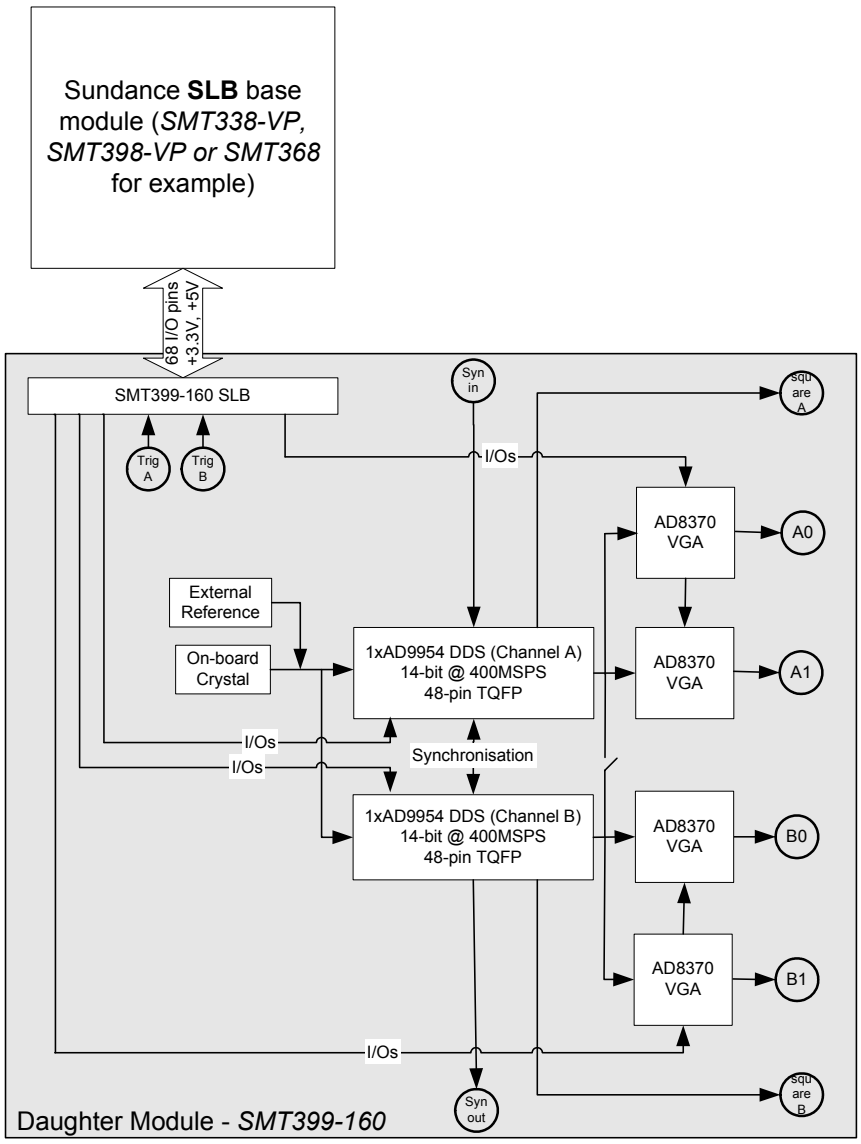


Figure 2 - *SMT399-160* Block Diagram.

2.2 Module Description

The module is built around two **D**irect **D**igital **S**ynthesizers (DDS): two AD9954.

The AD9954 is a DDS featuring 14-bit DAC operating at up to 400MSPS. It forms a digitally programmable high frequency synthesizer capable of generating an analog output sinusoidal waveform at up to 180MHz. The AD9954 provides fast frequency hopping and fine-tuning resolution (32-bit frequency tuning word). The AD9954 includes an integrated 1024x32 static RAM to support flexible frequency sweep capability in several modes. It also supports a user defined linear sweep mode of operation. The frequency resolution of the AD9954 is 0.0931

Hz when clocked at 400MHz. Both analog outputs can be linked together via jumpers in order to generate a dual tone signal.

DDS outputs are doubled and combined with Variable Gain Amplifiers (VGA).

Analog signals are all single-ended and output on MMCX connectors.

Output Sine waves can be turned into 'sharp' square signals using the AD9954 built-in comparator. Square signals (one per DDS) are also available on MMCX connectors.

All DDS settings travel via the FPGA present on SLB base module. Information comes from a Comport and the FPGA stores it first into internal registers and interfaces it to the DDS chips via the SLB connector. Comports follow the Texas Instrument C4x standard.

4 green LEDs are also available and driven by the FPGA to report working or failing conditions to the user. Other green LEDs show that all power supplies are ON and working.

2.3 *SMT399-160* characteristics.

***SMT399-160* outputs.**	
Output voltage range	3.3V p-p – AC coupled (Output level set via Control Register)
Impedance	50Ω - terminated to ground – single-ended
Frequency range	Up to 160 MHz.

Figure 3 - Output main characteristics.

2.4 Power Supply structure.

The *SMT399-160* conforms to the TIM standard for single width modules. The TIM connectors supply 5 Volts to the base module, which also requires an additional 3.3-Volt power supply, which must be provided by the two diagonally opposite mounting holes. This 3.3-volt is present on all Sundance TIM carrier boards. From these two power rails, are generated a filtered 3.3-volt as well as a 1.8-volt source for both AD9954s.

Greens LEDs placed on the board report the state of the power supplies.

2.5 On-board crystal.

The AD9954 are clocked from a crystal (20MHz). The master DDS then passes the sampling clock to the slave DDS to ensure synchronisation. Synchronisation can also be achieved when cascading several *SMT399-160* daughter modules.

2.6 Output Variable Gain Amplifier.

Each output is driven by a **V**ariable **G**ain **A**mplifier (VGA – AD8370), digitally controlled that uses 8 bits to code the gain and provides a power-down mode. Two ranges of gains are available: from –11 to +17dBs or from +6 to +34dBs.

2.7 Daughter sub-module interface.

The link between the main and the daughter sub-module is made via two Samtec connectors. There is no fast signal travelling between both cards. The first connectors passes control signals and the second one passes a 3.3-volt supply and a ground between sub-modules.

The female differential connector is located on the main module. The Samtec Part Number for this connector is QTH-060-01-F-D-DP-A.

The female power connector is located on the main module. The Samtec Part Number for this connector is BKS-133-03-F-V-A

The male differential connector is located on the daughter card. The Samtec Part Number for this connector is QSH-060-01-F-D-DP-A

The male power connector is located on the daughter card. The Samtec Part Number for this connector is BKT-133-03-F-V-A

The mated height between the main module and the daughter card is 5 mm.

2.8 Other Interfaces.

The *SMT399-160* SLB base module (*SMT338-VP, SMT398-VP* or SMT368 as an example), provides other interfaces, such as SHB (**S**undance **H**igh-speed **B**us), RSL (**R**ocket **S**erial **L**ink) or Comport.

Please refer to the documentation of the relevant base modules for more information.

3 Verification Procedures

4 Review Procedures

5 Validation Procedures

6 Timing Diagrams

7 Circuit Diagrams

8 PCB Layout Details

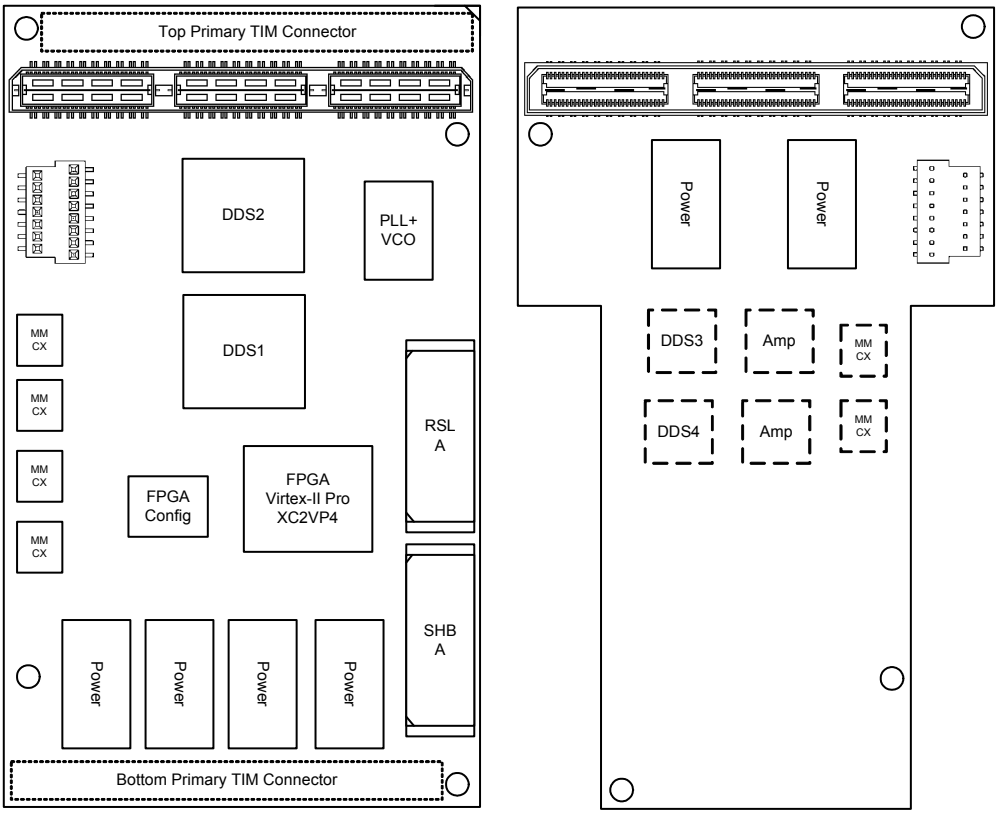


Figure 4 - Sub-module interface (SMT399 on the left and SMT399PB on the right).

9 Pinout and Package Requirements

Here is the pinout for the FPGA (XC2VP-FG256):

Start of Constraints extracted by Floorplanner from the Design

NET "TTLs<3>" LOC = "H16" ;

NET "TTLs<2>" LOC = "D9" ;

NET "TTLs<1>" LOC = "C9" ;

NET "TTLs<0>" LOC = "B9" ;

NET "SHB_WEN" LOC = "F2" ;

NET "SHB_UD<3>" LOC = "F3" ;

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NET "SHB_UD<2>" LOC = "F4" ;
NET "SHB_UD<1>" LOC = "F5" ;
NET "SHB_UD<0>" LOC = "E4" ;
NET "SHB_REQ" LOC = "A9" ;
NET "SHB_DATA<15>" LOC = "E2" ;
NET "SHB_DATA<14>" LOC = "E3" ;
NET "SHB_DATA<13>" LOC = "C2" ;
NET "SHB_DATA<12>" LOC = "C3" ;
NET "SHB_DATA<11>" LOC = "B3" ;
NET "SHB_DATA<10>" LOC = "C4" ;
NET "SHB_DATA<9>" LOC = "A2" ;
NET "SHB_DATA<8>" LOC = "A3" ;
NET "SHB_DATA<7>" LOC = "D5" ;
NET "SHB_DATA<6>" LOC = "C5" ;
NET "SHB_DATA<5>" LOC = "E6" ;
NET "SHB_DATA<4>" LOC = "E7" ;
NET "SHB_DATA<3>" LOC = "D7" ;
NET "SHB_DATA<2>" LOC = "C7" ;
NET "SHB_DATA<1>" LOC = "C8" ;
NET "SHB_DATA<0>" LOC = "A8" ;
NET "SHB_CLOCK" LOC = "D8" ;
NET "SHB_ACK" LOC = "F1" ;
NET "PLL_MUXOUT" LOC = "L4" ;
NET "PLL_LE" LOC = "L3" ;
NET "PLL_DATA" LOC = "L2" ;
NET "PLL_CLK" LOC = "L1" ;
NET "PLL_CE" LOC = "L5" ;
NET "nRESET" LOC = "N9" ;
NET "LEDs<3>" LOC = "H14" ;
NET "LEDs<2>" LOC = "H13" ;
NET "LEDs<1>" LOC = "G12" ;
NET "LEDs<0>" LOC = "G16" ;
NET "JUMPER" LOC = "H15" ;
NET "DDSD_SDO" LOC = "J13" ;
NET "DDSD_SDIO" LOC = "K15" ;
NET "DDSD_SCLK1" LOC = "M16" ;
NET "DDSD_SCLK0" LOC = "L14" ;
NET "DDSD_SCLK" LOC = "K16" ;
NET "DDSD_RESET" LOC = "J15" ;
NET "DDSD_PWUP1" LOC = "M15" ;
NET "DDSD_PWUP0" LOC = "L12" ;
NET "DDSD_PS<1>" LOC = "K13" ;
NET "DDSD_PS<0>" LOC = "K14" ;
NET "DDSD_nCS" LOC = "K12" ;
NET "DDSD_LTCH1" LOC = "M13" ;
NET "DDSD_LTCH0" LOC = "L15" ;
NET "DDSD_IOUPDATE" LOC = "L16" ;
NET "DDSD_IOSYNCH" LOC = "J14" ;
NET "DDSD_DATA1" LOC = "N16" ;
NET "DDSD_DATA0" LOC = "L13" ;
NET "DDSD_CLKMODELSEL" LOC = "J16" ;
NET "DDSC_SDO" LOC = "G1" ;
NET "DDSC_SDIO" LOC = "H3" ;
NET "DDSC_SCLK1" LOC = "K2" ;
NET "DDSC_SCLK0" LOC = "J3" ;
NET "DDSC_SCLK" LOC = "H4" ;
NET "DDSC_RESET" LOC = "G3" ;
NET "DDSC_PWUP1" LOC = "K4" ;
NET "DDSC_PWUP0" LOC = "K5" ;
NET "DDSC_PS<1>" LOC = "H1" ;
NET "DDSC_PS<0>" LOC = "H2" ;
NET "DDSC_nCS" LOC = "G5" ;
NET "DDSC_LTCH1" LOC = "K1" ;
NET "DDSC_LTCH0" LOC = "J2" ;
NET "DDSC_IOUPDATE" LOC = "J1" ;
NET "DDSC_IOSYNCH" LOC = "G2" ;
NET "DDSC_DATA1" LOC = "K3" ;
NET "DDSC_DATA0" LOC = "J4" ;
NET "DDSC_CLKMODELSEL" LOC = "G4" ;
NET "DDSB_SYNCLK" LOC = "P8" ;
NET "DDSB_SDO" LOC = "P9" ;
NET "DDSB_SDIO" LOC = "N8" ;
NET "DDSB_SCLK1" LOC = "P13" ;
NET "DDSB_SCLK0" LOC = "P12" ;
NET "DDSB_SCLK" LOC = "R8" ;
NET "DDSB_RESET" LOC = "M11" ;
NET "DDSB_PWUP1" LOC = "T14" ;
NET "DDSB_PWUP0" LOC = "M10" ;
NET "DDSB_PS<1>" LOC = "N10" ;
NET "DDSB_PS<0>" LOC = "P10" ;
NET "DDSB_nCS" LOC = "N7" ;
NET "DDSB_LTCH1" LOC = "M14" ;
NET "DDSB_LTCH0" LOC = "T15" ;
NET "DDSB_IORESET" LOC = "R9" ;
NET "DDSB_FUD" LOC = "T9" ;
NET "DDSB_DATA1" LOC = "P15" ;
NET "DDSB_DATA0" LOC = "N12" ;
NET "DDSA_SYNCLK" LOC = "T8" ;
NET "DDSA_SDO" LOC = "M2" ;
NET "DDSA_SDIO" LOC = "N1" ;
NET "DDSA_SCLK1" LOC = "M6" ;
NET "DDSA_SCLK0" LOC = "P5" ;
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NET "DDSA_SCLK" LOC = "M1" ;
NET "DDSA_RESET" LOC = "P2" ;
NET "DDSA_PWUP1" LOC = "N6" ;
NET "DDSA_PWUP0" LOC = "T3" ;
NET "DDSA_PS<1>" LOC = "R3" ;
NET "DDSA_PS<0>" LOC = "P3" ;
NET "DDSA_nCS" LOC = "M4" ;
NET "DDSA_LTCH1" LOC = "P7" ;
NET "DDSA_LTCH0" LOC = "N5" ;
NET "DDSA_IORESET" LOC = "M3" ;
NET "DDSA_FUD" LOC = "P4" ;
NET "DDSA_DATA1" LOC = "M7" ;
NET "DDSA_DATA0" LOC = "T2" ;
NET "CP3_STB" LOC = "E13" ;
NET "CP3_REQ" LOC = "E15" ;
NET "CP3_RDY" LOC = "C15" ;
NET "CP3_DATA<7>" LOC = "G14" ;
NET "CP3_DATA<6>" LOC = "G15" ;
NET "CP3_DATA<5>" LOC = "G13" ;
NET "CP3_DATA<4>" LOC = "F16" ;
NET "CP3_DATA<3>" LOC = "F15" ;
NET "CP3_DATA<2>" LOC = "F14" ;
NET "CP3_DATA<1>" LOC = "F13" ;
NET "CP3_DATA<0>" LOC = "F12" ;
NET "CP3_ACK" LOC = "E14" ;
NET "CP1_STB" LOC = "C10" ;
NET "CP1_REQ" LOC = "E11" ;
NET "CP1_RDY" LOC = "D10" ;
NET "CP1_DATA<7>" LOC = "D11" ;
NET "CP1_DATA<6>" LOC = "C12" ;
NET "CP1_DATA<5>" LOC = "D12" ;
NET "CP1_DATA<4>" LOC = "A14" ;
NET "CP1_DATA<3>" LOC = "A15" ;
NET "CP1_DATA<2>" LOC = "C13" ;
NET "CP1_DATA<1>" LOC = "B14" ;
NET "CP1_DATA<0>" LOC = "C14" ;
NET "CP1_ACK" LOC = "E10" ;
NET "CONF_INIT" LOC = "P14" ;
NET "CONF_DIN" LOC = "R14" ;
NET "CLOCK" LOC = "B8" ;
```

10 Safety

This module presents no hazard to the user.

11 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.