DESIGN SPECIFICATION

FOR

SMT399-FXXX

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APPROVAL PAGE

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DOCUMENT HISTORY

Date	Initials	Revision	Description of change
05-Jun-06	BV	0.1	Initial draft based on customer requirements, for review.
13-Jun-06	BV	0.2	Updated calibration, power-down, connector, jitter and phase-delay discussions based on customer input and internal correspondence.
16-Jun-06	BV	0.3	Updated based on initial schematic design. Changed jumper-selection to 0-ohm resistor(s), added test points.

TABLE OF CONTENTS

1. SCOPE

This document describes the design requirements of the SMT399-Fxxx Clock Generation/Distribution Module.

1.1. INTRODUCTION

The SMT399-Fxxx is a single size TIM that generates or distributes a sampling clock to four output connectors. Its purpose is to enable the synchronization of many ADC and DAC devices in systems which require a common clock source across all devices.

The module will consist of a very stable, thermally controlled fixed frequency clock generator and a 4-way 0-phase divider with limited phase delay across the ports.

An external source will be an optional input (instead of the generator) to the divider to allow distribution, or to daisy chain several SMT399-Fxxx boards to increase the number of common clocks.

The various interfaces available on the module are listed below:

- OCXO fixed frequency clock, wide frequency range available (5MHz – 200MHz)
- External clock input, distributed clock output
- OCXO/External selection
- 4-pin power connector for stand-alone operation

1.2. PURPOSE

The module must have the following features:

- Generate 4 clock outputs each of which may clock Sundance ADC's or DAC's.
- As a minimum, compatibility with the SMT364 **must** be provided. One SMT399-Fxxx must be able to drive 8 ADCs on a pair of SMT364[1].
- The frequency stability of the generated clock shall be 0.5ppm (+/-5x10-7) over an operating temperature of 0° to 40° C.
- The frequency shall be accurate to within 0.1ppm (+/-1x10-7) of the desired frequency.
- An external clock can be used with approximately 90° transfer phase delay.
- Powered by the TIM connector or external power (+5V) as needed.
- Provide a second set of mounting holes for stand-alone mechanical mounting.

[1] Each pair of ADCs on the SMT364 can be clocked by one clock input. Thus, 4 identical clocks are needed to drive 8 ADCs.

2. APPLICABLE DOCUMENTS AND REFERENCES

2.1. APPLICABLE DOCUMENTS

2.1.1. External Documents

TI TIM specification & user's guide.

Valpey-Fisher VFTCR Series OCXO Datasheet

MiniCircuits PSC-4-1W Datasheet

Analog Devices AD8367 Datasheet

2.1.2. Internal documents

2.1.3. Project Documents

SOW Fixed Clock Distribution Module, SPAWAR Project N65236-05-P-7949

2.2. REFERENCES

2.2.1. External documents

Molex R/A 4-way Power Connector 53109-0410

2.2.2. Internal documents

2.2.3. Project documents

N.A

2.3. PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

3. ACRONYMS, ABBREVIATIONS AND DEFINITIONS

3.1. ACRONYMS AND ABBREVIATIONS

ADC	Analogue to Digital Converter (Conversion)
DAC	Digital to Analogue Converter (Conversion)
OCXO	Oven Compensated (Crystal) Oscillator
SNR	Signal to Noise Ratio
TIM	Texas Instruments Module

3.2. DEFINITIONS

TIM carrier	A circuit board which contains TIM site(s). Typically these also contain an interface to a host (PCI, VME), or various interfaces for standalone operation.

4. DESIGN

4.1. GENERAL DESCRIPTION

The SMT399-Fxxx is a multi-output single width TIM module, which is able to generate sine waves at up to 200MHz. The board is to be fitted on any suitable TIM carrier, or by providing external power, can be used on its own. It is built around an OCXO high frequency signal source, featuring temperature-compensated operation, extremely low phase noise and controlled aging characteristics.

A 4-way 0° divider provides distribution of the clock signal to the 4 clock outputs.

Multiple SMT399-Fxxx modules can be cascaded to provide 8, 12 or 16 clock outputs.

It can be used in the following applications:

- Radio systems, as a Stratum 3E clock source (fine tuning)
- Beam forming (synchronized acquisition of many ADCs)
- Test systems (as a temperature-independent frequency reference)
- Quadrature clock generation systems

4.2. BLOCK DIAGRAM

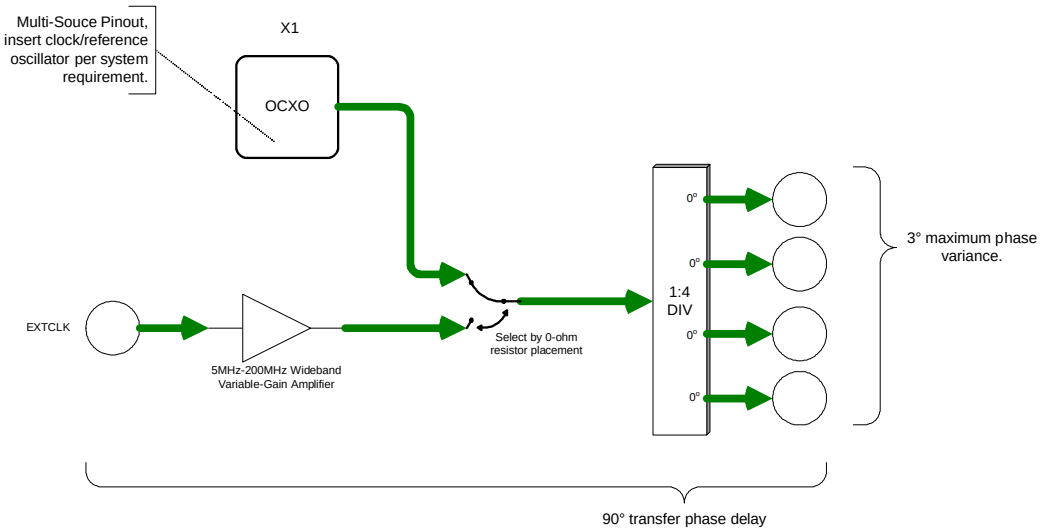

Figure 1 – Overall Block Diagram of SMT399-Fxxx module

4.3. CHARACERTISTICS

The SMT399-Fxxx module shall conform to the following characteristics:

***SMT399-Fxxx* Outputs**	
Output voltage range (min)	0.4V p-p – AC coupled
Impedance	50Ω – single-ended
Frequency range	5MHz to 200 MHz
Phase Variance (across outputs)	3° Maximum

Table 1 - Output Signal Characteristics

***SMT399-Fxxx* Input**	
Input voltage range (min)	0.4V p-p
Impedance	50Ω – single-ended
Frequency range	5MHz to 200 MHz
Transfer Phase Delay (to outputs)	90°
Transfer Phase Variance (board-to-board)	3° Maximum

Table 2 - Input Signal Requirements

4.4. POWER SUPPLY

The SMT399-Fxxx conforms to the TIM standard for single width modules. The TIM connectors supply +5V to the module. An external power connector is fitted which allows the module to be used outside of a TIM Carrier system. From the +5V supply, a filtered +3.3V is generated to power the OXCO and the external clock buffer amplifier.

A green LED is placed on the board to report the state of the power supply.

4.5. CLOCKS

The SMT399-Fxxx is fitted with an OXCO clock source which provides exceptional frequency stability and low phase noise throughout the operating temperature range. The characteristics of the OXCO are as follows:

***SMT399-Fxxx* Oscillator Specifications**			
	MIN	TYP	MAX
Frequency (specify at order)	5MHz		200MHz
Frequency Stability (vs. Temp)		+/- 50ppb	
Aging (per Day/Year)		$1x10^{-9}/3x10^{-7}$	
SSB Phase Noise[2] **10Hz** **100Hz** **10KHz**		 -125dBc/Hz -145dBc/Hz -165dBc/Hz	
Power Consumption (@+3.3V) **Steady state, 25°C** **Start up**		 1W 3.2W	 1.2W 3.5W
Warm-up Time (to 100ppb)		2 minutes	3 minutes
Output Power	+7dBm		

Table 3 - Local Oscillator Specifications

The clock frequency is specified when ordering. The clock circuit has a multiple turn potentiometer to make frequency adjustments to the oscillator output frequency. The adjustment range is approx +/- 1ppm, and is primarily used to counteract the effects of aging. A typical SMT399-Fxxx module will have a service life of 3-6yrs before the frequency adjustment will no longer be able to compensate for aging[3].

4.6. EXTERNAL CLOCK AMPLIFIER

When the external clock input is used, it a variable gain amplifier is used to overcome losses in the 4-way divider stage, as well as the phase delay circuit.

4.7. CONFIGURATION AND INITIALIZATION

The oscillator is calibrated to within 100Hz of the requested frequency at the factory. Special arrangements can be made with Sundance for higher tolerances, for example to within 0.1ppm. The user may adjust the frequency as needed to counteract aging.

A single jumper is provided to allow the user to select an external clock source instead of the OCXO local oscillator. When the jumper is fitted, the external clock source is selected, and the OXCO is ***powered off***.

4.8. ANALOG I/O CONNECTIONS

The clock outputs and external clock input can be specified as MMBX or MMCX style connectors when ordering. Both types of connectors are placed on the module, the choice of which connector is driven is determined by the placement of a 0ohm resistor.

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[2] Specified at 10MHz operating frequency

[3] Standard specification; increased temperature stability and aging characteristics may be available. Contact Sundance.

5. ENGINEERING NOTES

This section describes notes made during the development of this specification and are intended to guide the schematic designer and PCB layout engineer when engineering trade-offs are necessary.

5.1. POWER SUPPLY

A +5V supply voltage was selected because of the requirement to provide regulated +3.3V power to the OXCO and external clock amplifier. The TIM module provides +3.3V, +5V and +/- 12V, but the +12V does not source the amount of current needed to power the OXCO during its warm-up period. +5 are both available on the TIM as well as on the external power connector (standard PC).

The OXCO consumes up to 3.5W during warm-up, while the external clock amplifier will likely dissipate something in the range of ½W. Either the OXCO or the external clock amplifier will be operational at any given time. Supply of the OXCO or the amplifier will be selected by populating a 0-ohm selector pad as necessary.

5.2. CLOCK OSCILLATOR

The OCXO currently selected is the VFTCR-series from Valpey-Fisher. This oscillator was selected because of the excellent stability, phase-noise characteristics as well as its (relatively) shorter lead-time from the competitors.

Originally, the VFTCS-series was specified. This is a surface-mount variant that has a multi-source (standard) package outline. Using this device would allow us to obtain oscillators from a variety of sources such as Greenray and Raltron, etc.

The basic package pad is "22.0 x 25.4 FR4 SMD" and this is a standard. Here is a table of alternate sources in the SMD package variant:

Mfg.	Part Number	Jitter Metric[4]	Peak SNR[5]
Greenray	YH1441-B17-3.3-102.4MHz	0.041ps	91.6dB
Raltron	OX6551A-LX-3-102.400	0.031ps	94dB
SBtron	SBOC25BBS-3.3V-Sine-102.4MHz	0.020ps	97.8dB
Valpey-Fisher	VFTCS-B58L3S-102.4MHz	0.005ps	109dB
Vectron	C4530-D107-SV033-RFS-B1-102.4MHz	0.875ps	65dB

Table 4 - Alternate sources for SMD package OXCO

[4] Computed from the on-line calculator at: http://www.raltron.com/cust/tools/osc.asp

[5] SNR = 20log10(1/(2*PI*Fsignal*Tjitter)) as described in: http://www.analog.com/en/content/0,2886,760%255F788%255F91502,00.html

There is quite a bit of variation between the offerings. While most all the oscillators drop their phase noise down to about -160dBc/Hz at 10 KHz and beyond, the Valpey oscillators achieve a very low -120dBc/Hz right at 10Hz. This accounts for the very low jitter metric, and the subsequent peak SNR that might be achievable when using this oscillator.

It is requested that when layout is performed on the SMT399-Fxxx module, that both the VFTCR-series and VFTCS-series oscillators be accommodated. Only one type of oscillator shall be fitted at once, but having the standard SMD footprint is easy to prepare for now, while providing a multi-source capability in the future.

A geometrical analysis of the two pin-outs shows that the VFTCR pins allow it to be placed ***inside*** the VFTCS outline as the signal traces match up. Power/GND need to be crossed-over, so the PCB layout engineer should be aware of this.

In any case, the VFTCR will be used for the initial batch as the lead time for this part fits within the customer's delivery requirements, so the through-hole pins must be provided.

The clock oscillator provides an electronic frequency adjustment input which can be used to pull the frequency by a small amount, about +/- 1ppm, using a potentiometer. The potentiometer will have a minimum of 10 turns to allow fine tuning of the frequency to 0.2ppm per turn.

5.3. PHASE JITTER CONSIDERATIONS

In section 5.2. above, peak SNR based on average sampling jitter of the ADC clock was discussed. This section discusses practical design considerations necessary for the SMT399-Fxxx connected to real-world ADCs, etc. All ADCs have aperture jitter which limits their SNR. The clock which drives the ADC adds to this jitter which determines the final SNR possible for that clock/ADC pair.

Since the SMT399-Fxxx is intended for highly specialized sampling applications, attention to detail in the switching and the external clock amplifier circuits is important to achieving peak ADC performance. The amount of additional phase jitter that is introduced by these circuits must be controlled and minimized if possible.

As an illustration, reworking the equation[6] in footnote 5 above, using a 102.4MHz sample clock and a desired SNR of 75dB (the peak SNR of the AD6645 used on the SMT364), we obtain a maximum jitter of 0.276ps. This means that to peak SNR capability when using the SMT364, the path from the OCXO through the multiplexer and the 4-way divider must introduce no more than 200fs of jitter to the clock.

Analog Devices has a very good web-based tool to simulate the effects of clock jitter on the SNR of a sampled signal under a variety of different devices and signal conditions.

http://designtools.analog.com/dtSimADCWeb/dtSimADCMain.aspx

[6] Tjitter = 1/(2*PI*Fsignal*10^(SNR/20))

5.4. 4-WAY DIVIDER

A 4-way 0° phase divider is implemented to provide the signal distribution circuit. The two important specifications of the divider are insertion loss and phase unbalance.

The phase unbalance specification must be kept to within 3° across the outputs. This is to maintain synchronicity of the sampling signal across the various ADCs. The insertion loss affects the signal strength of the output signal. The SMT364 require +/- 0.2V (or approx. 0.4V p-p, about 0dBm). The OXCO provides >+7dBm of output signal, which when entering the divider network will drop by 6dB plus the insertion loss.

The MiniCircuits PSC-4-1W divider has been selected for this application, due to its availability.

Mfg.	Part Number	Loss @100MHz	Unbalance @100MHz
MiniCircuits	PSC-4-1W	0.5dB – 1.0dB	3°

Table 5 - 4-way Divider Components

Having a very low phase unbalance is critical to maintaining proper synchronization between the ADC sampling clocks, as well as allowing the daisy-chain of multiple SMT399-Fxxx boards to provide more than 4 synchronized clock outputs.

5.5. EXTERNAL CLOCK AMPLIFIER

An external clock amplifier may need to be used to allow for weak external input clocks to be divided and still meet the input specifications of the ADC/DAC module's clock inputs. This requires some research and design to implement a suitable circuit.

The amplifier currently selected is a variable-gain amplifier, the AD8367. Impedance matching can be resistive (DC coupled) to provide the widest input band. Since the amplifier has a lower noise figure at higher gain values, the additional attenuation (approx 11dB) is a benefit for noise performance.

The gain is adjustable via a multi-turn 1Kohm potentiometer.

Additionally, it is desired to have a 90° phase delay from clock input to clock outputs. Since the 4-way divider is anticipated to induce about 20°-25° of phase delay, an additional phase advance/retard circuit needs to be added to either the input or the output section of the amplifier. Possible circuits to use are T or PI-networks. Some relevant links which may be an aid to the designer are:

http://fermi.la.asu.edu/w9cf/articles/phase/phase.html
http://home.earthlink.net/~w6rmk/antenna/phased/networks.htm
http://www.smeter.net/feeding/phasenet.php
http://www.smeter.net/amplifiers/amplifiers.php
http://www.qsl.net/sv1grb/downloads.htm

5.6. ANALOG I/O CONNECTORS

The OXCO and Divider (input/output) impedances are 50ohm, as are the connectors and transmission lines into and out of this module.

The SMT364 uses MMBX connectors, therefore to avoid the necessity of a custom MMBX/MMCX patch cable; the SMT399-Fxxx will provide an order option to use MMBX or MMCX type of connectors. Most new Sundance modules use MMCX connectors.

The SMT399-Fxxx will fit both MMBX and MMCX connectors on the PCB. The signal path will be determined by a 0ohm resistor near each of the input and output signal traces. The placement of this resistor will determine which of the connectors is active for any given signal. The SMT399-Fxxx module will be built with all resistors populated according to the order option. The customer has the ability to modify their boards if they desire a mixture of connector types.

5.7. DAISY-CHAIN OF SMT399-FXXX MODULES

In order to implement more than 4 synchronized clocks, it is necessary to use (N/4)+1 SMT399-Fxxx modules, where N is the number of clocks desired. This is primarily due to the fact that a certain amount of transfer phase difference must occur in the divider circuit and in the external clock amplifier.

The SMT399-Fxxx has specified that to overall phase difference of the external clock circuit shall be designed to produce a 90° phase delay. This allows for two kinds of usage: A clock distribution system and a quadrature clock generation system.

Within a clock distribution system, a single SMT399-Fxxx would drive several SMT399-F000 modules which do not have an OXCO populated. The SMT399-F000 modules would provide the clock connections, and the primary SMT399-Fxxx would generate the clock signal. In this way, the accumulated transfer phase difference is irrelevant, and the only specification that matters is the phase unbalance on each of the 4-way 0° dividers.

The clock input amplifier circuit must be carefully designed in a temperature-compensated manner so as to reduce the phase unbalance variability between differently produced SMT399-Fxxx modules.

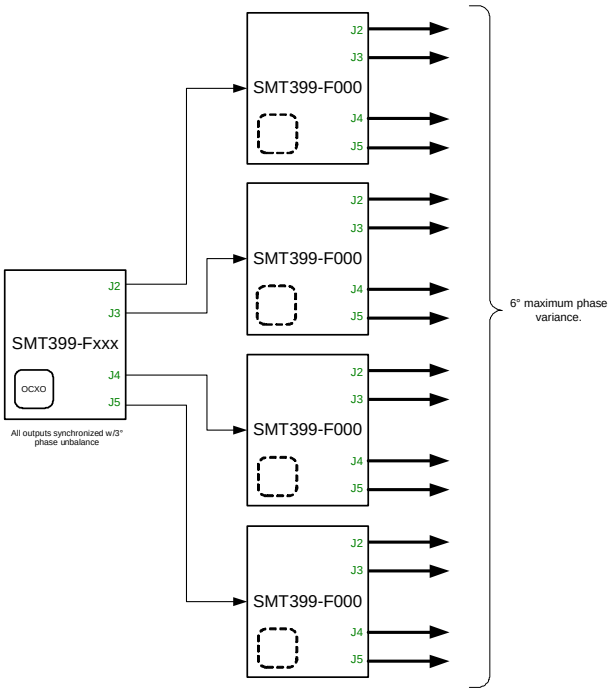


Figure 2 - Generating 16 clocks with the SMT399-Fxxx

When used as a quadrature clock generation system, a single SMT399-Fxxx would drive one SMT399-F000 module. Two of the outputs of the SMT399-Fxxx would be designated as the in-phase clock, while two of the outputs of the SMT399-F000 would be designated as the quadrature clock. Three outputs are not used in this configuration.

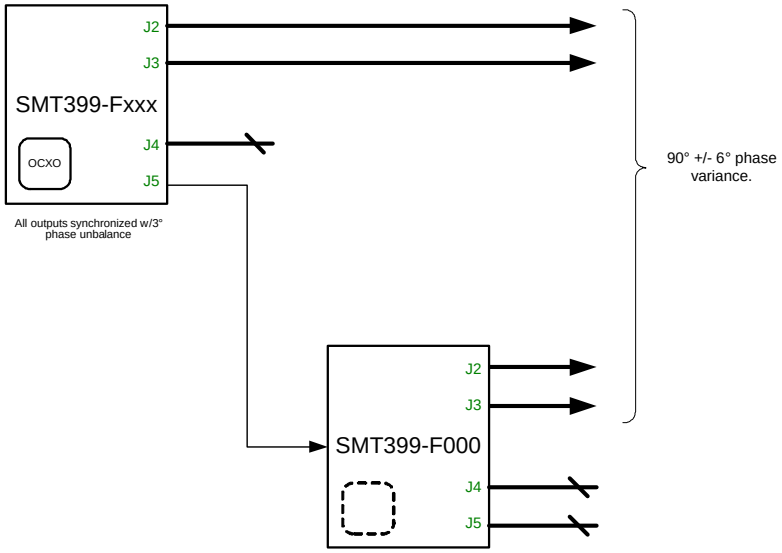


Figure 3 - Generating Quadrature clocks with the SMT399-Fxxx

6. PHYSICAL CHARACTERISTICS

6.1. ELECTRICAL

6.1.1. Power Budget

Device	Quantity	Voltage(V)	Current(mA)	Power(W)	Notes
Wideband amplifier	1	3.3	30	0.100	Analog Devices AD8367
4-way 0 divider	1			0.250	MiniCircuits PSC-4-1W
OXCO clock oscillator	1	3.3	1060 (max)	3.5	VFTCR-B58L3S-XXX.X MHz
LEDs	1	3.3	25	0.0825	
Jumper	1	3.3	0.7	0.002	4.7K ohm pull-up
Voltage Regulator	1			1.75	Micrel MIC29301
Total		5.0	1140	5.7	

Table 6 - Power Estimation

6.2. MECHANICAL

The module shall conform to TIM-40 specifications.

In addition, a second set of mounting holes will be located on the inside of the module (same diameter as primary set) for the purpose of fixing the PCB securely when not used in a TIM carrier system.

6.3. ENVIRONMENTAL

The module shall conform to TIM-40 specifications.

7. FOOTPRINT

7.1. TOP VIEW

7.2. BOTTOM VIEW

8. PINOUT

8.1. ANALOG I/O

Connector	Type	Description
J10	MMBX	External Clock Input
J1	MMBX	Output 1
J3	MMBX	Output 2
J5	MMBX	Output 3
J7	MMBX	Output 4
J9	MMCX	External Clock Input
J2	MMCX	Output 1
J4	MMCX	Output 2
J6	MMCX	Output 3
J8	MMCX	Output 4

8.2. POWER

PIN	Description
1	N/C
2	GND
3	GND
4	+5V

8.3. CONNECTOR SELECTION

Switch	Fit 0ohm	Description
S1	1-3	Enable J1 (MMBX)
S1	2-3	Enable J2 (MMCX)
S2	1-3	Enable J3 (MMBX)
S2	2-3	Enable J4 (MMCX)
S5	1-3	Enable J5 (MMBX)
S5	2-3	Enable J6 (MMCX)
S6	1-3	Enable J7 (MMBX)

S6	2-3	Enable J8 (MMCX)
S4	2-3	Select External Clock
S7	2-3	Select External Clock
S4	1-3	Select OXCO
S7	1-3	Select OXCO
S3	1-3	Select X1 (VFTCR)
S3	2-3	Select X2 (VFTCS)

Note: S4 and S7 must be set together for proper operation.

8.4. LED

Part	Description
D1	+5 Power Good

8.5. TIM-40

PIN (PB1)	Description
2,8,10,16,24,32,40,48,56,64,72	VCC (+5V)
6,11,12,13,14,20,28,36,44,52,60,68,75,76	GND

8.6. TEST POINTS

Location	PIN	Description
TP1	U1.5	Amplifier Gain Adjust
TP2	U1.6	Amplifier Detector Output
TP3	PSC1.4	Sum Port Input to Splitter
TP4	V_REG	Regulator Output
TP5	V_OSC	Oscillator Supply
TP6	V_AMP	Amplifier Supply

9. QUALIFICATION REQUIREMENTS

9.1. QUALIFICATION TESTS

9.1.1. Meet Sundance standard specifications

- Meet the TIM-40 standard specifications

9.1.2. Meet External specifications

- Meet frequency stability specifications over 0° to 40° C operating temperature
- Meet phase variance specifications across all 4 outputs
- Meet phase delay specification for external clock input mode

9.1.3. Meet Quality specifications

- Local oscillator adjustable range 30% of maximum at delivery
- Meet overall phase noise specification

9.1.4. Integration Qualification

- Must work on ALL Sundance platforms as a secondary (non-root) TIM module
- Must be able to work stand-alone (meeting above specifications)

10.SAFETY

This module presents no hazard to the user.

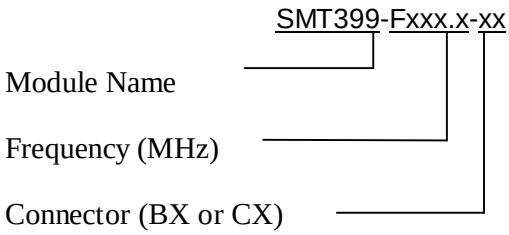
11.EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

12. ORDERING INFORMATION



Example: A 102.4MHz module with MMBX Connectors: **SMT399-F102.4-BX**

NOTE: If daisy-chaining SMT399 modules, only one module requires an oscillator, and the 'slave' modules can be ordered as 'SMT399-F000-xx', as appropriate.