

<b>Unit / Module Name:</b>	Dual DSP PMC Module
<b>Unit / Module Number:</b>	SMT417
<b>Used On:</b>	PMC Carriers
<b>Document Issue:</b>	See Revision History
<b>Date:</b>	See Revision History

# CONFIDENTIAL

<b>Approvals</b>		<b>Date</b>
Managing Director		
Software Manager		
Design Engineer		

Sundance Digital Signal Processing Inc, 4790 Caughlin Parkway #233, Reno, NV 89509-0907, USA.  
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Certificate Number FM 55022

## Revision History

	<b>Changes Made</b>	<b>Issue</b>	<b>Initials</b>
5/30/06	First Draft, from 407	0.0	FRH
06/09/06	Revised RSL, added SMA connector, removed SLB, updated JTAG description, added external power connector, compliance references.	0.1	BV
6/16/06	Merged QL JTAG into Xilinx chain for manufacturing testing. Separated QL/DSP clocks. Identified RSL allocation for different Virtex devices.	0.2	FRH
6/22/06	Updated top-level block diagram. Clarified FPGA block diagram and switch operation. Updated Sec 2.4 regarding XMC standard. Added several illustrative figures.	0.3	BV

## List of Abbreviations

Abbreviation	Explanation
ASIC	Application Specific Integrated Circuit
BOM	Bill Of Materials
CMC	Common Mezzanine Card
Comport	Communications Port
DSP	Digital Signal Processor
FMS	Trade name for a flat-ribbon cable family from JST Mfg. Inc.
FPDP	Front Panel Data Port
FPGA	Field Programmable Gate Array
NA	Not Applicable
OTP	One-Time Programmable
PC	Personal Computer
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PMC	PCI Mezzanine Card
PrPMC	Processor PMC
RF	Radio Frequency
RSL	Rocket Serial Link
SDB	Sundance Digital Bus
SDRAM	Synchronous Dynamic Random Access Memory
SHB	Sundance High-speed Bus
SLB	Sundance LVDS Bus
SMA	Trade name for a threaded RF co-axial connector family
SMT	Sundance Multiprocessor Technology
TBD	To Be Determined
TI	Texas Instruments
XMC	Switched Mezzanine Card

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# 1 Introduction

## 1.1 Overview

This document describes the implementation of a PMC module with two fixed-point DSPs, one large FPGA, and other interfaces described below. The details of this specification will include hardware and programmable logic aspects.

## 1.2 Module Features

The main features of the *SMT417* are listed below:

- § Two [TI 6416T](#) DSPs with independent SDRAM
- § Xilinx [Virtex II Pro](#) (FF1152 package)
- § Provision for data processing in FPGA
- § One XMC connector with 8 RSL data links
- § Two FMS connectors
- § Standard single-size PMC module
- § 66MHz 64-bit PCI interface with over 500MB/s data rate
- § Standard Sundance software interface

Additional features meeting ANSI/VITA 32 (PrPMC) spec for tall modules:

- § Two [SHB](#) AND one [RSL](#) (7x bidirectional RocketIO) interface for easy interconnection to Sundance products.
- § One (1x bidirectional RocketIO) to a Samtec [GRF1-J](#) connector for interfacing to Xilinx RocketIO connectivity boards and other custom multi-gigabit serial interface hardware.

## 1.3 Related Documents

[1] **PCI Mezzanine Card (PMC)** Specification – IEEE 1386-2001.

[http://standards.ieee.org/reading/ieee/std/busarch/1386-2001\\_and\\_1386.1-2001.pdf](http://standards.ieee.org/reading/ieee/std/busarch/1386-2001_and_1386.1-2001.pdf)

[2] **Sundance High-speed Bus (SHB)** Specification – Sundance.

<http://sundance.com/docs/SHB%20Technical%20Specification.pdf>

[3] **External Interface User Manual** – Sundance.

<http://sundance.com/docs/Firmware.pdf>

[4] **Rocket Serial Link (RSL)** Specification – Sundance.

[http://www.sundance.com/docs/Specification\\_RSL.pdf](http://www.sundance.com/docs/Specification_RSL.pdf)

[5] **Processor PMC (PrPMC)** Specification – VITA 32.

<http://www.vita.com/specifications.html>

[6] **(FMS)** Specification - Sundance

<ftp://ftp2.sundance.com/Pub/documentation/pdf-files/comm-port.pdf>

[7] **Switched Mezzanine Card (XMC)** Specification- VITA 42

<http://www.vita.com/specifications.html>

## 2 Functional Description

### 2.1 Module Overview

The following figure details the block diagram of the SMT417.

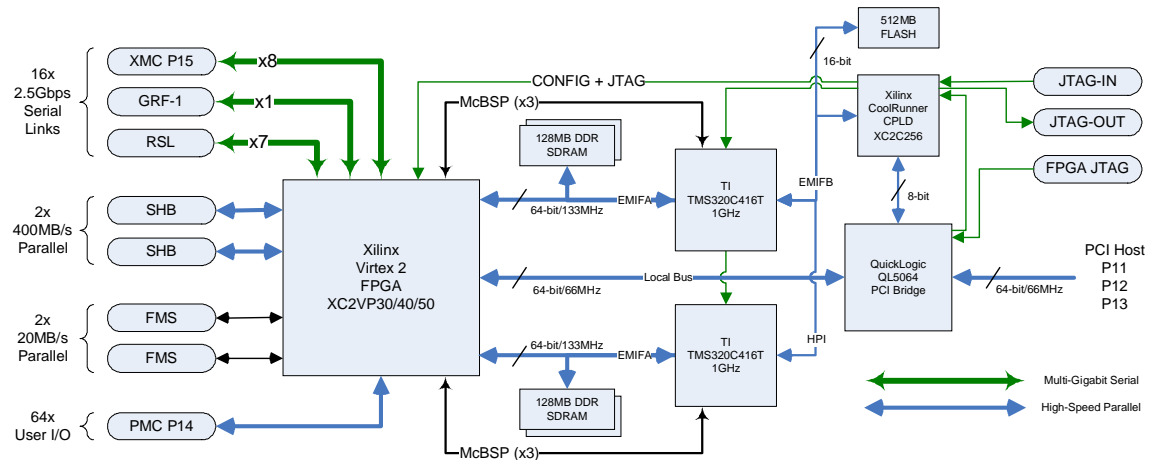


Figure 1 - Block diagram of the SMT417.

The SMT417 allows for parallel DSP computation on data acquired from PCI, SHB or RSL interfaces while conforming to a single-sized PMC form factor.

### 2.2 Hardware Features

#### 2.2.1 TI 6416

Two Texas Instruments 320C6416T DSPs, up to 1GHz, are present in this design. Both DSPs will have equal access to the PCI bus via logic within the Virtex FPGA. DSPA will be responsible for initial configuration of DSPB, and will have the ability to configure the FPGA.

#### 2.2.2 PCI Bridge

The PCI bridge is a separate hardware component. It is implemented as a QuickLogic 5064 device which includes a hard PCI ASIC as well as an OTP fabric. The QL5064 FPGA is preconfigured with the dedicated “Companion Design” logic from QL, which provides a very efficient multi-master 64-bit bus interface to the FPGA and allows the FPGA full access to the DMA controllers, single-access PCI controller, and the target read/write buffers. The QL5064 also has the ability to configure the FPGA and to access the DSP JTAG chain. In cases where no host is present, and therefore the state of the QL5064 is unknown, the rest of the board may continue to configure and run normally.

#### 2.2.3 Memory

Flash memory attached exclusively to DSPA/EMIFB provides boot code and FPGA configuration data. Each DSP has separate banks of SDRAM for local processing on EMIFA. Up to 128MB of 64-bit SDRAM per DSP may be populated on the board, based on two 512Mbit x32 parts per DSP (Total of 256MB on board).

#### 2.2.4 JTAG

A PCI-addressable CPLD provides JTAG access for Code Composer compatibility. Hardware is provided such that TI Code Composer can control the DSPs on the module without need for additional cables.



## 2.2.5 FPGA

### 2.2.5.1 FPGA block diagram

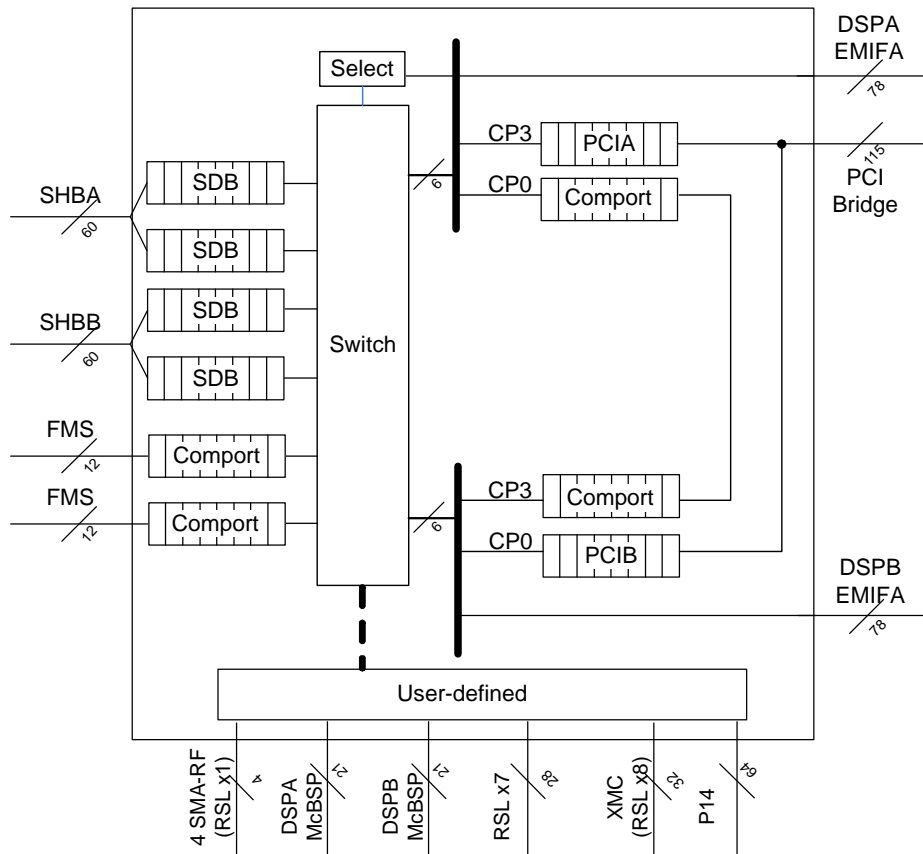


Figure 2 - Block diagram of SMT417 FPGA (standard firmware)

The basic architecture of the FPGA implements an EMIF target interface to each of the DSPs. Each DSP accesses its resources independently and concurrently of the other. Resources such as comports, SDBs, the PCI interface and the user-defined blocks are memory mapped into the DSPs EMIF. The DSP's DMA engines and device drivers are responsible for pushing or pulling data to and from the resources respectively.

The switch is statically configured by DSPA after reset, and remains set for the duration of operation (until the next reset). Standard Sundance device drivers on the DSP have the capability of supporting up to 4 SDB ports and up to 6 Comport link ports mapped on the EMIF of any given DSP processor. Control of the switch is a memory mapped register whose value can be defined in flash and programmed by the boot loader.

User-defined resources can be mapped into the EMIF as appropriate and necessary for the customer application.

### 2.2.5.2 Comports

Comports will be implemented in order to allow communication between the DSPs. When running 3L Diamond software a Comport is required for loading applications. Each DSP will have an independent set of Comport interfaces; Comport0 of DSPA will be bridged to Comport3 of DSPB to allow standard Diamond software to function normally.

Each Comport includes a status register indicating the current port direction and number of FIFO entries (for each direction). The Comport will be implemented with 32-word bi-

directional FIFOs. Interrupts generated by the Comports will be routed through standard Sundance interfaces.

### 2.2.5.3 PCI

A Comport-like interface will also be provided to interface each DSP to the PCI bridge. The differences between this interface and a standard Comport is the 64-bit data path and the FIFO buffering depth. The 64-bit data path from each DSP EMIFA, through the FPGA, to the PCI bus allows for maximum performance using currently established software implementations. The interface between the FPGA and PCI bridge is determined by the speed grade of the QL5064 device that is ordered. This will be a minimum of 60MHz, and typically 66MHz.

### 2.2.5.4 SHB

The SMT417 can include two Sundance High-speed Bus (SHB) interfaces, both on side two of the board. They are connected directly to the FPGA device, and can support data rates of 100MHz. The SHBs can be configured for data widths of 8, 16, or 32-bits. The SHB FIFO is 512 words deep, and bi-directional.

The SHB interface will generate interrupts to the DSP when a predefined number of words are available in the FIFO. SHB interrupts will be routed through standard Sundance interfaces.

The default configuration will be for each SHB to implement 2 SDBs. Either DSP may control either SHB through software setting of the switch matrix.

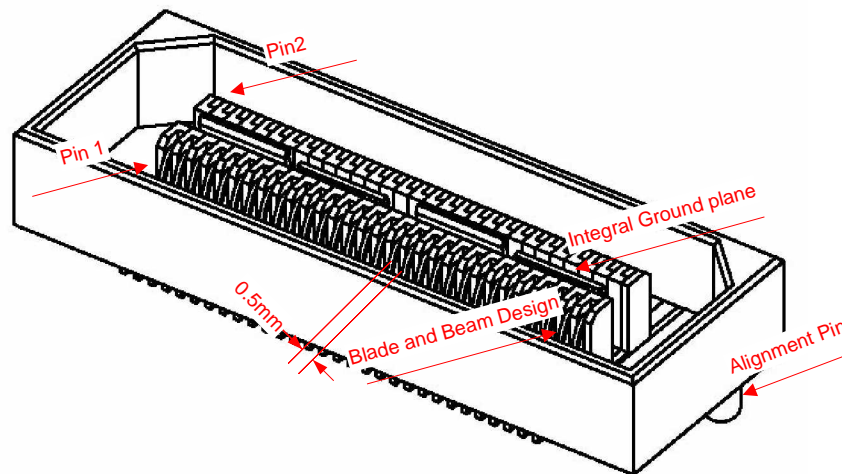


Figure 3 - SHB Connector

Note that if the SHB connectors are mounted (a build-time option), the module becomes governed by the ANSI/VITA 32 specification (PrPMC). This may preclude spacing the PMC carrier boards in adjacent slots.

### 2.2.5.5 Interrupts and miscellaneous I/O

Registers grouped under this heading serve to provide two basic functions: interrupt routing and I/O interfaces. The interrupt control registers (ICR) allow interrupts from any Comport or SHB or PCI I/O interfaces to be mapped to any of the four external interrupts connected to the DSP.

### 2.2.5.6 FMS

2 FMS connectors are provided on side 1 of the board.

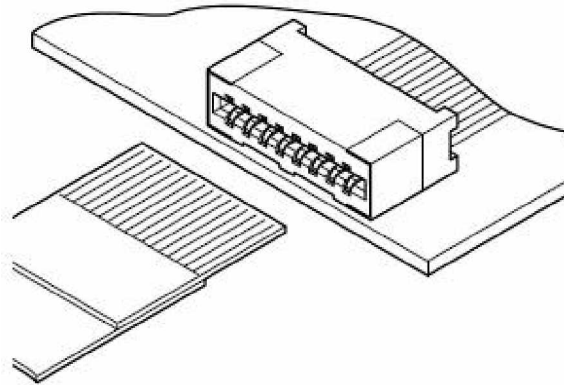


Figure 4 - FMS Connector Detail

These are connected to Comports inside the FPGA, and can be routed as described in Figure 2, above. These are provided to make simple integration with other Sundance carrier boards to create multiprocessor systems.

### 2.2.5.7 XMC

One XMC primary (P15) connector is also provided on side 1, implementing 8 Rocket-Serial-Link (RSL) interfaces.

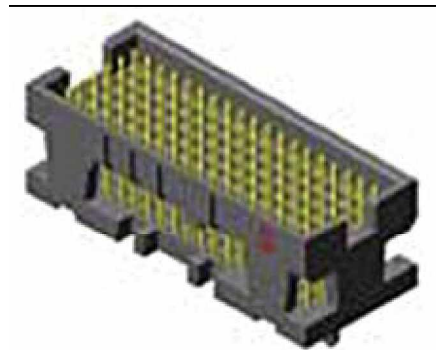


Figure 5 - XMC Connector Detail

### 2.2.5.8 JTAG

The ANSI/VITA 42 specification governs how the JTAG signals are to be treated. The board will not attach any devices to the PMC or XMC JTAG pins, but will route TDI->TDO to maintain integrity of any chains on the carrier boards. All manufacturing tests of the SMT417 are performed using the dedicated JTAG header.

### 2.2.5.9 User-defined I/O

Each DSP will provide the following interfaces to the FPGA:

- 3x McBSP

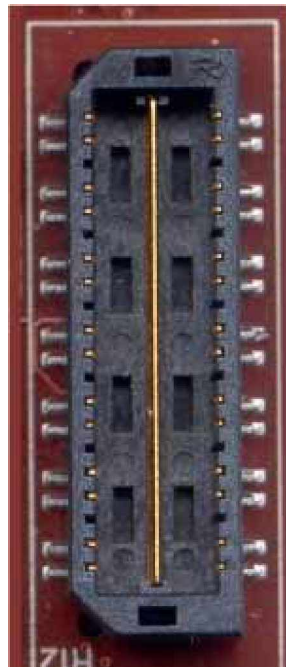
The following external interfaces will be provided for user-defined functions:

- q PMC P14 (64-bits including 2 global clocks). This port will be made 5V tolerant through the use of “zero-delay” bidirectional FET switches. *NOTE, these are the **only** 5V tolerant pins that interface directly to the FPGA. All other external interfaces must be clamped to 4.5V.*

#### **2.2.5.10 RSLs**

Three Rocket Serial Link interfaces are present in this design.

1. A Sundance RSL connector with up to 7 bidirectional links routed to it. Note, that the RLS specification defines only 6 bidirectional pairs, but the connector allows for 14 signal pairs, so the 7<sup>th</sup> link is connected.
2. The XMC connector implements 8 bidirectional links according to ANSI/VITA 42.2 (Serial RapidIO for XMC)
3. A set of 4 coaxial connectors in a high-density mounting (5mm x 32.20mm) from Samtec. The [GRF1-J](#) PCB connector mates with a [GRF1-C](#) cable end to provide a means to expose a single 1x bidirectional RSL.



**Figure 6 - Sundance RSL Connector Detail**

#### **2.2.5.11 External Power**

The SMT417 derives its supply voltage from the PMC/XMC bus. Many customers desire to use the board in a stand-alone (non PMC/PCI) mode. For this purpose, a connector can be optionally fitted to provide the +3.3V and +5V voltages from which the operating voltages are derived.

## 2.3 PMC Standard

### 2.3.1 General

PMC is a variant of CMC that uses PCI to communicate over the backplane. The IEEE CMC standard describes both single- and double-size mezzanine cards. The SMT417 will be a single-size card.

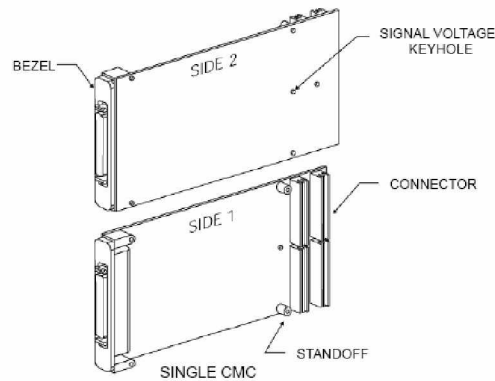


Figure 7 - Single-size PMC card (from IEEE 1386-2001)

Dimensions of the single-size CMC are 74.0mm wide by 149.0mm deep. *Note that the SMT417 does not provide any front panel connectors or ports, as per the ANSI/VITA 20 (conduction cooled specification).*

### 2.3.2 Voltage keying

The QuickLogic 5064 bridge is both 3.3V and 5V compliant. Both keying holes will be provided. *Note that the SMT417 requires **both** 3.3V and 5V power to function.*

### 2.3.3 Connectors

According to IEEE 1386.1-2001 connectors Pn1 through Pn3 are required for 64-bit PCI connectivity. Additionally, connector Pn4 shall be provided for 64 bits of user-defined I/O. Given that the SMT417 is a single-size card, these connectors are referenced P11 through P14.

### 2.3.4 Component heights

Heights of components on PMC Side 1 (see Figure 3) are limited to 4.7mm except in the I/O Area (where they may extend to the host module surface). Components on PMC Side 2 (see Figure 3) are limited to 3.5mm minus PCB thickness, or about 2.0mm (assuming 1.5mm PCB thickness).

Given that neither the DSPs nor FPGA meet the clearance requirement, only the slightest parts such as memories and discretes will be allowed on Side 2. Note that the SMT417 has build options which place certain connectors onto Side 2. When ordered in this way, the SMT417 conforms to ANSI/VITA 32 (PrPMC), which allows 10mm to 20mm of height above the PCB for components on Side 2.

### 2.3.5 Standoffs

There shall be two standoffs as part of the module. The standoffs should be of standard 10mm height in order to support the broadest range of host modules.

### 2.3.6 Power Consumption

Due to the close packing of components between PMC Side 1 and the host module, power consumption is limited to 4.0W for 10.0mm standoffs (this increases to 6.0W for 13.0mm standoffs). The total consumption for Side 1 and Side 2 of the module shall not exceed 7.5W.

The following information shall be provided on the PMC card:

- 5V current drawn, peak and average
- 3.3V current drawn, peak and average

*Note: While it may appear that a stacking height of 13.0mm is desirable, some hosts may not accept this.*

*Note: Depending on the operating frequency and user-defined FPGA designs implemented, the SMT417 is easily capable of exceeding the recommended power dissipation limits. Careful planning at both the software and firmware levels is required when integrating the SMT417 into end-user systems.*

### 2.3.7 Cooling

The SMT417 is designed to be used with conduction-cooled PMC carriers and systems. The specifications governing this are defined by ANSI/VITA 20-2001. The specification defines certain areas on the PMC board to be reserved free of components, to contain significant amounts of metal for thermal conductivity and to provide numerous through-hole terminals for attaching thermal and stiffening components.

### 2.3.8 Grounding

Per section 4.14 of IEEE 1386-2001.

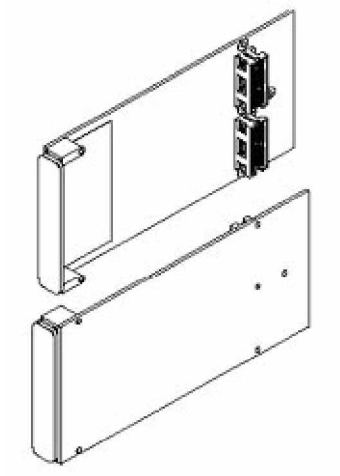
### 2.3.9 Compliance

The SMT417 shall conform to EN61000-4-2 for EMC and ANSI/VITA 47-2005 for other mechanical and environmental requirements.

## 2.4 XMC Standard

### 2.4.1 General

XMC is an extension of CMC that uses implements multi-gigabit switched serial connections to the backplane. The ANSI/VITA 42 standard describes both single- and double-size mezzanine cards. The SMT417 will be a single-size card implementing an 8-lane interface to the XMC connector.



**Figure 8 - Single-size XMC card (from ANSI/VITA 42)**

### 2.4.2 ANSI/VITA 42.2 Serial RapidIO Protocol Layer Standard

ANSI/VITA 42.2 defines requirements and considerations for implementing Serial RapidIO over XMC to switched serial carriers. The SMT417 **will be** electrically compatible with this

standard. Two x4 links will be available to the connector. A user will have the option of introducing a Serial RapidIO core to the FPGA on the SMT417 to allow it to interact with the fabric.

### 2.4.3 ANSI/VITA 42.3 PCI Express Protocol Layer Standard

ANSI/VITA 42.3 defines requirements and considerations for implementing PCI Express over XMC to switched serial carriers. The SMT417 *may be*<sup>1</sup> electrically compatible with this standard. One x8 link will be available to the connector. A user will have the option of introducing a PCI Express core to the FPGA on the SMT417 to allow it to interact with the fabric.

## 2.5 Power Supplies

The SMT417 shall conform to the PMC standard for single-size modules. The PCI connectors supply the module with 5.0V and 3.3V power supply. The 3.3V will be used to supply all LVTTTL digital I/O voltages directly, including the FPGA I/O rail  $V_{CCO}$ . The FPGA Core Voltage ( $V_{CCINT} = 1.5V$ , up to 10A) and DSP Core Voltage ( $V_{DSP} = 1.2V$ , up to 5A) are generated from the 5.0V by high-efficiency DC/DC converters. To avoid problems with the FPGA, the ramp rate of  $V_{CCINT}$  is limited by soft-start circuitry to between 200us and 50ms.

The FPGA Auxiliary voltage ( $V_{CCAUX} = 2.5V$ ) is derived from 3.3V using a linear LDO regulator to minimise losses.

2.5V Power for the Rocket-IO sections of the FPGA is supplied by two independent linear regulators,

*Note: On 11/17/04, the Virtex-IIPro datasheet was amended, removing the requirement for special power-supply sequencing. From the v4.5 datasheet: "VCCAUX and VCCO can power on at any ramp rate. Power supplies can be turned on in any sequence."*

## 2.6 Reset Hierarchy

The SMT417 shall obey the reset signal provided by the PCI connector; however this signal will only reset the QL5064. If desired, the DSPs and FPGA may be reset via PCI control through the CPLD interface. Additionally, the DSPs may also reset the FPGA. In any case the FPGA reset should not be released until the FPGA configuration has completed. Proper operation of the board in a stand-alone configuration (no PCI host present, no PCI clock) will be insured by use of a dedicated reset generator.

There are two fundamental scenarios at power-on:

1. PCI-controlled: The PCI bus resets the QL5064. Following PCI enumeration the driver software asserts reset to the DSPs and FPGA, configures the FPGA, loads code into DSPA and/or DSPB via JTAG, and releases the resets. Note that in this case, if there is valid code in the flash memory, the DSPs may start to execute code before the host PC has gotten around to asserting reset. This is a necessary consequence of supporting the following non-PCI case, where the state of the QL5064 is undefined. If this could be a problem, a "NOP" program should be loaded into the flash memory.
2. "Embedded The PCI bus may or may not be connected. Following the expiration of the on-board reset timer, DSPA begins to execute code from the flash memory. This code likely contains a configuration for the FPGA which will be loaded by DSPA, as well as code to be loaded into DSPB through that processor's host port. DSPB will

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<sup>1</sup> Primary requirement for the product is ANSI/VITA 42.2; electrical compatibility with ANSI/VITA 42.3 will be provided resource permitting. [There are several additional signaling pins that take on special meaning between the various protocols].

not begin execution until commanded to do so by host-port control. Once the FPGA and DSPB have been configured, the two DSPs may communicate with each other through the FPGA, and other peripherals through various comports.

## 2.7 Clock sources

There are several independent clock sources on the SMT417:

1. PCI Clock: From the external PCI host, this clock is connected only to the QL5064. This clock may be idle if no external host is present.
2. QLCLK: The clock for the FPGA side of the QL5064, a dedicated crystal oscillator provides up to 66MHz (default, max for the QL5064 Companion Design). This clock is distributed to the QL5064, the Virtex FPGA and the control CPLD.
3. DSPCLKA/B: Both DSPs have a fixed 50MHz clock input, and may be configured to run at an internal clock rate which is any supported multiple of this frequency. For a 1G device this includes 1GHz (x20), 600MHz (x12), and 300MHz (x6); for all other speed grades the internal DSP clock may be 600MHz or 300MHz. The crystal oscillator may be populated with a different value to support other DSP clock speeds.
4. EMIFCLK: Both DSPs are supplied with a single clock to use with the two EMIF ports. If the DSP is operating at no more than 800MHz, the user has the option of generating the EMIF clock by dividing-down the DSP clock by 6, or by using the external clock. Whichever clock is chosen by software will be passed to the external devices through the ECLKOUT pins. EMIFA and EMIFB may be configured separately. If the DSP clock is faster than 800MHz, then the external EMIF clock must be selected for both EMIFA and EMIFB. The frequency of the EMIF crystal may be selected at build time based on the speed of the SDRAM devices installed, (133MHz default). The EMIFB clock input runs at  $\frac{1}{2}$  the rate of the EMIFA clock input.

## 2.8 JTAG chains

(See "JTAG Headers" section below)



### 3 Description of Interfaces

#### 3.1 PCI

A 66MHz 64-bit PCI bridge allows the SMT417 to communicate with the host module. Given this bus architecture, transfer rates of over 500MB/s may be achievable. This interface is also completely backward-compatible with 32bit and/or 32MHz PCI hosts.

The minimum addressable functions include a high-speed Comport-like interface to each DSP, as well as any user-defined interfaces that may be built inside the Virtex FPGA. Access is also provided to a JTAG master attached to both DSPs on one chain, through a CPLD that also arbitrates configuration of the FPGA via the FPGA's SelectMAP port.

PMC PCI connectors are directly connected to the QuickLogic QL5064 bridge chip.

P11				P12			
Pin #	Signal name	Signal name	Pin #	Pin #	Signal name	Signal name	Pin #
1	TCK	-12V	2	1	+12V	TRSTN	2
3	GND	INTAN	4	3	TMS	TDO	4
5	INTBN	INTCN	6	5	TDI	GND	6
7	BUSMODE1N	+5V	8	7	GND	PCI-RSVD*	8
9	INTDN	PCI-RSVD*	10	9	PCI-RSVD*	PCI-RSVD*	10
11	GND	3.3Vaux	12	11	BUSMODE2N	+3.3V	12
13	CLK	GND	14	13	RSTN	BUSMODE3N	14
15	GND	GNTN	16	15	+3.3V	BUSMODE4N	16
17	REQN	+5V	18	17	PMEN	GND	18
19	VIO	AD31	20	19	AD30	AD29	20
21	AD28	AD27	22	21	GND	AD26	22
23	AD25	GND	24	23	AD24	+3.3V	24
25	GND	C/BE3N	26	25	IDSEL	AD23	26
27	AD22	AD21	28	27	+3.3V	AD20	28
29	AD19	+5V	30	29	AD18	GND	30
31	VIO	AD17	32	31	AD16	C/BE2N	32
33	FRAMEN	GND	34	33	GND	PMC-RSVD	34
35	GND	IRDYN	36	35	TRDYN	+3.3V	36
37	DEVSELN	+5V	38	37	GND	STOPN	38
39	GND	LOCKN	40	39	PERRN	GND	40
41	PCI-RSVD*	PCI-RSVD*	42	41	+3.3V	SERRN	42
43	PAR	GND	44	43	C/BE1N	GND	44
45	VIO	AD15	46	45	AD14	AD13	46
47	AD12	AD11	48	47	M66EN	AD10	48

49	AD9	+5V	50	49	AD8	+3.3V	50
51	GND	C/BE0N	52	51	AD7	PMC-RSVD	52
53	AD6	AD5	54	53	+3.3V	PMC-RSVD	54
55	AD4	GND	56	55	PMC-RSVD	GND	56
57	VIO	AD3	58	57	PMC-RSVD	PMC-RSVD	58
59	AD2	AD1	60	59	GND	PMC-RSVD	60
61	AD0	+5V	62	61	ACK64N	+3.3V	62
63	GND	REQ64N	64	63	GND	PMC-RSVD	64

**Table 1 - PMC P11/P12 Interface**

Pin #	P13		Pin #	Pin #	P14		Pin #
	Signal name	Signal name			Signal name	Signal name	
1	PCI-RSVD	GND	2	1	I/O	I/O	2
3	GND	C/BE7N	4	3	I/O	I/O	4
5	C/BE6N	C/BE5N	6	5	I/O	I/O	6
7	C/BE4N	GND	8	7	I/O	I/O	8
9	VIO	PAR64	10	9	I/O	I/O	10
11	AD63	AD62	12	11	I/O	I/O	12
13	AD61	GND	14	13	I/O	I/O	14
15	GND	AD60	16	15	I/O	I/O	16
17	AD59	AD58	18	17	I/O	I/O	18
19	AD57	GND	20	19	I/O	I/O	20
21	VIO	AD56	22	21	I/O	I/O	22
23	AD55	AD54	24	23	I/O	I/O	24
25	AD53	GND	26	25	I/O	I/O	26
27	GND	AD52	28	27	I/O	I/O	28
29	AD51	AD50	30	29	I/O	I/O	30
31	AD49	GND	32	31	I/O	I/O	32
33	GND	AD48	34	33	I/O	I/O	34
35	AD47	AD46	36	35	I/O	I/O	36
37	AD45	GND	38	37	I/O	I/O	38
39	VIO	AD44	40	39	I/O	I/O	40
41	AD43	AD42	42	41	I/O	I/O	42
43	AD41	GND	44	43	I/O	I/O	44
45	GND	AD40	46	45	I/O	I/O	46

47	AD39	AD38	48	47	I/O	I/O	48
49	AD37	GND	50	49	I/O	I/O	50
51	GND	AD36	52	51	I/O	I/O	52
53	AD35	AD34	54	53	I/O	I/O	54
55	AD33	GND	56	55	I/O	I/O	56
57	VIO	AD32	58	57	I/O	I/O	58
59	PCI-RSVD	PCI-RSVD	60	59	I/O	I/O	60
61	PCI-RSVD	GND	62	61	I/O	I/O	62
63	GND	PCI-RSVD	64	62	I/O	I/O	64

**Table 2 - PMC P13/P14 Interface**

### 3.2 SHB

The SHB signals have been named to match 2 16-bit SDB interfaces (or Hw SHB interface) pinout according to the [SUNDANCE SHB specification](#) Half Word configuration. The SMT417 will be equipped with 2 SHBs, both on side 2.

	Hw	QSH Pin number	QSH Pin number		Hw
Hw0	SHBxCLK0	1	2	Hw0	SHBxD0(0)
	SHBxD0(1)	3	4		SHBxD0(2)
	SHBxD0(3)	5	6		SHBxD0(4)
	SHBxD0(5)	7	8		SHBxD0(6)
	SHBxD0(7)	9	10		SHBxD0(8)
	SHBxD0(9)	11	12		SHBxD0(10)
	SHBxD0(11)	13	14		SHBxD0(12)
	SHBxD0(13)	15	16		SHBxD0(14)
	SHBxD0(15)	17	18		SHBxUSER0(16)
	SHBxUSER0(17)	19	20		SHBxUSER0(18)
	SHBxUSER0(19)	21	22		SHBxWEN1
	SHBxREQ1	23	24		SHBxACK1
Hw1	SHBxUSER1(23)	25	26	Hw1	SHBxUSER1(24)
	SHBxUSER1(25)	27	28		SHBxUSER1(26)
	SHBxUSER1(27)	29	30		SHBxUSER1(28)
	SHBxUSER1(29)	31	32		SHBxUSER1(30)
	SHBxUSER1(31)	33	34		SHBxUSER1(32)
	SHBxUSER1(33)	35	36		SHBxUSER1(34)
Hw1	SHBxCLK3	37	38	Hw1	SHBxD1(0)

SHBxD1(1)	39	40	SHBxD1(2)
SHBxD1(3)	41	42	SHBxD1(4)
SHBxD1(5)	43	44	SHBxD1(6)
SHBxD1(7)	45	46	SHBxD1(8)
SHBxD1(9)	47	48	SHBxD1(10)
SHBxD1(11)	49	50	SHBxD1(12)
SHBxD1(13)	51	52	SHBxD1(14)
SHBxD1(15)	53	54	SHBxUSER2(52)
SHBxUSER2(53)	55	56	SHBxUSER2(54)
SHBxUSER2(55)	57	58	SHBxWEN4
SHBxREQ4	59	60	SHBxACK4

**Table 3 - SHB Interface**

Typically right-angle SHB cables are used:

<http://www.sundance.com/edge/files/productpage.asp?strfilter=smt512-120>

### 3.3 JTAG headers

There are two distinct JTAG chains present on the SMT417:

1. The Xilinx JTAG chain is used to access the XC2VP FPGA + CoolRunnerII CPLD. The chain is brought out to a high-density debug header, and is used to update the CPLD firmware and to assist in board bring-up and debug of the FPGA firmware. The QL5064 JTAG interface is also on this chain, and is used for manufacturing test only. When programming the FPGA using an external JTAG controller, it is important to configure the tool to bypass both the CPLD and the QL5064.
2. The TI DSP JTAG chain connects the two DSPs to separate pins on the same high-density debug header. Additionally, this chain terminates into I/O pins of the CoolRunnerII CPLD. The CPLD can function as a Master (driver) of the chain, or as a Linker (transparent) according the debug mode desired. When functioning as a master, the CPLD is under the control of the host driver. This chain is used to control and debug DSP software, as well as to run the Sundance FLASH programming utility when managing the contents of the FLASH.

The XMC and PMC connectors also provide JTAG pins, but they are not used on the SMT417 and are simply tied TDI->TDO to maintain integrity of any chains that may be implemented on the carrier cards.

The SMT417 attempts to maximize compatibility with existing practices and software. The Xilinx and TI JTAG chains are kept separate, allowing both sets of devices to be connected to corresponding standard external controllers as needed.

Both JTAG-IN and JTAG-OUT for the DSP JTAG is provided to allow daisy-chaining of multiple DSP boards. Alternatively, users may target Code Composer Studio to the DSP boards directly through the PCI interface without connecting an external emulator.

Due to board real estate constraints, it was not possible to use standard headers for the external JTAG. The SMT417 implements a proprietary high-density debug header to allow the Xilinx and DSP JTAG headers to be available. A small companion PCB and short cable

interfaces to this high-density connector and provides standard Xilinx Parallel Cable IV or Platform Cable USB and TI XDS510 (IN and OUT) emulation headers.

### 3.3.1 JTAG Operation

The default state of the CPLD is to provide (transparent) operation to the DSP JTAG chains from the external connector. Through the programming of control registers accessible from the PCI host, the CPLD is capable of driving the DSP JTAG chain as a scan path controller. During stand-alone operation, the PCI is inactive, so the CPLD operates in its default state.

### 3.4 XMC

The XMC connector conforms to the type, position, and pinout specified in VITA 42.2 for XMC serial RapidIO. The pinout is shown below.

	A	B	C	D	E	F
1	S0_TD0+	S0_TD0-	3.3V	S0_TD1+	S0_TD1-	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	S0_TD2+	S0_TD2-	3.3V	S0_TD3+	S0_TD3-	VPWR
4	GND	GND	TCK	GND	GND	MRSTO#
5	S1_TD0+	S1_TD0-	3.3V	S1_TD1+	S1_TD1-	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	S1_TD2+	S1_TD2-	3.3V	S1_TD3+	S1_TD3-	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	UD	RFU	RFU	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	S0_RD0+	S0_RD0-	MBIST#	S0_RD1+	S0_RD1-	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	S0_RD2+	S0_RD2-	3.3V AUX	S0_RD3+	S0_RD3-	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	S1_RD0+	S1_RD0-	UD	S1_RD1+	S1_RD1-	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	S1_RD2+	S1_RD2-	RFU	S1_RD3+	S1_RD3-	RFU
18	GND	GND	UD	GND	GND	UD
19	RFU	RFU	UD	RFU	RFU	UD

Table 4 - XMC P15 pinout

### 3.5 FMS

Two FMS connectors are provided on side 1, and conform to the Sundance “Comm-ports” spec to implement one comm. port each. The connectors are single-row 14-pin type with 0.6mm pitch, and the pinout follows in table 5. To determine ownership of the port on

initialization, one of the two “detect” pins may be pulled-up to 3.3V while the other is grounded by the FPGA. If each side sees that both pins have been forced to ground then it may be understood that one port has initially been configured as an input and the other as an output. On the SMT417 this may be configured through the FPGA.

<b>Signal</b>	<b>Pin No.</b>	<b>Function</b>	<b>Type</b>
DET1	1	Direction-indicator	I/O
CxD(0-7)	2-9	Comm-Port DataBus	I/O
CREQx	10	Comm-Port Token Request	I/O
CACKx	11	Comm-Port Token Acknowledge	I/O
CSTRBx	12	Comm-Port Data Strobe	I/O
CRDYx	13	Comm-Port Ready	I/O
DET2	14	Direction-indicator	I/O

Table 5 - FMS connector pinout

## **4 Control Register Settings**

### **4.1 Control Packet Structure**

No special commands are defined.

### **4.2 Reading and Writing Registers**

Register formats and offsets for Comport, SDB/SHB, interrupt selection, etc. conform to Sundance firmware spec.

### **4.3 Memory Map**

Memory locations of standard Sundance functions conform to the Sundance firmware spec. The FPGA base address is TBD.

## 5 PCB Layout

The following figures show a preliminary concept of the top, bottom, and side view of the module. [Need to change QL5064 to full-matrix 484 package, restore original IRF DC/DC, add second SHB connector on side 2, change flash to a BGA, and add GRF1-J connector]

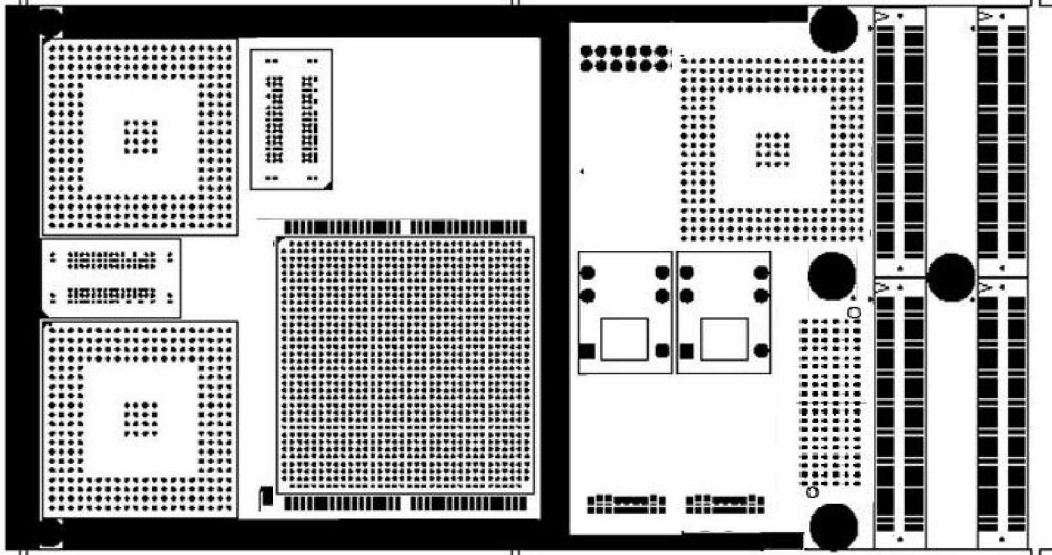


Figure 9 - Module Top View – Artist’s Conceptualization

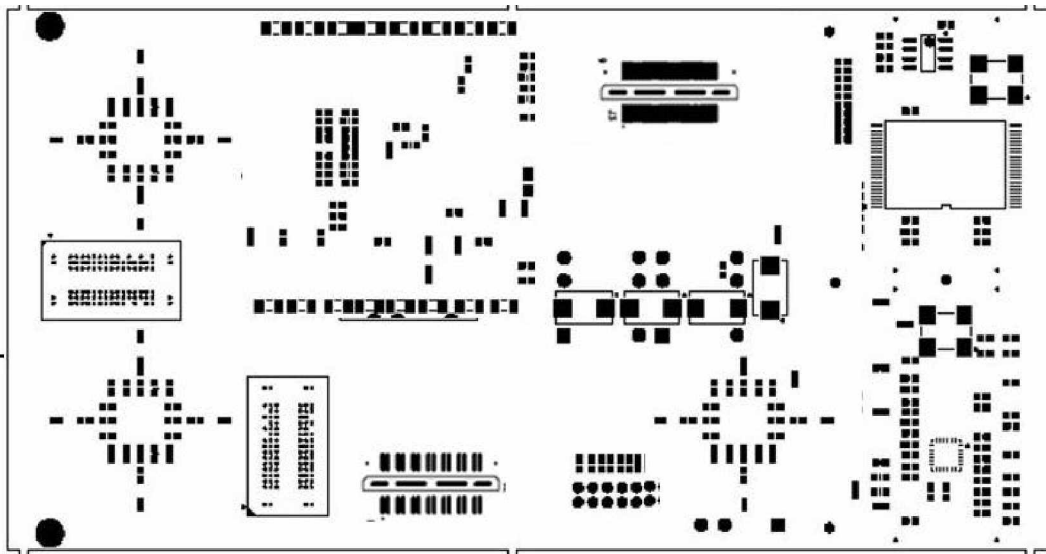


Figure 10 - Module Bottom View – Artist’s Conceptualization

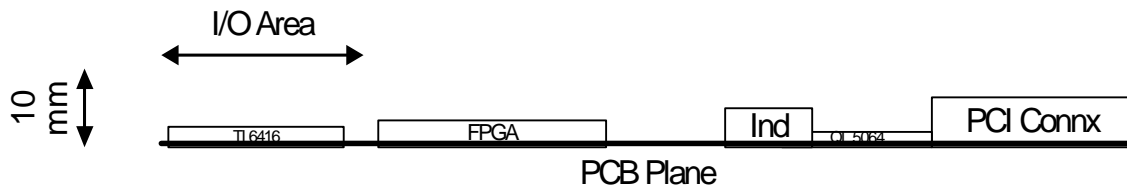


Figure 11 - Module Side View

## 6 Design Notes

### 6.1 FPGA Choice

The FPGA device will be a Xilinx Virtex II Pro of package type FF1152. In order to support the 637 total I/Os required by this design, the minimum device size will be a VP30. A VP50 is the minimum size that supports all 16 RSL links possible on this board. Table 6 shows the number and allocation of RSLs for different Virtex devices.

Virtex Device	XMC RSLs	RSL Connector	GRF-1
VP30	4	3	1
VP40	4	7	1
VP50	8	7	1

Table 6 – RSL Allocation vs. Virtex size

### 6.2 Power Requirements

Using the standard Comport/SDB/PCI interface FPGA firmware, and with arbitrary DSP programs running on both processors, the SMT417 must conform to PMC specification of no more than 7.5W power dissipation.

Voltage	Current(typ) Output	Current(max) Output	Current (supply)	Derived From	Supplies
3.3V				3.3V PCI (direct)	LVTTTL Digital I/O, FPGA Vcco, DSP Vio
2.5				3.3V PCI (linear LDO)	FPGA Vccaux
2.5				3.3V PCI (linear LDO)	RocketIO transceivers
1.5		10A		5V PCI (switching)	FPGA Vccint
1.2		5A		5V PCI (switching)	DSP Vcore

Table 7 - Power Budget Based on Supply

Note that in the table above, the maximum current represents the capacity of the power supply unit, not the actual consumption of the derived rail.

### 6.3 BOM

TBD