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Product Specification for SMT712

Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

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Revision History

Issue	Changes Made	Date	Initials
1	First Release	10/04/07	PhSR
2	DDR2 interface speed added, changed to hybrid PXI module	15/04/07	PhSR
3	Options (PXIe/PXI) clarified	19/04/07	PhSR
4	SHB connector added; Block Diagrams updated.	16/05/07	PhSR
5	PCB Layout updated	15/01/08	PhSR

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1 Introduction

The SMT712 is a PXI Express (opt. Hybrid) Peripheral Module (3U), which integrates two fast 12-bit DACs, 2 banks of DDR2 memory, a clock circuitry and a Virtex5 Xilinx FPGA, under the 3U format.

The PXIe specification integrates PCI Express signalling into the PXI standard for more backplane bandwidth. It also enhances PXI timing and synchronisation features by incorporating a 100MHz differential reference clock and triggers. The SMT712 can also integrate the standard 32-bit PXI signalling as an option.

Both DAC chips are identical and can update their output at up 2.3 Giga-samples per second each, with an 12-bit resolution. The manufacturer is Maxim and the part number is MAX19692. Digital-to-Analog converters are clocked by circuitry based on a PLL coupled with a VCO in order to generate a low-jitter fixed signal. The MAX19692 is capable to achieve SFDR figures close to 70dBs. Each DAC integrates settings depending on the type of frequency response required.

An on-board PLL+VCO chip ensure a stable fixed sampling frequency (maximum rate), in order for the board to be used as frequency synthesizer without the need of external clock signal. The PLL will be able to lock the VCO either on the on-board 100MHz reference or the 100MHz PXI express reference (or 10MHz PXI reference depending on option) or on an external reference signal. The sampling clock for the converters can be either coming from the PLL+VCO chip or from an external source. The reference clock selected is also output on a connector in order to pass it to an other module.

The Virtex5 FPGA is responsible for controlling all interfaces, including PXI (32-bit) and PXIe (8 lanes allocated – depending on PXIe chassis, 4 or 8 lanes would be used), as well as routing samples. The SMT712 is populated with an XC5VLX110T.

Two DDR2 memory banks are accessible by the FPGA in order to store data on the fly.

An SHB connector is available in order to transfer data/samples from an other Sundance module.

All analog connectors on the front panel are SMA.

Examples of application where the SMT712 can be involved in are wideband communication, radar, wireless modem, software radio or waveform generator systems.

2 Related Documents

2.1 Referenced Documents

1 – Maxim MAX19692:

http://www.maxim-ic.com/quick_view2.cfm/qv_pk/5172

2 – Analog Devices AD9516-2:

http://www.analog.com/en/prod/0,2877,AD9516-0,00.html

3 - Virtex5 FPGA:

http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/index.htm

4 - PXIe specifications:

http://www.pxisa.org/Spec/PXIEXPRESS_HW_SPEC_R1.PDF

5 – Micron 2Gigabit DDR2 chip MT47H128M16:

http://download.micron.com/pdf/datasheets/dram/ddr2/2gbddr2.pdf

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

PXIe : PXI Express.

SNR: Signal-to-Noise Ratio. It is expressed in dBs. It is defined as the ratio of a signal power to the noise power corrupting the signal.

SINAD: Signal-to-Noise Ratio plus Distorsion. Same as SNR but includes harmonics too (no DC component).

ENOB: Effective Number Of Bits. This is an alternative way of defining the Signal-to-Noise Ratio and Distorsion Ratio (or SINAD). This means that the ADC is equivalent to a perfect ADC of ENOB number of bits.

SFDR: Spurious-Free Dynamic Range. It indicates in dB the ratio between the powers of the converted main signal and the greatest undesired spur.

3.2 Definitions

4 Functional Description

4.1 General Block Diagram

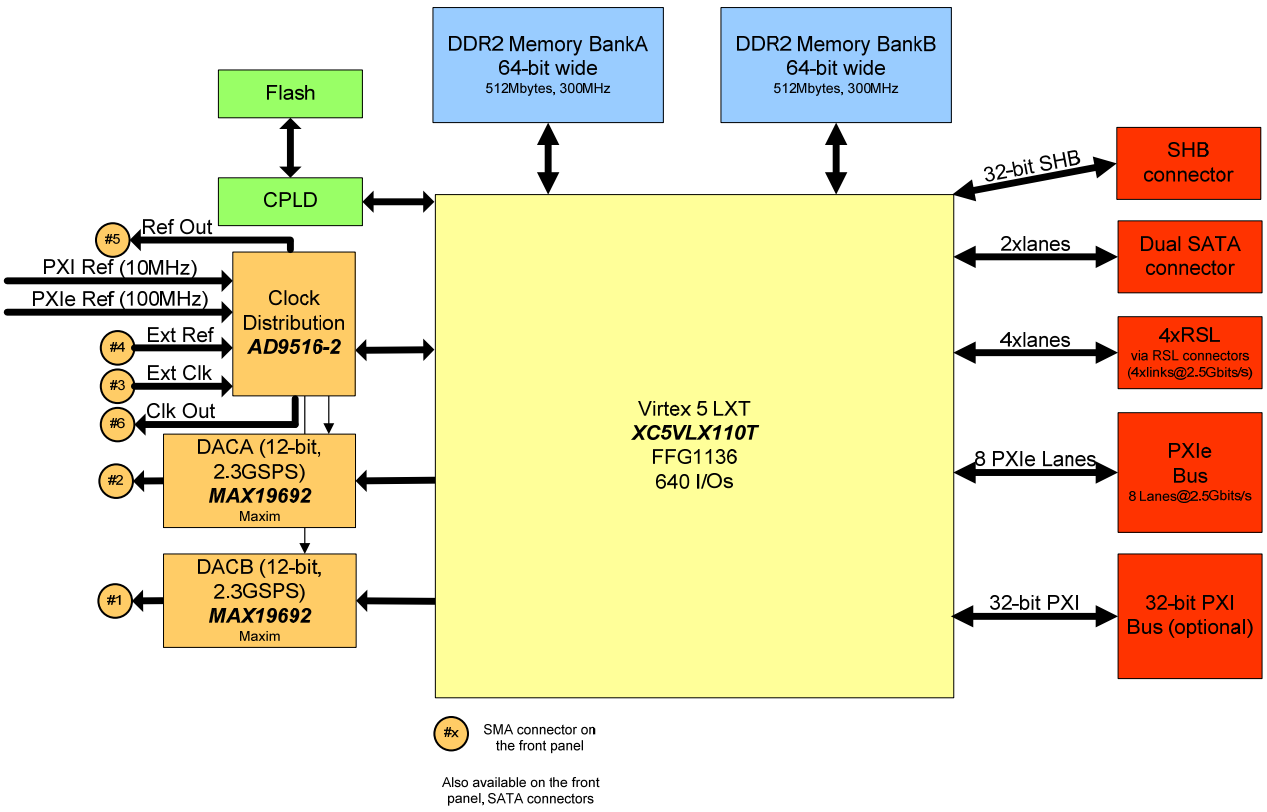


Figure 1 - SMT712 General Block Diagram.

The following block diagram clarifies both options. The first option (PXIe) can plugged into any PXI Express slot and the second (32-bit PXI) into any Hybrid PXI Express slot.

4.2 Block Diagram (Option PXIe)

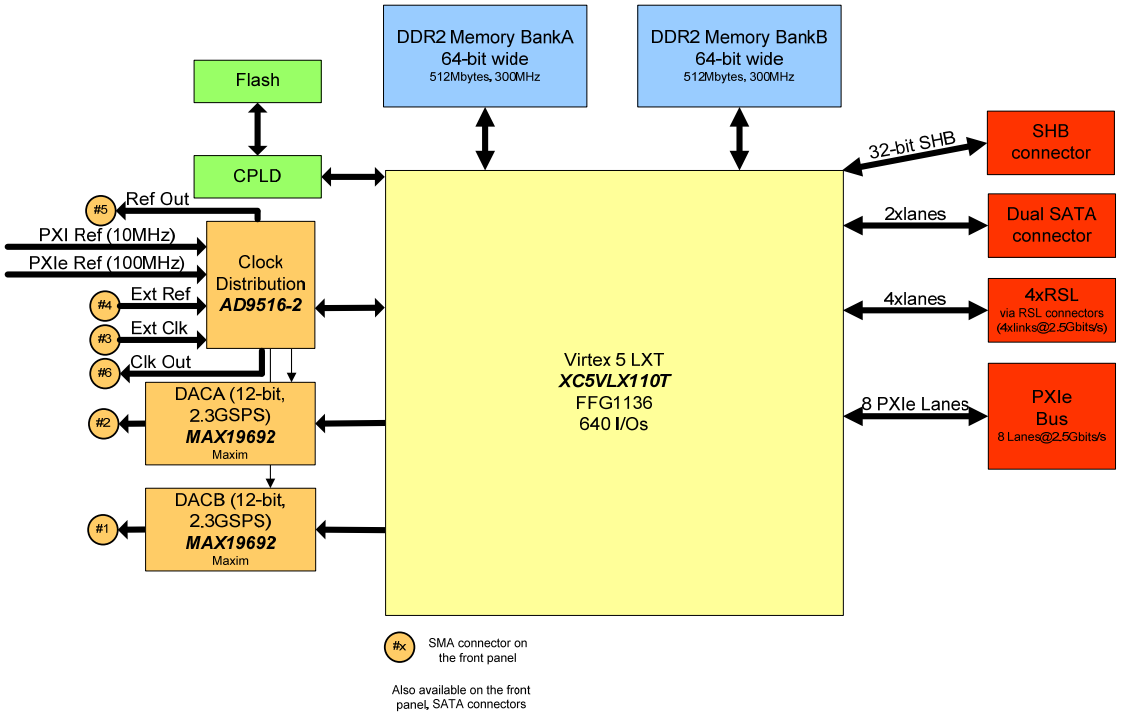


Figure 2 - SMT712 Block Diagram (option PXI Express)

4.3 Block Diagram (option 32-bit PXI)

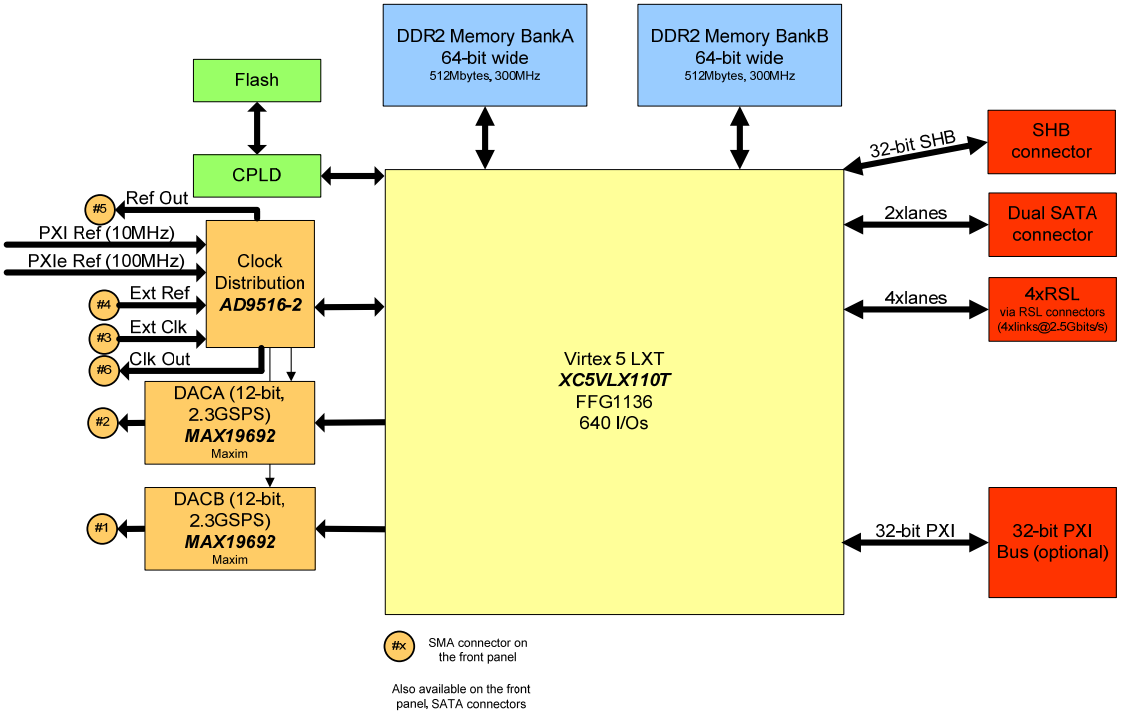


Figure 3 - SMT712 Block Diagram (32-bir PXI Option)

4.4 Module Description

4.4.1 DACs

The DACs are 12-bit parts from Maxim (MAX19692). On the SMT712, each DAC can achieve up to 2.3 GSPS, via a built-in 4:1 multiplexer.

Both DACs have a selectable frequency response mode, that can be NRZ (Non-Return-to-Zero – high dynamic range and output power in the first Nyquist zone), RZ (Return-to-Zero – this mode trades off SNR for improved gain flatness in the first, second and third Nyquist zones) or RF (Radio Frequency – high SNR and dynamic range in the second and third Nyquist Zones). For more information, please refer to the MAX19692 datasheet (Maxim).

The typical output power of the MAX19692 is -2.6 dBm (50-Ohm). These are the manufacturer figures.

4.4.2 FPGA

The FPGA fitted as standard on the SMT712 is part of the Virtex5 LXT family: XC5VLX110T. The package used if FFG1136.

The FPGA should be at least a -2 speed grade, or -3 for an even faster FPGA.

4.4.3 DDR2 Memory

Two banks of DDR2 memory are available on the SMT712, directly connected to the FPGA. Interfaces are part of the FPGA design. Each bank is 64-bit wide and 64-Meg deep, so each bank can store up to 320 Mega samples. Each memory bank is dedicated to one DAC.

Xilinx provides performances of a DDR2 interface as being: 200MHz for a -1 part, 267MHz for a -2 part and 333MHz for a -3 part.

The clock of the DDR2 interface should be at least 287.5MHz in order to achieve direct transfers from the memory to the DAC at the maximum sampling clock of the converter (2.3 GHz). This would be by the way of burst mode read operations and does not take into account any refresh cycles.

4.4.4 Clock circuitry

An on-board PLL+VCO chip ensure a stable fixed sampling frequency (maximum rate, i.e. 2300MHz), in order for the board to be used as synthesizer without the need of external clock signal. The PLL will be able to lock the VCO either on the on-board 10MHz PXI reference or the 100MHz PXI express reference or on an external reference signal. The sampling clock for the converters can be either coming from the PLL+VCO chip or from an external source. The chip used is a part from Analog Devices, the AD9516-2. The reference used for locking the VCO is output on a connector available on the front panel.

The selection Internal/External clock is made via a bit in the control register. The same applies to the selection of the reference clock.

4.4.5 PXI Express Bus

As standard, the SMT712 is a 3U PXI Express peripheral module, which means it comes with two PXI Express connectors: XP4 (PXI timing and synchronisation signals) and XP3 (x8 PCI Express and additional synchronisation signals). The SMT712 dedicates 8 lanes to the PXI Express bus, which gives an effective bandwidth per direction of 16Gb/s. It also implies core

and user clocks to be 250 MHz. Note that not all PXIe Express chassis can handle 8 lanes on peripheral modules.

The standard SMT712 can plug in any PXI Express Peripheral Slot or any PXI Express Hybrid Slot.

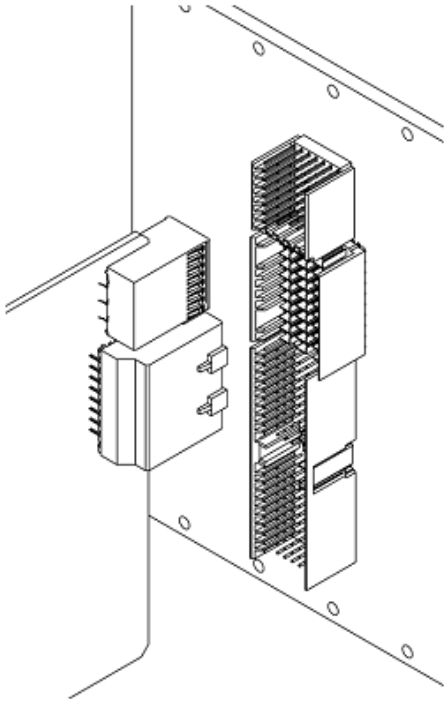


Figure 4 - Standard SMT712 - PXI Express Peripheral Module

Optionally, the module can be a 3U Hybrid Peripheral Slot Compatible PXI-1 Module, means it comes with two connectors: XP4 (PXI timing and synchronisation signals) and P1 (32-bit, 33MHz PCI Signals). This version of SMT712 can only plug in any PXI Express Hybrid Slot

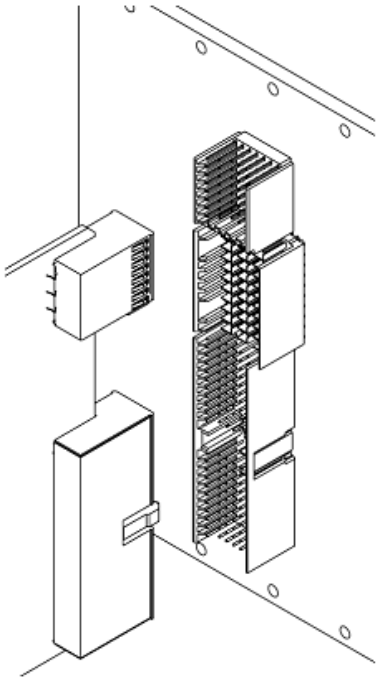


Figure 5 - SMT712 (opt.) - Hybrid Peripheral Slot Compatible PXI-1 Module

4.4.6 SHB connector

An SHB Connector is available from the FPGA. It maps 32 single-ended data lines and a set of control signals including a clock.

It can be used to transfer samples from an other Sundance module, for instance the SMT702.

4.4.7 DAC Synchronisation

The DAC chips used on the SMT712 have multiplexed input and may not start both a same time, which would have as an effect unsynchronised outputs. The FPGA implements a scheme that skips clock cycles in the initialisation state.

4.4.8 Power Supply (PXI Express Chassis)

The PXI Express specifications defines the maximum power consumption of 3U PXI Express peripheral modules as:

- 12-Volt rail: 2 Amps maximum (**24 watts**),
- 3.3-Volt rail: 3 Amps maximum (**10 watts**),
- 5-Volt rail (5Vaux): 1 Amp maximum.

An optional external power connector is available for external sources of the above rails. This should be carefully assessed as the fact of using an external power source may not meet the PXI Express specifications.

4.4.9 Power consumption

The FPGA and the DDR2 memory block will be powered from the 12-Volt PXI rail, whereas the ADCs and the clock circuitry will have their own supplies derived from the 3.3-Volt PXI rail.

Virtex5 FPGA (Worst case XC5VLX110T)(19.0 watts)

The XC5VLX110T is the part that will be fitted by default. Footprint compatible parts include XC5VSX50T and XC5VSX95T. The following power estimation has been done using a Xilinx spreadsheet, targeting the XC5VLX110T, with 98% of its LUTs and Flip-Flips used, an 8-lane PCI Express core, 128 DDR lines and the rest of the IOs set to standard LVTTL.

Note that in the case of the XC5VSX95T, using all 640 DSP slices would add an extra 2.7 watts to Vccint.

Vccint = 1.0 Volt / Estimated current = 11Amps [11 watts]

Vccaux = 2.5 Volts / Estimated current = 825mA [2.0 watts]

Vcco_18 = 1.8 Volts / Estimated current = 460mA [0.82 watt]

Vcco_33 = 3.3 Volts / Estimated current = 639mA [2.11 watt]

Vccmgt = 1 Volt / Estimated current = 294mA [0.294 watt]

Vccmgpll = 1.2 Volts / Estimated power = 198mA [0.238 watt]

Vtttx = 1.2 Volts / Estimated power = 390mA [0.468 watt]

Vttrx = 1.2 Volts / Estimated power = 72mA [0.086 watt]

The above figures stand as the worst case, where an XC5VLX110T is fitted with a chip full working at 500MHz. This will not be the case of the standard firmware provided with the board. In case the FPGA design gets to be modified, it is strongly recommended that an power consumption analysis is performed in order to check that 19 watt of total power is not exceeded.

Memory DDR2 – 2 banks of 1Gbytes (5 watts)

Vdd = Vddl = Vddq = 1.8V / Maximum current per chip = 355mA (8 chips – Micron MT47H128M16-37E - in total so 2.8 Amps). This does not include the termination resistors.

Vreference = Vddq/2 = 0.9V

Note that downsizing the memory capacity to 2 banks of 512Mbytes (MT47H64M16-37E) would reduce the current consumption per chip of 25mA (330mA) and would reduce power consumption down to 4.7 watts.

Note that downsizing the memory capacity to 2 banks of 256Mbytes (MT47H32M16-37E) would reduce the current consumption per chip of 15mA (340mA) and would reduce power consumption down to 4.9 watts.

DACs (2.5 Watts)

AVdd = 3.3 Volts / Maximum current per DAC = 117mA

AVclk = Vdd = 1.8 Volts / Maximum current per DAC = 500mA

Clock chip (1.2 Watts)

Vs = 3.3 Volts.

4.4.10 Power dissipation

The PXI Express chassis receiving the SMT712 module should provide enough forced air flow in order to dissipate the heat generated by the module. The air flow must be going against gravity or upwards, as specified in the PXI Specification.

It is also specified that a 3U PXI Express module should not dissipate more than 30 Watts of heat.

The following picture shows the direction of the forced air flow across a 3U PXI Express module:

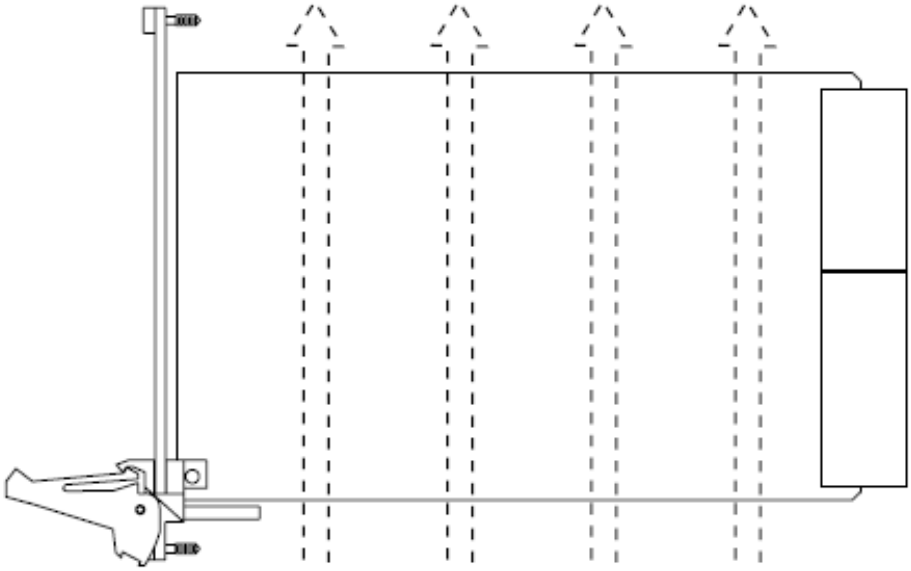


Figure 6 - Forced airflow for a 3U module.

A PXI Express rack has a capacity of dissipating 30 watts of heat per slot using forced air-cooling system via typically two 110-cfm fans with filter.

4.4.11 PXI Express Glyph

PXI Express System Module

PXI-1 Peripheral Module and Hybrid Slot Compatible PXI-1 Peripheral Module

PXI Express Peripheral Module

PXI Express System Timing Module

4.4.12 External Reset Button

Tbd.

4.4.13 JTAG

A connector is specifically dedicated for FPGA and CPLD detection and programming. Both the CPLD and the FPGA are part of the JTAG chain. A 14-position (2x7) connector (2mm) is available and shows TDI, TDO, TCK and TMS lines, as well as a Ground and a reference voltage, as shown below:

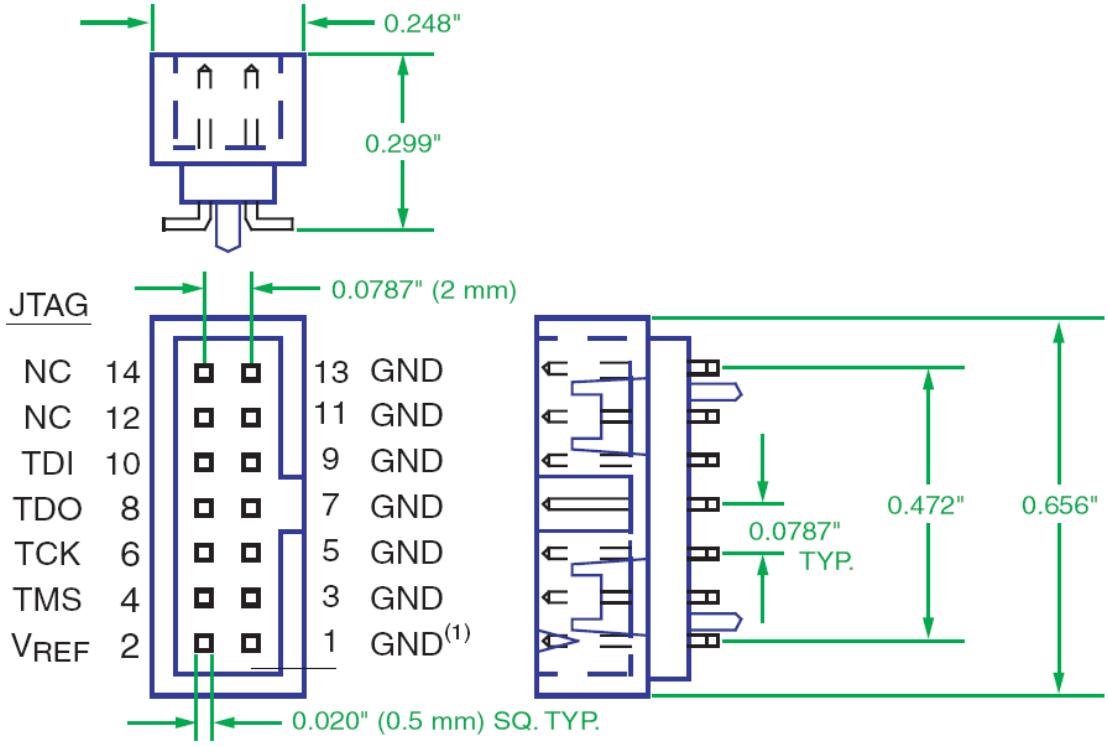


Figure 7 - JTAG Connector.

This connector has been chosen because it can connect easily to a Xilinx Parallel IV cable using the ribbon cable provided by Xilinx. The connector is a Molex part: Molex 87831-1428.

Figure 8 - Photo of a Xilinx Parallel IV cable and its ribbon cable for JTAG connection

4.4.14 PXI Express Hybrid Connectors

As being a PXI Express Hybrid Peripheral Module, the SMT712 is a 3U card with 2 PXI connectors, XP3, XP4 and P1. The following table shows their pinouts.

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND

XP4 / XJ4 Connector

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_CLK100+	PXIe_CLK100-	GND	PXIe_SYNC100+	PXIe_SYNC100-	GND	PXIe_DSTARC+	PXIe_DSTARC-	GND
2	PRSNT#	PWREN#	GND	PXIe_DSTARB+	PXIe_DSTARB-	GND	PXIe_DSTARA+	PXIe_DSTARA-	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

XP3 / XJ3 Connector

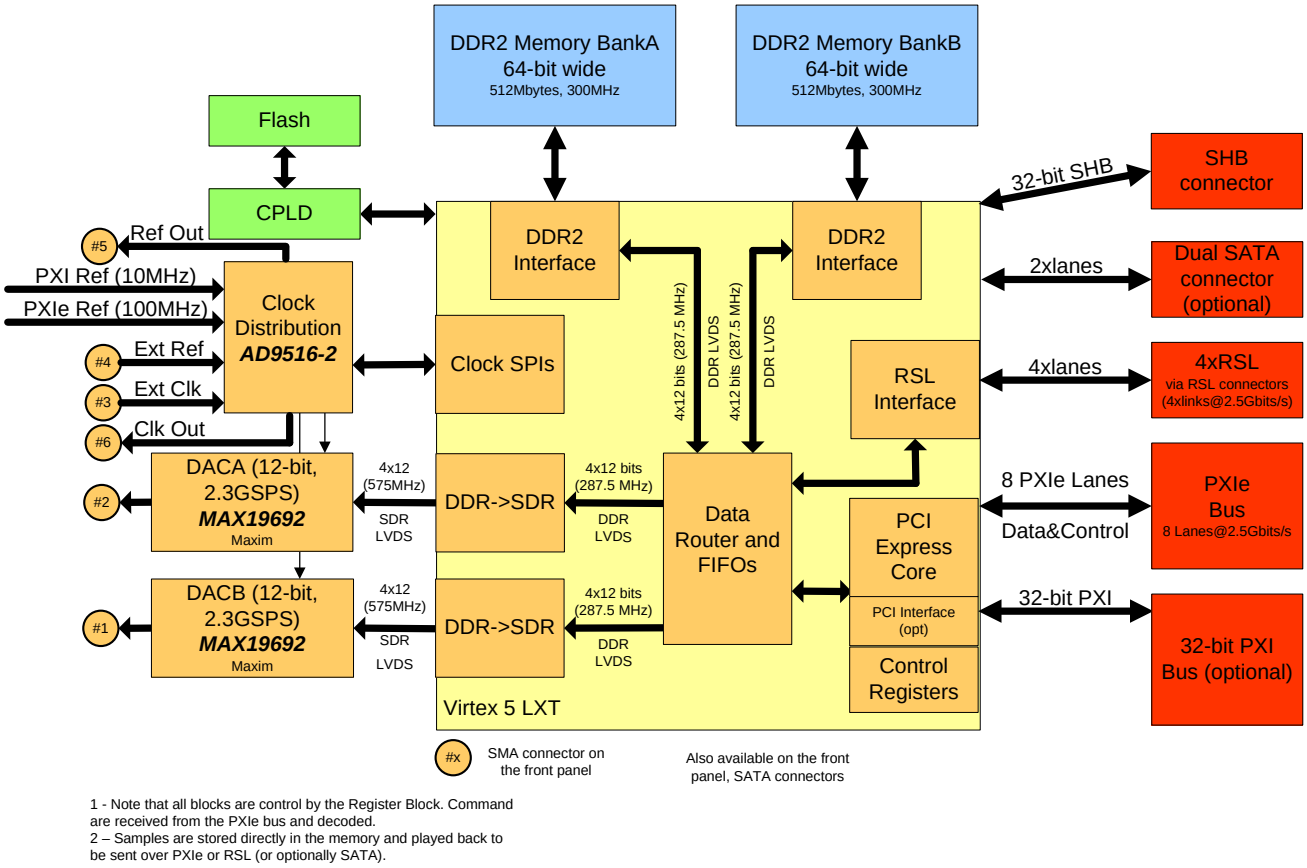
Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12–14				Key Area			
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

P1 / J1 Connector

The SMT712 implements up to eight 2.5-Gigabit PCI Express lanes, allowing a maximum data transfer of 2 gigabytes per second. It also implements optionally a 32-bit, 33-MHz PCI interface.

4.5 FPGA Design

The following block diagram shows how the default FPGA design is organised.



1 - Note that all blocks are control by the Register Block. Command are received from the PXIe bus and decoded.
2 – Samples are stored directly in the memory and played back to be sent over PXIe or RSL (or optionally SATA).

Figure 9 - Block Diagram - FPGA Design (standard Firmware).

4.5.1 Control Registers

The Control Registers control the complete functionality of the SMT712. They are setup via the PXIe bus (standard firmware provided). The settings of the DACs, triggers, clocks and the configuration of the RSL/PXI interfaces (optional SATA) and the internal FPGA data path settings can be configured.

The data passed on to the SMT712 over the PXIe bus must conform to a certain packet structure. Only valid packets will be accepted and only after acceptance of a packet will the appropriate settings be implemented. Each packet will start with a command (2 bits – 0x1 for a write operation – 0x2 for a read operation) information, followed by a register address (6 bits – see table), followed by a 24-bit data. This structure is illustrated in the following figure:

	Byte Content							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
3	Command 1	Command 0	Address 5	Address 4	Address 3	Address 2	Address 1	Address 0
2	Data 23	Data 22	Data 21	Data 20	Data 19	Data 18	Data 17	Data 16
1	Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

Figure 10 – Setup Packet Structure.

4.5.1.1 Memory Map

The write packets must contain the address where the data must be written to and the read packets must contain the address where the required data must be read. The following figure shows the memory map for the writable and readable Control Registers on the SMT712*:*

Address	Writable Registers	Readable Registers
0x00	Reset Register.	Reserved.
0x01	Test Register.	Test Register.
0x02	Update and Read-back command Register	Firmware Version and Status bits.
0x03		
0x11	DACs (MAX19692) Register 0x1.	Read-back (FPGA Register) DACs (MAX19692) Register 0x1.

Figure 11 – Register Memory Map.

4.5.1.2 Register Descriptions

Reset Register – 0x0.

	Reset Register – 0x0							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Reserved	Reserved	Reserved	Reserved		Reserved	Reserved	Reserved
Default	'0'	'0'	'0'	'0'		'0'	'0'	'0'

	Reset Register – 0x0	
Setting	**Bit 0**	**Description**
0	0	tbd
1	1	tbd
Setting	**Bit 1**	**Description**
0	0	tbd
1	1	tbd

4.5.1.2.1 DACs (MAX19692) Register 0x1 – Configuration Register.

	DACs (MAX19692) Register 0x1 – Configuration Register							
Byte	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Reserved	Reserved	Reserved	Cal (DacB)	Delay (DacB)	ClkDiv (DacB)	RZ (DacB)	RF (DacB)
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
0	Reserved	Reserved	Reserved	Cal (DacA)	Delay (DacA)	ClkDiv (DacA)	RZ (DacA)	RF (DacA)
Default	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

	DACs (MAX19692) Register 0x1 – Configuration Register	
Setting	**Bit 12**	**Description (Cal – DACB Output Resistance Calibration)**
0	0	Output Resistors are un-calibrated.
1	1	Output Resistors are calibrated.
Setting	**Bit 11**	**Description (Delay – DACB Data Clock Delay Mode Input)**
0	0	No Delay added.
1	1	Adds a delay of half of the input data period (2 DAC clock cycles).
Setting	**Bit 10**	**Description (ClkDiv – DACB Data Clock Divide Mode Input)**
0	0	Data Clock Rate is the input data rate divided by 4 (fclk/16).
1	1	Data Clock Rate is the input data rate divided by 2 (fclk/8).
Setting	**Bit 9**	**Description (RZ – DACB Return-to-Zero Mode select input)**
0	0	Normal DAC mode of operation (NRZ – high dynamic range and output power in the first Nyquist Zone).
1	1	Return-to-Zero mode of Operation (RZ – this mode trades-off SNR for improved gain flatness in the first, second and third Nyquist zones)
Setting	**Bit 5**	**Description (RF – DACA Radio Frequence Mode Input)**
0	0	NRZ or RZ DAC operation.
1	1	RF DAC operation (Provides higher SNR and dynamic performance in the second and third Nyquist Zone).
Setting	**Bit 4**	**Description (Cal – DACA Output Resistance Calibration)**
0	0	Output Resistors are un-calibrated.
1	1	Output Resistors are calibrated.
Setting	**Bit 3**	**Description (Delay – DACA Data Clock Delay Mode Input)**
0	0	No Delay added.
1	1	Adds a delay of half of the input data period (2 DAC clock cycles).
Setting	**Bit 2**	**Description (ClkDiv – DACA Data Clock Divide Mode Input)**
0	0	Data Clock Rate is the input data rate divided by 4 (fclk/16).
1	1	Data Clock Rate is the input data rate divided by 2 (fclk/8).
Setting	**Bit 1**	**Description (RZ – DACA Return-to-Zero Mode select input)**
0	0	Normal DAC mode of operation (NRZ – high dynamic range and output power in the first Nyquist Zone).
1	1	Return-to-Zero mode of Operation (RZ – this mode trades-off SNR for improved gain flatness in the first, second and third Nyquist zones)
Setting	**Bit 0**	**Description (RF – DACA Radio Frequence Mode Input)**
0	0	NRZ or RZ DAC operation.
1	1	RF DAC operation (Provides higher SNR and dynamic performance in the second and third

		Nyquist Zone).

4.5.2 External Signal characteristics

The main characteristics of all external signals of the SMT712 are gathered into the following table.

Analogue Outputs (TBC)	
Output voltage range	**AC coupled option**. TBC - AC coupled via RF transformer. **DC coupled option**. TBC.
DACs Maximum Output Power	-2.6dBm (50R)
Impedance	50Ω.
Output Bandwidth	Minimum 1500MHz depending on the frequency response mode set.
External Reference Input (TBC)	
Input Voltage Level	0.5 – 3.3 Volts peak-to-peak (AC-coupled)
Input Impedance	50-Ohm (Termination implemented at the connector)
Frequency Range	0 – 100 MHz.
External Reference Output (TBC)	
Output Voltage Level	1.6 Volts peak-to-peak (AC-coupled)
Output Impedance	50-Ohm (Termination implemented at the connector)
External Sampling Clock Input (TBC)	
Input Voltage Level	0.5 – 3.3 Volts peak-to-peak (AC-coupled)
Input Format	Single-ended or differential on option (3.3V LVPECL).
Frequency range	500-2300 MHz
External Trigger Inputs (TBC)	
Input Voltage Level	1.5-3.3 Volts peak-to-peak.
Format	DC-coupled and Single-ended (Termination implemented at the connector). Differential on option (3.3 V PECL).
Impedance	50-Ohm.
Frequency range	62.5 MHz maximum
***DACs* Input Format**	
Input Data Width	12-Bits
Data Format	Offset Binary
SFDR	58-75dBs maximum (manufacturer)
Wideband Noise-spectral Density	Up to -162dBm/Hz maximum (manufacturer)
Minimum Sampling Clock	10 MHz
Maximum Sampling Frequency	2300 MHz

Figure 12 – Main Characteristics.

4.6 Interface Description

4.6.1 Mechanical Interface

4.6.2 Electrical Interface

5 Verification Procedures

5.1 CPLD and FPGA detection

This, using the JTAG connector and a Xilinx parallel cable IV.

5.2 DAC connections

Specific pattern.

5.3 DAC Performance

Sinewave patterns. Performances measured with a spectrum analyser (Anritsu – MS2717A)

6 Review Procedures

7 Validation Procedures

8 Timing Diagrams

9 Circuit Description / Diagrams

10 Board Layout

10.1 Top View

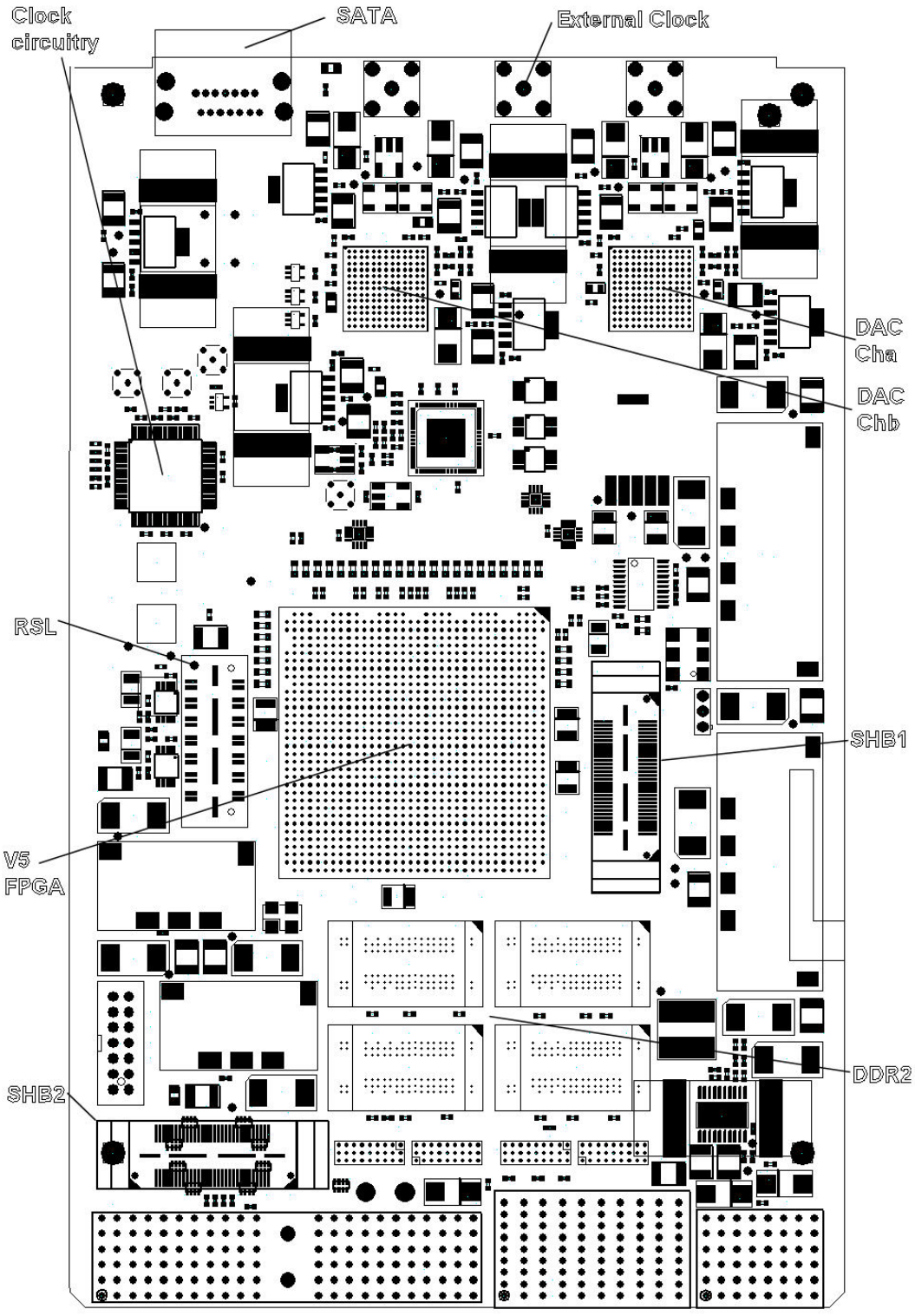


Figure 13 - Board Layout (Top View)

10.2 Bottom View.

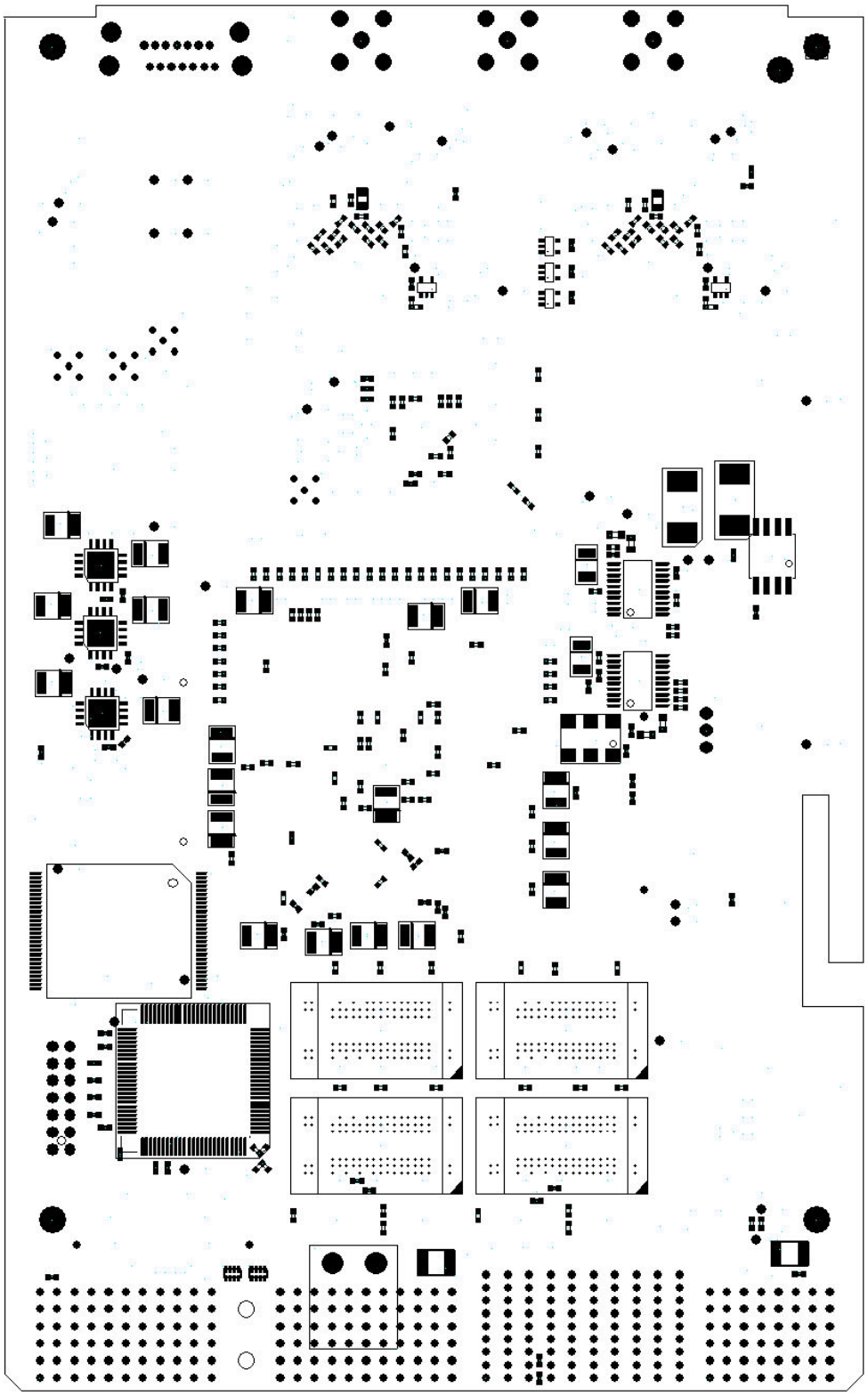


Figure 14 - Board Layout (Bottom View).

11 Pinout

12 Support Packages

13 Physical Properties

Dimensions	PXI Express 3U	
Weight		
Supply Voltages		
Supply Current	+12V	Est. 2 amps
	+5V	N/A
	+3.3V	Est. 3 amps
	-5V	N/A
	-12V	N/A
MTBF		

14 Safety

This module presents no hazard to the user when in normal use.

15 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.