SUNDANCE

SMT8096

User Manual

Revision History

Date	Comments	Engineer	Version
13/10/2005	Original Document	PSR	1.0
09/12/2005	Partslist updated	PSR	1.1
22/12/2005	3L Application instructions added	PSR	1.2

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Contacting Sundance.

You can contact Sundance for additional information by sending email to support@sundance.com.

Notes.

- SHB stands for **S**undance **H**igh-speed **B**us.
- Comport denotes an 8-bit communication port following the TI C4x standards.
- *SMT8096* is a PCI system to be plugged in a PC. The only software requirement is to have 3L Diamond server installed. Application files can be found in the *SMT6600* package provided when purchasing an *SMT8096* system.

Precautions

In order to guarantee that Sundance's boards function correctly and to protect the module from damage, the following precautions should be taken:

- They are static sensitive products and should be handled accordingly. Always place the modules in a static protective bag during storage and transition.
- When operated in a closed environment make sure that the heat generated by the system is extracted e.g. a fan extracting heat or blowing cool air. Sundance recommends and uses PAPST 12-Volt fans (Series 8300) producing an air flow of 54 cubic meters per hour (equivalent to 31.8 CFM). Fans are placed so they blow across the PCI bus.

Outline description.

The *SMT8096* is PCI based and stands as an evaluation/development platform as part of a Multi-carrier / Multi-standard cellular system, MIMO infrastructure, Test Equipment, etc…

The *SMT8096* is a PCI system based on 3 main modules: TI DSP C6416T module (*SMT395-VP30-6*) combined with a dual high-speed ADC/DAC mezzanine SLB module (*SMT350*) and an SLB base module (*SMT368*), all plugged on a PCI carrier board (*SMT310Q*).

SMT395-VP30-6 characteristics:

⇒ 1GHz TMS320C6416T fixed-point DSP,

⇒ 8000 MIPS peak performance,

⇒ Xilinx Virtex-II Pro VP30-6 FF896 package,

⇒ Six 20MB/s communication ports (Comports),

⇒ 256MBytes of SDRAM (133MHz),

⇒ 8MByte Flash ROM for boot code and FPGA programming,

⇒ Global expansion connector,

⇒ High bandwidth data I/O via 2 Sundance High-speed Buses (SHB),

⇒ JTAG Diagnostics port.

SMT350 characteristics:

⇒ Two 14-bit ADCs (TI – ADS5500) sampling at up to 105MHz,

⇒ Dual 16-bit DAC (DAC5686) sampling at up to 500MHz (interpolation),

⇒ One **S**undance **L**VDS **B**us (SLB – 60-way Samtec SQH),

⇒ Low-jitter on-board system clock based around the combination of a VCXO and the TI - CDCM7005,

⇒ 50-Ohm terminated analogue inputs and outputs, external triggers and clocks via MMCX (Huber and Suhner) connectors.

SMT368 characteristics:

⇒ Virtex 4-SX (XCV4SX35 FPGA) in an FF668 package,

⇒ Two banks of 8Mbytes of ZBTRAM,

⇒ Four **S**undance **H**igh-speed **B**us (SHB – 160 I/Os),

⇒ Two Comport,

⇒ One **S**undance **L**VDS **B**us (SLB – 60-way Samtec SQH).

The *SMT8096* development platform supports the design and development of a wide range of radio and waveform applications. It can be used for prototyping communication systems, third and fourth generation wireless architecture as well as MIMO structures.

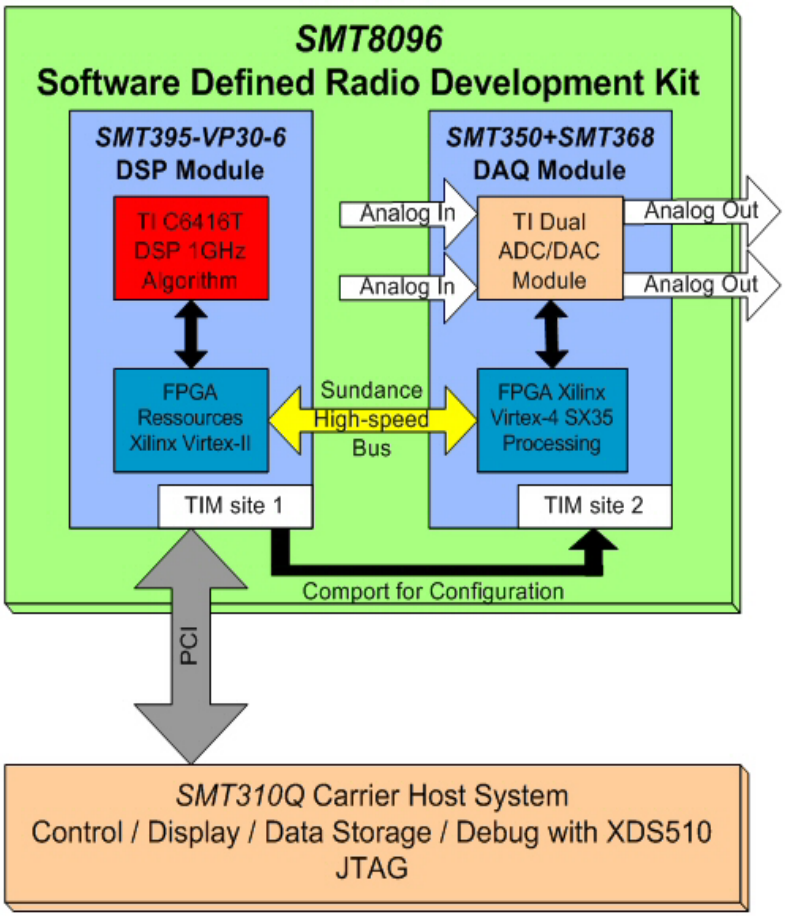
This document is an installation guide for the *SMT8096* demonstration system.

Documentation and source files are installed by the way of the *SMT6600* package, which is the Sundance DAQ package. ***Source and application files provided are to be run by the way of 3L Diamond Server only***.

The *SMT8096* application gets the DSP on the *SMT395-VP30* to configure the DAC of the *SMT350* to generate a continuous sine wave via a first SHB connection. DAC outputs are loop onto the ADCs inputs. The DSP grabs data from both channels and stores them into a file, which can be read by a Matlab application for data displaying and FFT processing. Sampling clocks (122MHz for the ADCs and the DAC) are generated by on-board VCXO locked onto an on-board reference clock.

Architecture.

The following diagram shows the architecture of the *SMT8096* system:



What is provided in the *SMT8096* system?

When purchasing an *SMT8096* system, you will get the following (unless stated on order/invoice):

- SMT395-VP30-6,
- SMT310Q,
- *SMT368* (SMT368),
- *SMT350* (SMT350),
- *One 200mm FMS cable (SMT500-FMS20),*
- SMT596-H (Dual SHB PCB),
- SMT595 (MMCX PCB for Analog feed-back).

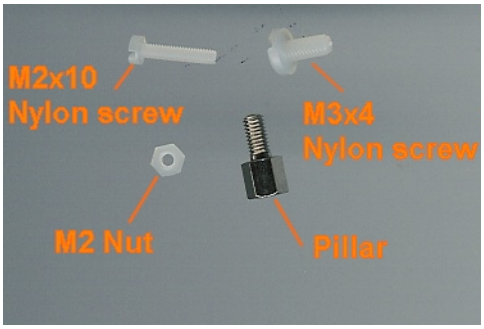
Hardware installation.

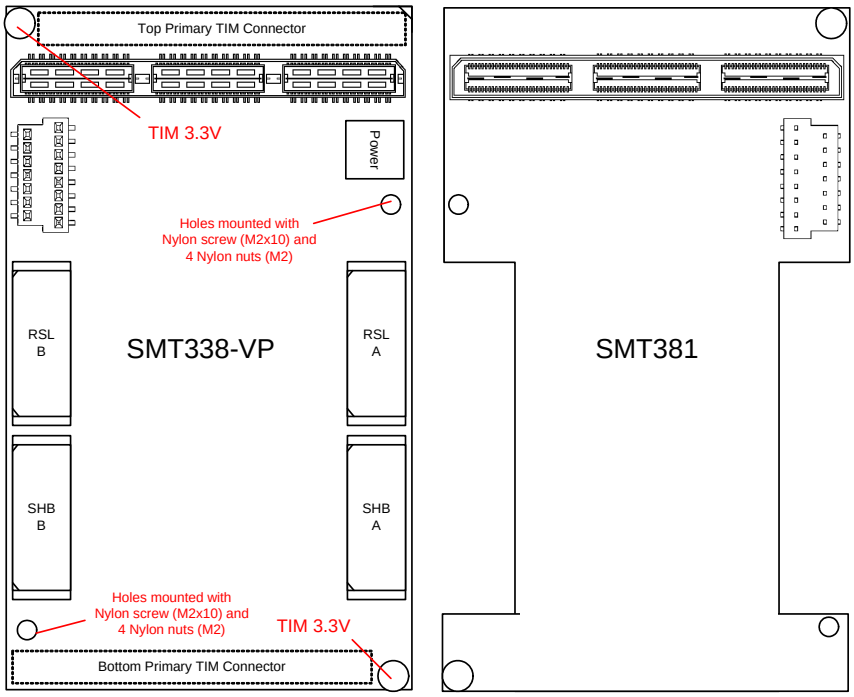
Here are the steps to follow to install the *SMT8096* system.

1 – Place the *SMT395-VP30-6* on TIM site 1 of the carrier board (*SMT310Q*).

2 – Place the *SMT368* on TIM site 2 of the carrier board (*SMT310Q*).

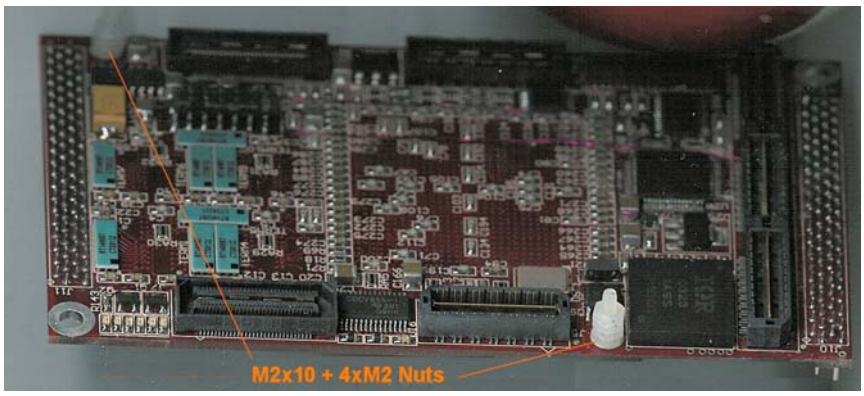
3 – Place the *SMT350* on top of the *SMT368* as follow. Please note that the example shows how to plug an *SMT381* on top of an *SMT338-VP*, similar to plug respectively an *SMT350* on top of an *SMT368*.



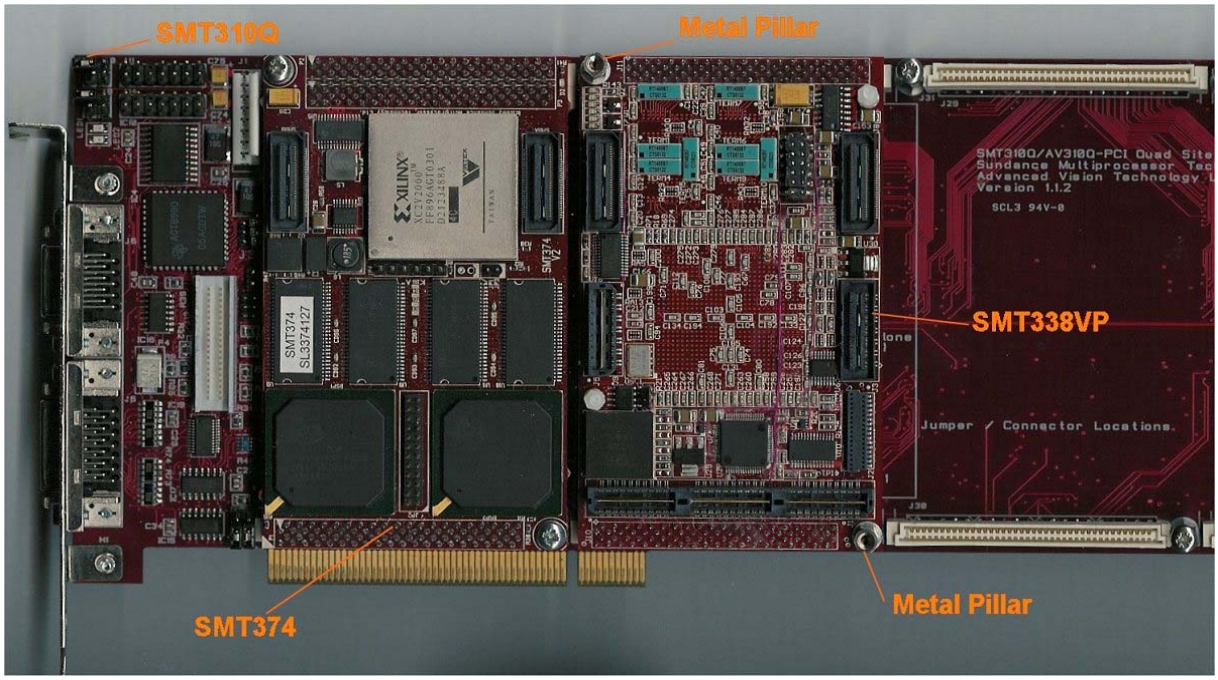


a – First, fit two Nylon screws (M2x10), pointing out (the head of the screws on bottom side).

b – Then fit four M2 nuts on each screw.



c – Place the *SMT338-VP* on the second site (*SMT395-VP* already on first site) on the *SMT310Q* and fit two metal pillars (3.3 Volts).



d – Place the *SMT381* on top of the *SMT338-VP*. Make sure that both modules fit firmly.

e – Fit two M2 nuts on the Nylon screws and two M3x4 screws in the 3.3V pillars.

4 – Connect CommPort 0 of the *SMT395* to CommPort 3 of the *SMT368* (T1C0 to T2C3) via an FMS cable at the back of the *SMT310Q*.

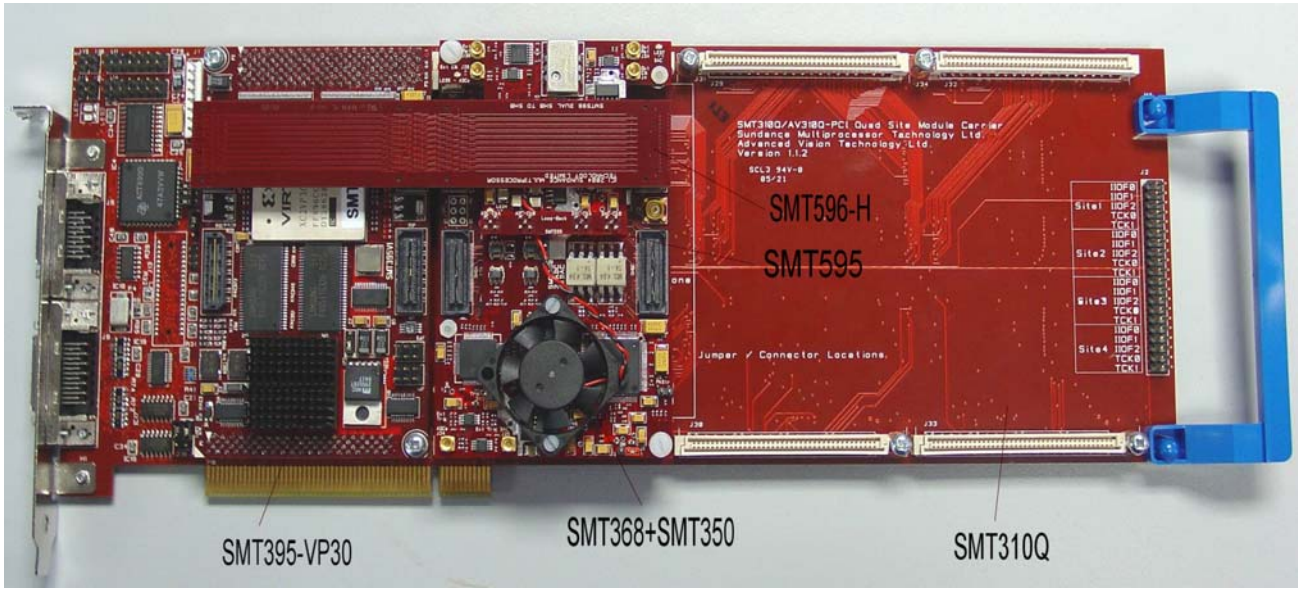
5 – Connect SHBA on the *SMT395* to SHBA on the *SMT368* via the *SMT516*.

6 – Connect SHBB on the *SMT395* to SHBB on the *SMT368* via a standard SHB cable.

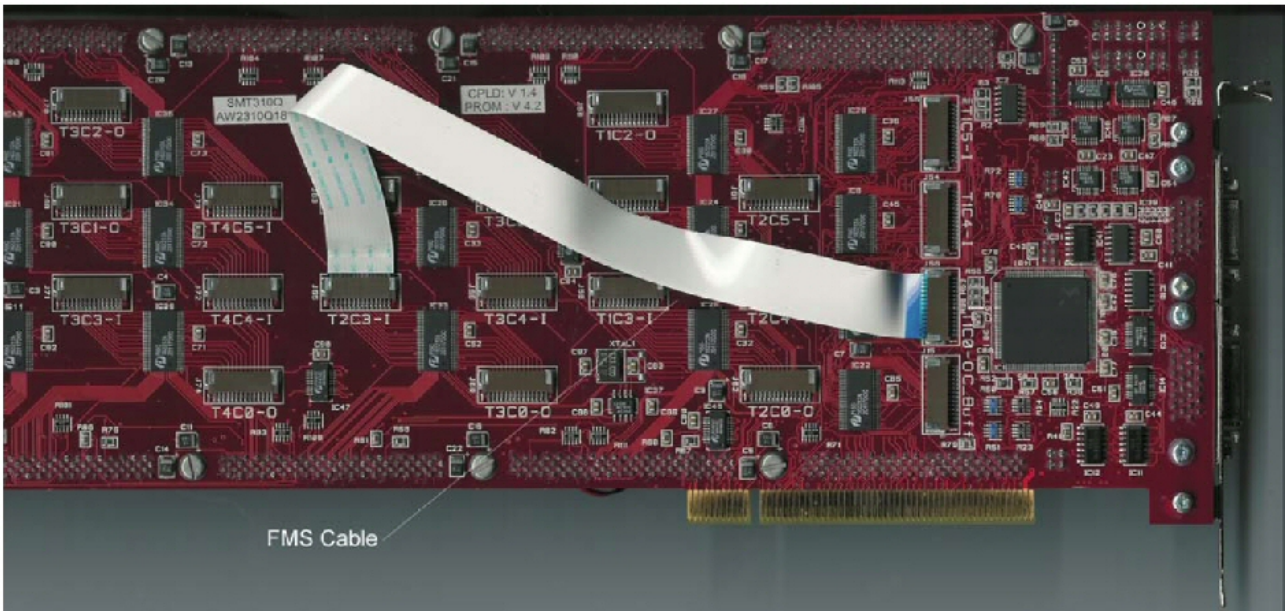
7 – Connect J3 to J11 and J32 to J31 on the *SMT350* using the *SMT595*.

8 – Place the carrier board in the host system.

The following picture shows how connections are made at the top of the system:



The following picture shows the CommPort connection at the back of the SMT310Q. Note that the FMS are ‘twisted’, i.e. one end should be blue and the other should show silver pins.



Hardware Connections.

Below are listed the connection to be checked before plugging the system in the PC:

FMS connections:

- T1C0 to T2C3,

SHB connections via SMT596-H:

- *SMT395-VP30* (SHBA) to *SMT368* (SHBB),
- *SMT395-VP30* (SHBB) to *SMT368* (SHBA).

Analog connections via SMT595:

- J3 and J11 to J32 and J31.

3L Application.

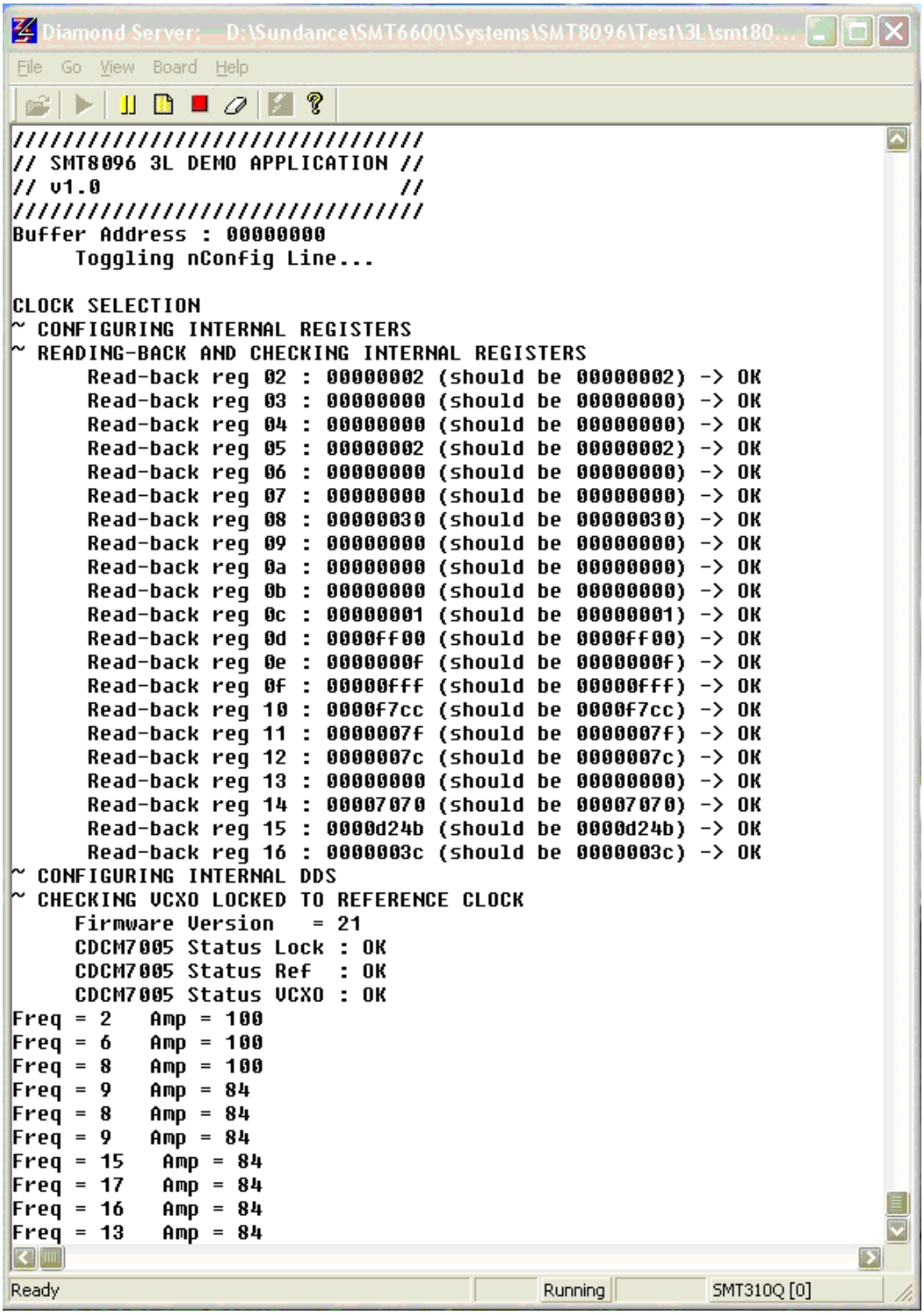
The application provided configured the FPGA (*SMT368*) and sets up registers so the board works as a DDS. DAC outputs are loopback onto the ADCs inputs. Samples are then captured, processed with in FFT (1K) and sent to the host for display.

With each DAQ module purchased, comes the SMT6600 package. Once installed you will find in ***\Program Files\Sundance\SMT6600\Systems\SMT8096\3L***, a 3L application called ***SMT8096.app***. This implies of course that *3L Diamond* has been installed beforehand.

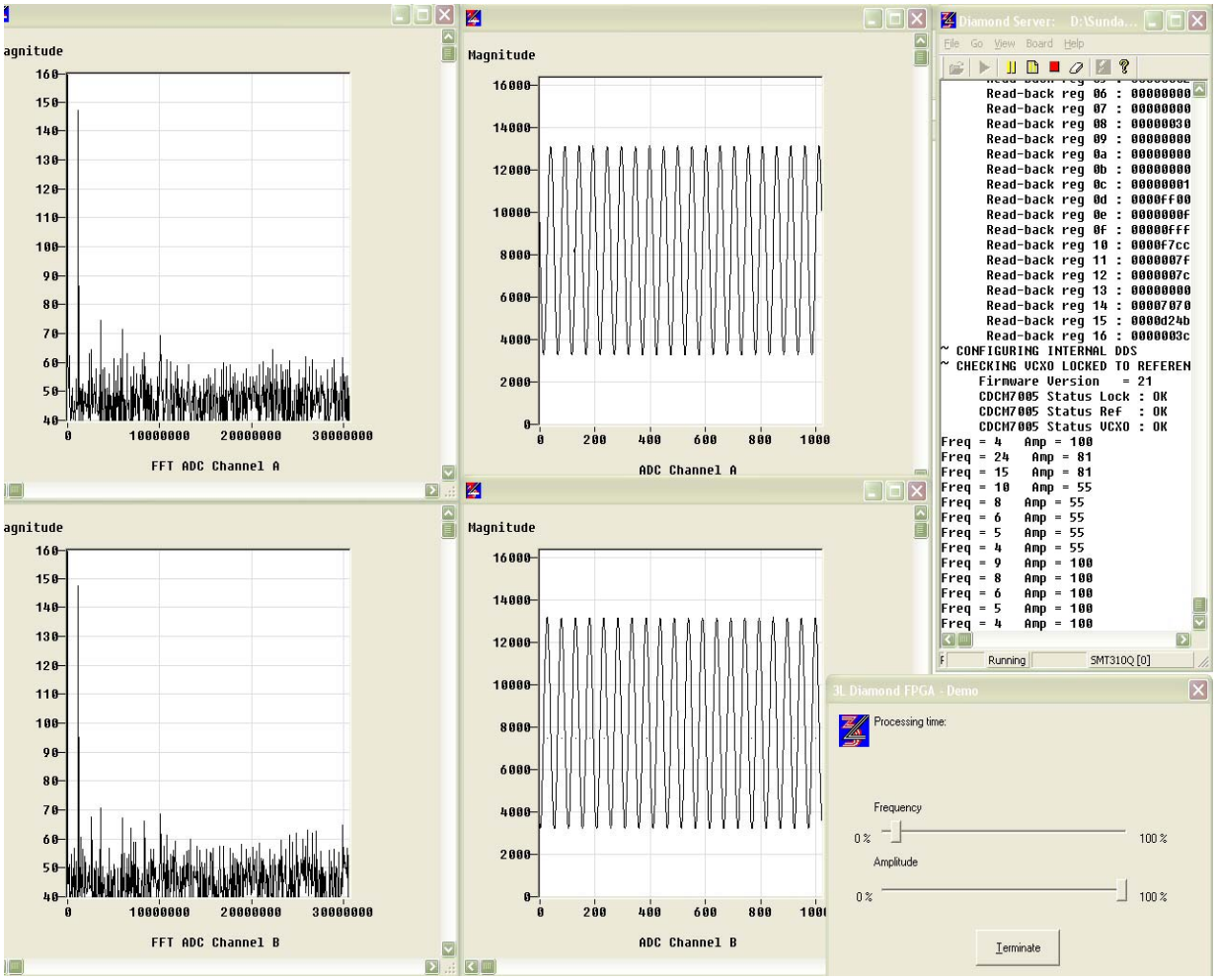
Also in the same directory, you will find a dll (*clu3L_300.dll*) that you will have to copy into the ***Windows\System32*** directory.

Once done, you can launch *SMT8096.app* (double-click on the file). This will open 5 windows. The main one will report the different steps of the application. Registers are written and read-back to check the good functioning of the system, same applies for the CDCM7005 status bit. All should be ‘OK’.

When the frequency on the scroll bar is changed, position of the scroll bar for frequency and amplitude are reported in the main window.



Four other windows will open to display raw data for each ADC channel as well as the matching FFT. A scroll bar is also available to change the frequency generated by the DDS (and output by the DAC), as well as the amplitude. Note that ‘left-clicking’ in one of the graphics windows will freeze the display and make cursors appear for measurement purpose (X and Y).


agnitude
FFT ADC Channel A
Magnitude
ADC Channel A
Diamond Server: D:\Sunda...
File Go View Board Help
Read-back reg 06 : 00000000
Read-back reg 07 : 00000000
Read-back reg 08 : 00000030
Read-back reg 09 : 00000000
Read-back reg 0a : 00000000
Read-back reg 0b : 00000000
Read-back reg 0c : 00000001
Read-back reg 0d : 0000ff00
Read-back reg 0e : 0000000f
Read-back reg 0f : 00000fff
Read-back reg 10 : 0000f7cc
Read-back reg 11 : 0000007f
Read-back reg 12 : 0000007c
Read-back reg 13 : 00000000
Read-back reg 14 : 00007070
Read-back reg 15 : 0000d24b
Read-back reg 16 : 0000003c
~ CONFIGURING INTERNAL DDS
~ CHECKING VCXO LOCKED TO REFEREN
Firmware Version = 21
CDCM7005 Status Lock : OK
CDCM7005 Status Ref : OK
CDCM7005 Status VCXO : OK
Freq = 4 Amp = 100
Freq = 24 Amp = 81
Freq = 15 Amp = 81
Freq = 10 Amp = 55
Freq = 8 Amp = 55
Freq = 6 Amp = 55
Freq = 5 Amp = 55
Freq = 4 Amp = 55
Freq = 9 Amp = 100
Freq = 8 Amp = 100
Freq = 6 Amp = 100
Freq = 5 Amp = 100
Freq = 4 Amp = 100
Running
SMT310Q [0]
agnitude
FFT ADC Channel B
Magnitude
ADC Channel B
3L Diamond FPGA - Demo
Processing time:
Frequency
0 %
100 %
Amplitude
0 %
100 %
Terminate