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Unit / Module Number:	SMT903
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Product Specification for SMT903

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Revision History

Issue	Changes Made	Date	Initials
1	Original Document released	25/06/07	PhSR
2	Updates	02/07/07	PhSR
3	More Updates	02/09/08	DH
4	Replace Atmel RFIC with Maxim	06/11/08	DH
5	Post PCB layout updates	07/02/08	DH

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1 Introduction

The *SMT903* is a single width TIM that plugs onto an SLB base module such as the SMT368 (Virtex-4 FPGA) or the SMT351T (Virtex-5 LXT/SXT FPGA) or other SLB base module. It incorporates 2 Maxim Wimax (IEEE802.16-2004) Transceivers that operate at 2.3 – 2.7 GHz (MAX2837). The transceivers integrate a power amplifier driver, receive/transmit mixer, low-noise amplifier, receive/transmit filters, synthesizer, VCO, receive gain control, and transmit power control.

Each RF transceivers is coupled with a Mixed-Signal Front End chip from Analog Devices (AD9863) that integrates two 12-bit ADCs (80MSPS) as well as two 12-bit DACs (200MSPS using interpolation), to provide analog and digital conversions and ensure a sufficient level of precision for Wimax applications.

Clocking circuits enable the board to run the transceivers and the converters from internal 40MHz VC-TCXO, an external input, a PLL or the FPGA.

The Xilinx FPGA on the base module is responsible for handling data or control commands to/from **C**omports (TIM-40 standard), **S**undance **H**igh-speed **B**us (SHB) or **R**ocket-IO **S**erial **L**ink (RSL). These interfaces are compatible with a wide range of Sundance's modules. Typically, the FPGA can implement control and baseband processing. Converter configuration, sampling rates and transceiver modes are set via internal control registers stored inside the FPGA and accessible via Comport.

The purpose of the SMT903 is to provide customers with a hardware module in order to develop or implement a Wimax core and/or fixed applications. All necessary control interfaces are provided with the board. Note that no Wimax core is provided with the board.

2 Related Documents

MAX2837 Datasheet – Maxim:

http://www.maxim-ic.com/quick_view2.cfm/qv_pk/5452

AD9863 Datasheet – Analog Devices:

http://www.analog.com/en/rfif-components/rxtx-subsystems/ad9863/products/product.html

Rocket-IO **S**erial **L**ink (*RSL*) specifications – Sundance.

http://www.sundance.com/docs/Specification_RSL.pdf

Sundance **H**igh-speed **B**us (*SHB*) specifications – Sundance.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification.pdf

Sundance **L**VDS **B**us (SLB) specifications – Sundance.

http://www.sundance.com/docs/SLB%20-%20Technical%20Specifications.pdf

TIM specifications.

ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf

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SMT368

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3 Acronyms, Abbreviations and Definitions

Wimax is defined as **W**orldwide **I**nteroperability for **M**icrowave **Acc**ess. It defines a wireless digital communication system.

MxFE is abbreviation for **Mi**x**F**ed-Signal **F**ront **E**nd. MxFE is an integrated component that contains two ADC and two DAC. MxFE converts digital baseband signals to analog baseband signals in the transmission path and analog baseband signals to digital baseband signals in the reception path.

TX is abbreviation for transmitter or transmission

RX is abbreviation for receiver or reception

TRX is abbreviation for transceiver, i.e. a component or circuit that handle both the transmission and the reception paths.

4 Functional Description

4.1 Block Diagram

The following figure shows the block diagram of the SMT903 SLB Mezzanine Module: **(TBD)**

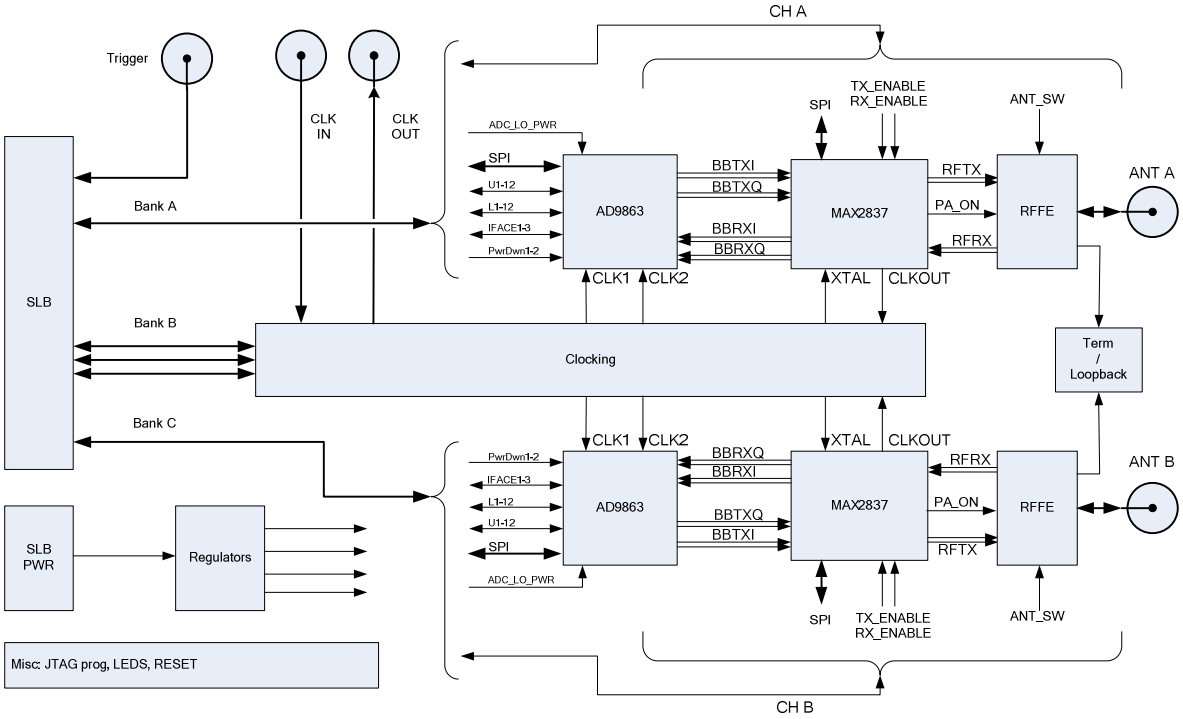


Figure 1 - Block Diagram.

The SLB mezzanine module is connected to the based module via SLB data and SLB power connectors. The FPGA directly accesses the transceivers and MxFE chips.

A wide range of SLB base modules are available to be paired with the SMT903, including Virtex-2Pro, Virtex-4 and Virtex-5 (Xilinx FPGAs) modules, that can implement control operations as well as some signal processing and communicate through the digital communication links to other Sundance modules.

In cases where more FPGA gates are required or to extend the processing chain, SHB connectors are available on the base module for fast data transfers. (see Sundance High-speed Bus - SHB - specifications).

4.2 Module Description

Wimax transceivers: The chip, by Maxim, can support Wimax bandwidth from 1.75 to 28 MHz. The transceivers used on the SMT903 are IEEE 802.16-2004 compliant and support OFDM up to 64-QAM. The following figure shows the high level block diagram of the MAX2837:

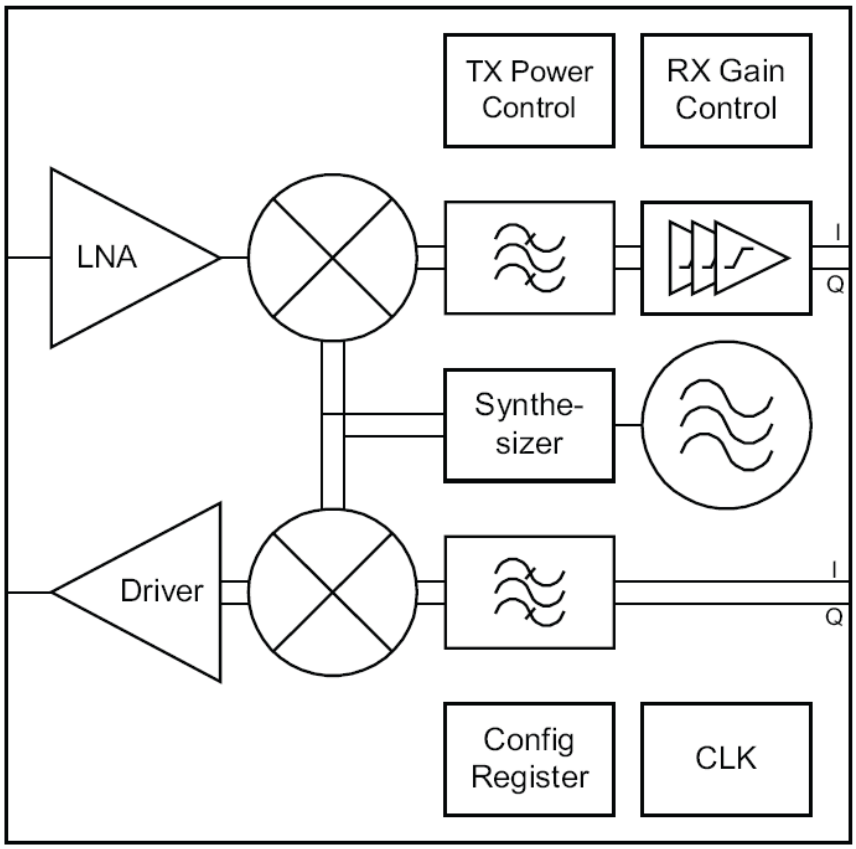


Figure 2 – MAX2837

Clock Distribution Circuit: ensures distribution of clock signals to the converters and transceiver, which is essential for such module an especially if used in a multi-transceiver configuration.

AD9863 Mixed-Signal Front-End: the MxFE is an integrated solution for analog to digital and digital to analog conversion. Single-chip architecture integrates two ADCs and two DACs with 12 bit resolution and more then 70 dBc SFDR.

External input and output clocks: they are to facilitate synchronisation with other modules. This can be used for cascading several SMT903 modules.

Power Supplies : they are all based on linear regulator with high rejection noise figures in order to provide power rails as clean of noise as possible. All are sourced from the SLB power connector.

FPGA base board: It is responsible for programming registers of all components on the board. Most components on the board have Serial Port Interfaces (SPI) and their registers can be programmed via serial interfaces via the SLB bus.

4.3 Interface Description

4.3.1 Mechanical Interface

The SMT903, as being an SLB mezzanine board, is matted on an SLB base module. The pair of modules is attached together using nylon and/or metal screws combined with 5mm spacers.

The WiMax RF connectors are SMAs, which are coaxial RF connectors with a screw type coupling mechanism to ensure good electrical performance. Clocks and trigger connectors are MMCX snap connectors.

4.3.2 Electrical Interface

The SMT903 is electrically connected to its base module it is coupled with using an SLB data connector and a SLB power connector.

The female differential connector is located on the base module. The Samtec Part Number for this connector is QTH-060-01-F-D-DP-A.

The female power connector is located on the base module. The Samtec Part Number for this connector is BKS-133-03-F-V-A

The male differential connector is located on the mezzanine card. The Samtec Part Number for this connector is QSH-060-01-F-D-DP-A

The male power connector is located on the mezzanine card. The Samtec Part Number for this connector is BKT-133-03-F-V-A

The mated height between the main module and the daughter card is 5 mm.

SMA connectors are rated for frequency up to 18GHz. In this case the frequency band is 2.5GHz.

5 Verification Procedures

6 Review Procedures

7 Validation Procedures

8 Timing Diagrams

9 Circuit Description / Diagrams

9.1 Clocking

The following figure shows the clocking diagram of the SMT903 SLB Mezzanine Module:

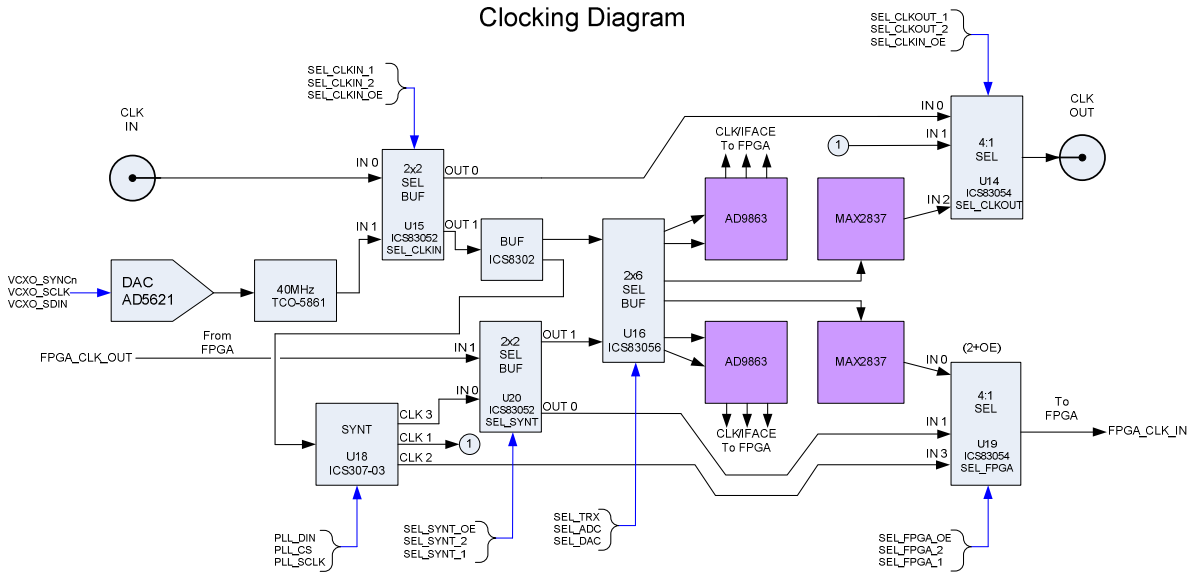


Figure 3 – Clocking Diagram.

The diagram shows how the SMT903 drives clock to the two transceivers and two Mixed-Signal Front End converters. All clocks are 3.3V single ended clocks.

The following clock sources are available to drive the system

(1) A VCTCXO (TCO-5851) Clock oscillator with nominal frequency of 40 MHz fine-frequency tuneable by analog voltage provided by serially controlled Analog to digital converter (AD5621)

(2) External clock from MMCX connector J5.

(3) ICS307-03 Synthesizer with the above 40MHz clock serves as a reference clock.

(4) Clock driven from the FPGA main module (Note: this is a high jitter clock and performance may be degraded).

Both RF transceivers are driven from the same clock source. Both AD9863 are driven from the same sources however ADC/RX clock (CLK1) and DAC/TX clock (CLK2) can each have separate clock frequency.

The FPGA can receive reference clock from one of the following sources:

(1) Transceiver output (40MHz)

(2) Synthesizer output

(3) AD9863 (using IFACE2-3 outputs)

The Clock Out signal driven from MMCX connector J4 may be originated from one of the following sources:

(1) Transceiver output (40MHz)

(2) 40MHz VCTCXO Clock Oscillator

(3) Clock In

(4) Synthesizer output

9.2 RF Front End

In each channel the circuit between the RF connector and the transceiver contains the following circuit:

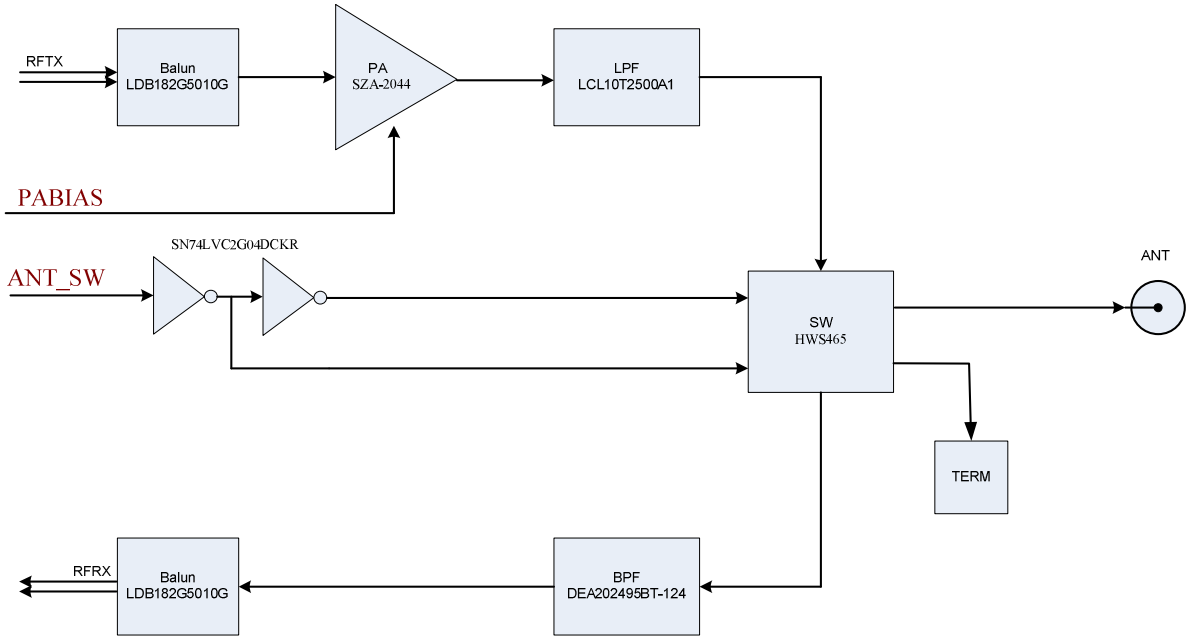


Figure 4 – RF Front End Block Diagram.

The ANT+SW signal coming from the SLB control the switch that determine if the channel is in TX or RX mode. The RX chain contains BPF and a BALUN. The TX chain contains a power amplifier which is controlled by PABIAS signal generated by the TRX to turn the power amplifier ON in TX mode and OFF in RX mode.

9.3 Loopback

Each channel has DPDT RF switch that connects the unused RF port to a terminator. The terminator is actually a 60dB attenuator that connects the two channel and enable testing loopback.

Figure 5 illustrate the loopback mode. In loopback mode one channel is acting as a transmitter and the other channel as a receiver; however, the switches (controlled directly from the FPGA) are set to the reverse mode (i.e. in the transmitting channel the switch is set to receive mode and vice versa). Transmitting 20dBm will produce a signal of -40 dBm in the receiver. One must also take into account that other signal components such as all kind of parasite coupling between the transmit path and the receive part might also be received. If antennas are installed a signal due to coupling between the antennas also will be presented. The strength of this signal depend on the coupling between the antennas but it is expected to be at least around 20 dB lower the loopback component as shown in the figure.

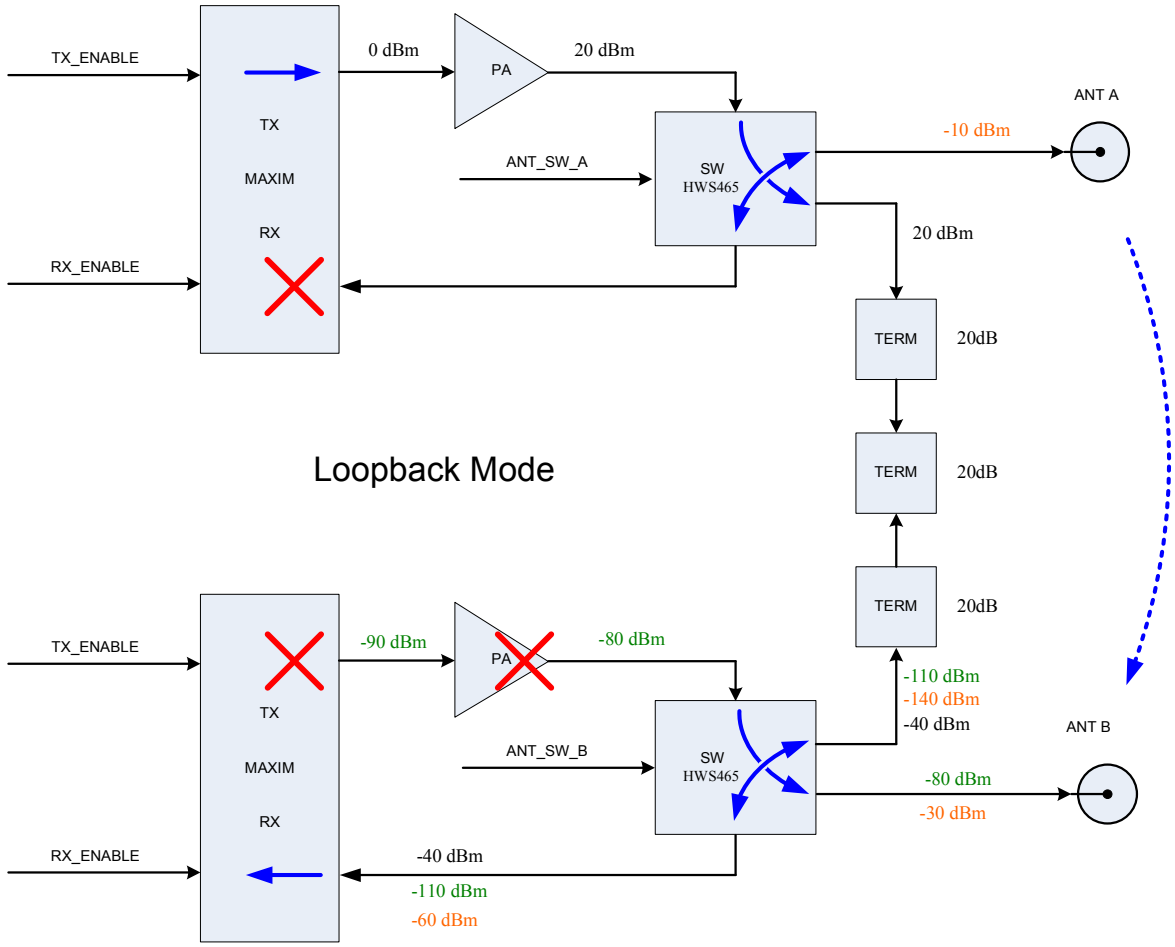


Figure 5 – Loopback mode.

In normal operation, when both channel are in transmit mode or receive mode the coupling the loopback signal produced between the channels do not interfere with proper operation of the module.

10 Board Layout

10.1 Top View

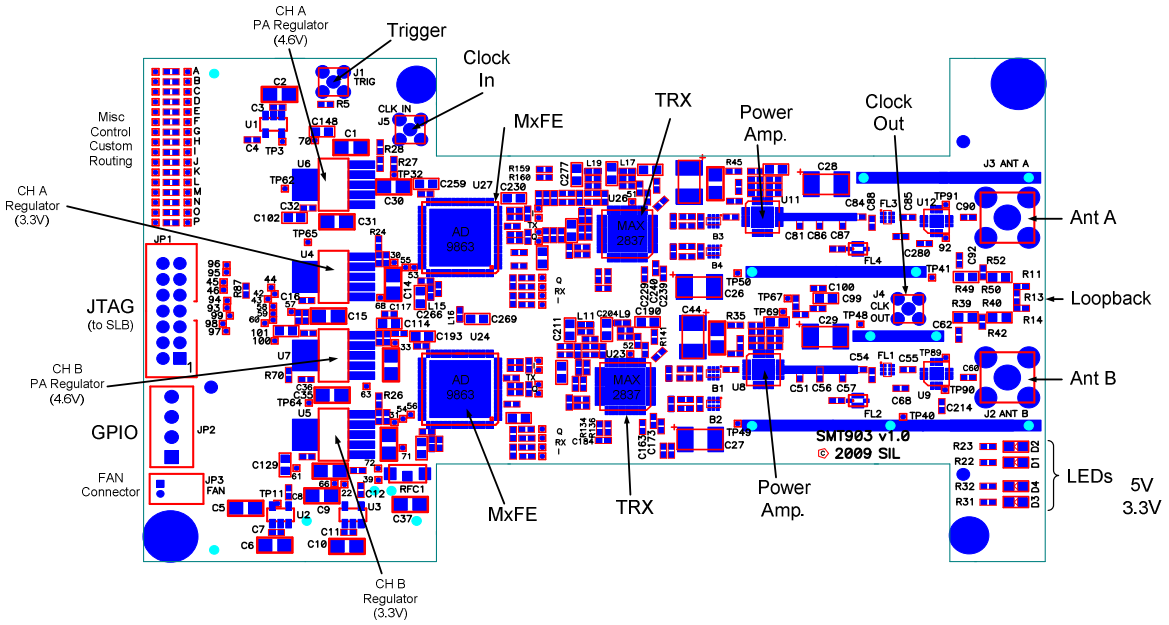


Figure 6 - Board Layout – top view.

10.2 Bottom View

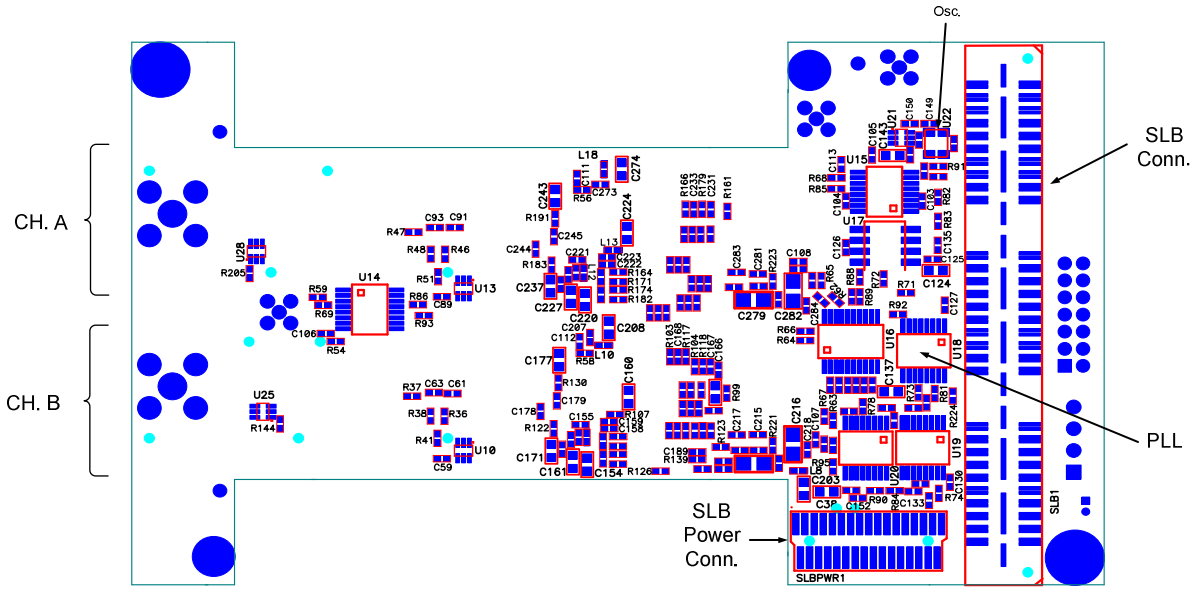
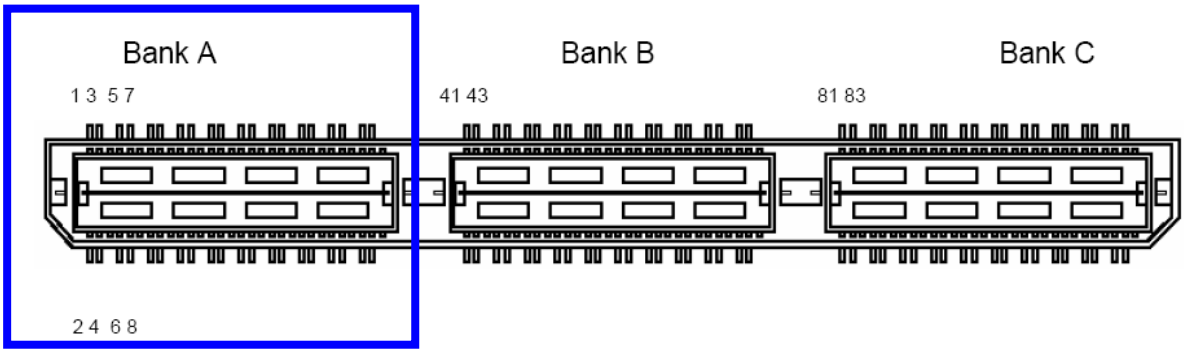


Figure 7 - Board Layout – bottom view.

11 Pinout

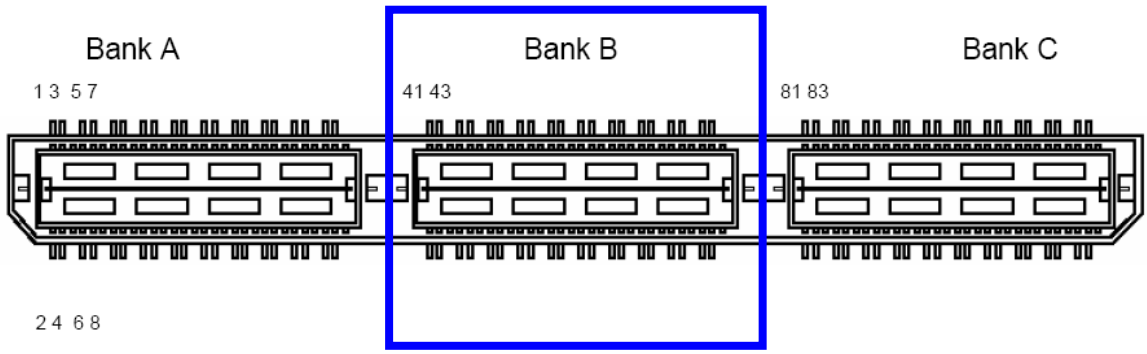
11.1 SLB Connector

Bank A



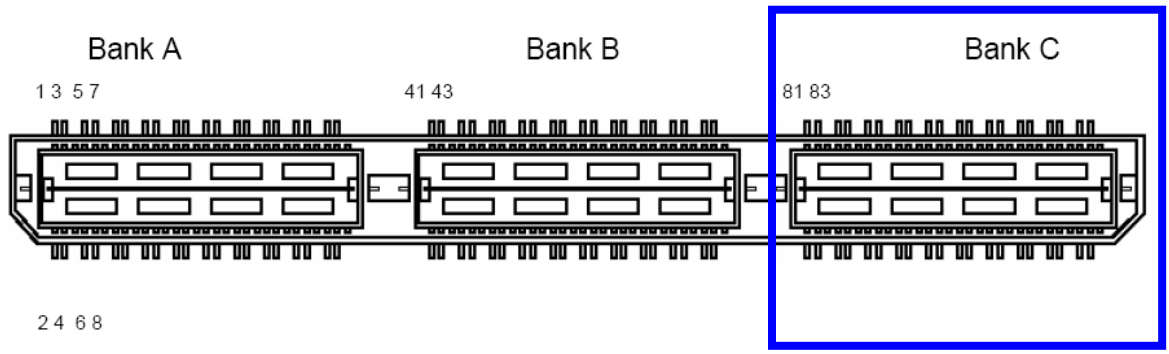
SLB		FPGA (SMT351T)	SMT903			Remarks
pin #	SLB name	pin name	component / section	pin_name	net_name	
1	DOAI0p	IO_L19P_12	U27 - AD9863 - MxFE A	U11	U11_A	
3	DOAI0n	IO_L19N_12	U27 - AD9863 - MxFE A	U10	U10_A	
5	DOAI1p	IO_L15P_12	U27 - AD9863 - MxFE A	U9	U9_A	
7	DOAI1n	IO_L15N_12	U27 - AD9863 - MxFE A	U8	U8_A	
9	DOAI2p	IO_L13P_12	U27 - AD9863 - MxFE A	U7	U7_A	
11	DOAI2n	IO_L13N_12	U27 - AD9863 - MxFE A	U6	U6_A	
13	DOAI3p	IO_L12P_12	U27 - AD9863 - MxFE A	U5	U5_A	
15	DOAI3n	IO_L12N_12	U27 - AD9863 - MxFE A	U4	U4_A	
17	DOAI4p	IO_L0P_12	U27 - AD9863 - MxFE A	U3	U3_A	
19	DOAI4n	IO_L0N_12	U27 - AD9863 - MxFE A	U2	U2_A	
21	DOAI5p	IO_L3P_12	U27 - AD9863 - MxFE A	U1	U1_A	
23	DOAI5n	IO_L3N_12	U27 - AD9863 - MxFE A	U0	U0_A	
25	DOAI6p	IO_L14P_12	Custom Routing	Row D	RxPwrDwn_A	Default: U27 - MxFE A \ TxPwrDwn
27	DOAI6n	IO_L14N_VREF_12	Custom Routing	Row C	TxPwrDwn_A	Default: U27 - MxFE A \ RxPwrDwn
29	DOAI7p	IO_L9P_CC_12	U27 - AD9863 - MxFE A	IFACE2	IFACE2_A	Connected to FPGA clock input
31	DOAI7n	IO_L9N_CC_12	U27 - AD9863 - MxFE A	SPI_CS	SPI_CS_A	
33	ClkOIp	IO_L8P_CC_12	U27 - AD9863 - MxFE A	IFACE3	IFACE3_A	Connected to FPGA clock input
35	ClkOIn	IO_L8N_CC_12	U26 - MAX2837 - TRX A	SCLK	TRX_SCLK_A	
37	FPGASysClkp	IO_L18P_12	U27 - AD9863 - MxFE A	IFACE1	IFACE1_A	
39	FPGASysClkn	IO_L18N_12	U27 - AD9863 - MxFE A	SPI_SDO	SPI_SDO_A	
2	DOBI0p	IO_L17P_12	U27 - AD9863 - MxFE A	L11	L11_A	
4	DOBI0n	IO_L17N_12	U27 - AD9863 - MxFE A	L10	L10_A	
6	DOBI1p	IO_L11P_CC_12	U27 - AD9863 - MxFE A	L9	L9_A	
8	DOBI1n	IO_L11N_CC_12	U27 - AD9863 - MxFE A	L8	L8_A	
10	DOBI2p	IO_L6P_12	U27 - AD9863 - MxFE A	L7	L7_A	
12	DOBI2n	IO_L6N_12	U27 - AD9863 - MxFE A	L6	L6_A	
14	DOBI3p	IO_L4P_12	U27 - AD9863 - MxFE A	L5	L5_A	
16	DOBI3n	IO_L4N_VREF_12	U27 - AD9863 - MxFE A	L4	L4_A	
18	DOBI4p	IO_L3P_12	U27 - AD9863 - MxFE A	L3	L3_A	
20	DOBI4n	IO_L3N_12	U27 - AD9863 - MxFE A	L2	L2_A	
22	DOBI5p	IO_L5P_12	U27 - AD9863 - MxFE A	L1	L1_A	
24	DOBI5n	IO_L5N_12	U27 - AD9863 - MxFE A	L0	L0_A	
26	DOBI6p	IO_L12P_VRN_12	U27 - AD9863 - MxFE A	SPI_DIO	SPI_SDO_A	
28	DOBI6n	IO_L12N_VRP_12	U27 - AD9863 - MxFE A	SPI_CLK	SPI_SCLK_A	
30	DOBI7p	IO_L7P_12	U26 - MAX2837 - TRX A	DOUT	TRX_DOUT_A	
32	DOBI7p	IO_L7N_12	U26 - MAX2837 - TRX A	DIN	TRX_DIN_A	
34	DOIRIp	IO_L16P_12	U26 - MAX2837 - TRX A	CS	TRX_CS_A	
36	DOIRIn	IO_L16N_12	U26 - MAX2837 - TRX A	RX_ENABLE	TRX_RX_EN_A	
38	ExtTriggerI0	IO_L10P_CC_12	RF FE A \ U12 \ RF SW	VC1, VC2	ANT_SW_A	
40	ExtTriggerI1	IO_L10N_CC_12	U26 - MAX2837 - TRX A	TX_ENABLE	TRX_TX_EN_A	

Bank B



SLB		FPGA (SMT351T)	SMT903			
pin #	SLB name	pin name	component / section	pin_name	net_name	Remarks
41	SMBClk	IO_L4P_10	LED D2		D0	Optionaly used in Costum Routing Row O
43	SMBnAlert	IO_L6N_20	JP2 - GPIO	Pin 2	D2	Optionaly used in Costum Routing Row G
45	Cntrl0	IO_L7N_20	J1	TRIG_IN	TRIG_IN	MMCX connector
47	Cntrl1	IO_L9N_CC_20	U24+U27 - MxFE A and B	RESETn	RESETn	Reset MxFE in both channels
49	PSEnable0	IO_L8P_CC_20	U19 - Clocking section	MUX OUT	FPGA_CLK_IN	Connected to FPGA clock input
51	Mode0	IO_L10P_CC_20	U20 - Clocking section	MUX IN	FPGA_CLK_OUT	
53	Signal0	IO_L11N_CC_20	U21 - AD5621 - DAC	SYNCn	VCXO_SYNCn	
55	Signal1	IO_L12N_VRP_20	U21 - AD5621 - DAC	SCLK	VCXO_SCLK	
57	Signal2	IO_L13N_20	U21 - AD5621 - DAC	SDIN	VCXO_SDIN	
59	Signal3	IO_L14N_VREF_20	U18 - ICS307-03 - PLL	DIN	PLL_DIN	
61	Signal4	IO_L15N_20	U18 - ICS307-03 - PLL	CS	PLL_CS	
63	Signal5	IO_L16N_20	U18 - ICS307-03 - PLL	SCLK	PLL_SCLK	
65	Cntrl4	IO_L17N_20	Clocking section	MUX SELECT	SEL_FPGA_1	See Details on clocking mode selection
67	Cntrl5	IO_L18N_20	Clocking section	MUX SELECT	SEL_FPGA_2	
69	Cntrl6	IO_L19N_20	Custom Routing	Row F	SHUTDOWNn	shoudown clocking and TRX A + B
71	FpgaTck	JTAG_CON	JP1	Pin 6	TCK	FPGA programming
73	FpgaTdi	JTAG_CON	JP1	Pin 10	TDI	FPGA programming
75	MspVRef	NC	NC			
77	MspTms	NC	NC			
79	Msptdo	NC	NC			
42	SMBData	IO_L6P_20	LED D1		D1	Optionaly used in Costum Routing Row J
44	SerialNo	IO_L7P_20	JP2 - GPIO	Pin 3	D3	Optionaly used in Costum Routing Row B
46	Cntrl2	IO_L8N_CC_20	Clocking section	MUX SELECT	SEL_CLKIN_1	See Details on clocking mode selection
48	Cntrl3	IO_L10N_CC_20	Clocking section	MUX SELECT	SEL_CLKIN_2	
50	PSEnable1	IO_L9P_CC_20	Custom Routing	Row L	CLOCK_OUT_OE	See details on custom routing
52	Mode1	IO_L11P_CC_20	Clocking section	MUX SELECT	SEL_SYNT_1	See Details on clocking mode selection
54	Signal6	IO_L12P_VRN_20	Clocking section	MUX SELECT	SEL_SYNT_2	
56	Signal7	IO_L13P_20	Custom Routing	Row K	ADC_LO_PWR	Default: MxFE A+B \ ADC_LO_PWR
58	Signal8	IO_L14P_20	Clocking section	MUX SELECT	SEL_CLKOUT_1	See Details on clocking mode selection
60	Signal9	IO_L15P_20	Clocking section	MUX SELECT	SEL_CLKOUT_2	
62	Signal10	IO_L16P_20	Custom Routing	Row E	TRX_RXHP	Default: TRX A+B \ RXHP
64	Signal11	IO_L17P_20	U16 - ICS83056 - clocking	SEL_TRX	SEL_TRX	See Details on clocking mode selection
66	Cntrl7	IO_L18P_20	U16 - ICS83056 - clocking	SEL_ADC	SEL_ADC	
68	Cntrl8	IO_L19P_20	U16 - ICS83056 - clocking	SEL_DAC	SEL_DAC	
70	FpgaVRef	JTAG_CON	JP1	Pin 2	VFPGAREF	FPGA programming
72	FpgaTms	JTAG_CON	JP1	Pin 4	TMS	FPGA programming
74	FpgaTdo	JTAG_CON	JP1	Pin 8	TDO	FPGA programming
76	MspTck	NC				
78	MspTdi	NC				
80	MspnTrst	NC				

Bank C



SLB		FPGA (SMT351T)	SMT903			
pin #	SLB name	pin name	component / section	pin_name	net_name	Remarks
81	DOAQ0p	IO_L19P_18	U24 - AD9863 - MxFE B	U11	U11_B	
83	DOAQ0n	IO_L19N_18	U24 - AD9863 - MxFE B	U10	U10_B	
85	DOAQ1p	IO_L15P_18	U24 - AD9863 - MxFE B	U9	U9_B	
87	DOAQ1n	IO_L15N_18	U24 - AD9863 - MxFE B	U8	U8_B	
89	DOAQ2p	IO_L4P_18	U24 - AD9863 - MxFE B	U7	U7_B	
91	DOAQ2n	IO_L4N_VREF_18	U24 - AD9863 - MxFE B	U6	U6_B	
93	DOAQ3p	IO_L13P_18	U24 - AD9863 - MxFE B	U5	U5_B	
95	DOAQ3n	IO_L13N_18	U24 - AD9863 - MxFE B	U4	U4_B	
97	DOAQ4p	IO_L0P_18	U24 - AD9863 - MxFE B	U3	U3_B	
99	DOAQ4n	IO_L0N_18	U24 - AD9863 - MxFE B	U2	U2_B	
101	DOAQ5p	IO_L7P_18	U24 - AD9863 - MxFE B	U1	U1_B	
103	DOAQ5n	IO_L7N_18	U24 - AD9863 - MxFE B	U0	U0_B	
105	DOAQ6p	IO_L10P_CC_18	U24 - AD9863 - MxFE B	IFACE2	IFACE2_B	Connected to FPGA clock input
107	DOAQ6n	IO_L10N_CC_18	Custom Routing	Row M	RxPwrDwn_B	Default: U24 - MxFE A \ RxPwrDwn
109	DOAQ7p	IO_L12P_VRN_18	U24 - AD9863 - MxFE B	IFACE1	IFACE1_B	
111	DOAQ7n	IO_L12N_VRP_18	Custom Routing	Row N	TxPwrDwn_B	Default: U24 - MxFE A \ TxPwrDwn
113	ClkOQp	IO_L8P_CC_18	U24 - AD9863 - MxFE B	IFACE3	IFACE3_B	Connected to FPGA clock input
115	ClkOQn	IO_L8N_CC_18	U24 - AD9863 - MxFE B	SPI_SDO	SPI_SDO_B	
117	FPGARslClkp	IO_L18P_18	U24 - AD9863 - MxFE B	SPI_CS	SPI_CS_B	
119	FPGARslClkn	IO_L18N_18	U24 - AD9863 - MxFE B	SPI_DIO	SPI_DIO_B	
82	DOBQ0p	IO_L17P_18	U24 - AD9863 - MxFE B	L11	L11_B	
84	DOBQ0n	IO_L17N_18	U24 - AD9863 - MxFE B	L10	L10_B	
86	DOBQ1p	IO_L11P_CC_18	U24 - AD9863 - MxFE B	L9	L9_B	
88	DOBQ1n	IO_L11N_CC_18	U24 - AD9863 - MxFE B	L8	L8_B	
90	DOBQ2p	IO_L6P_18	U24 - AD9863 - MxFE B	L7	L7_B	
92	DOBQ2n	IO_L6N_18	U24 - AD9863 - MxFE B	L6	L6_B	
94	DOBQ3p	IO_L2P_18	U24 - AD9863 - MxFE B	L5	L5_B	
96	DOBQ3n	IO_L2N_18	U24 - AD9863 - MxFE B	L4	L4_B	
98	DOBQ4p	IO_L1P_18	U24 - AD9863 - MxFE B	L3	L3_B	
100	DOBQ4n	IO_L1N_18	U24 - AD9863 - MxFE B	L2	L2_B	
102	DOBQ5p	IO_L5P_18	U24 - AD9863 - MxFE B	L1	L1_B	
104	DOBQ5n	IO_L5N_18	U24 - AD9863 - MxFE B	L0	L0_B	
106	DOBQ6p	IO_L3P_18	U24 - AD9863 - MxFE B	SPI_CLK	SPI_CLK_B	
108	DOBQ6n	IO_L3N_18	U23 - MAX2837 - TRX B	DOUT	TRX_DOUT_B	
110	DOBQ7p	IO_L9P_CC_18	U23 - MAX2837 - TRX B	DIN	TRX_DIN_B	
112	DOBQ7p	IO_L9N_CC_18	U23 - MAX2837 - TRX B	SCLK	TRX_SCLK_B	
114	DOIRQp	IO_L14P_18	U23 - MAX2837 - TRX B	CS	TRX_CS_B	
116	DOIRQn	IO_L14N_VREF_18	U23 - MAX2837 - TRX B	RX_ENABLE	TRX_RX_EN_B	
118	ExtTriggerQ0	IO_L16P_18	RF FE B \ U9 \ RF SW	VC1, VC2	ANT_SW_B	
120	ExtTriggerQ1	IO_L16N_18	U23 - MAX2837 - TRX B	TX_ENABLE	TRX_TX_EN_B	

11.2 Custom routing

All control signals for the SMT903 comes from the SLB connector, however the number of controlling signal is limited. Due to that fact less important control signals where combined together. In order to provide maximum flexibility some of those controlling signal are routed through a connection matrix located on the upper left of the board. The connection matrix is identified by rows A – P. The left side of each raw contains a signal coming from the SLB connector while the right side is connected to 16 different targets on the SMT903 board. The default signals routing is shown in the following figure and table.

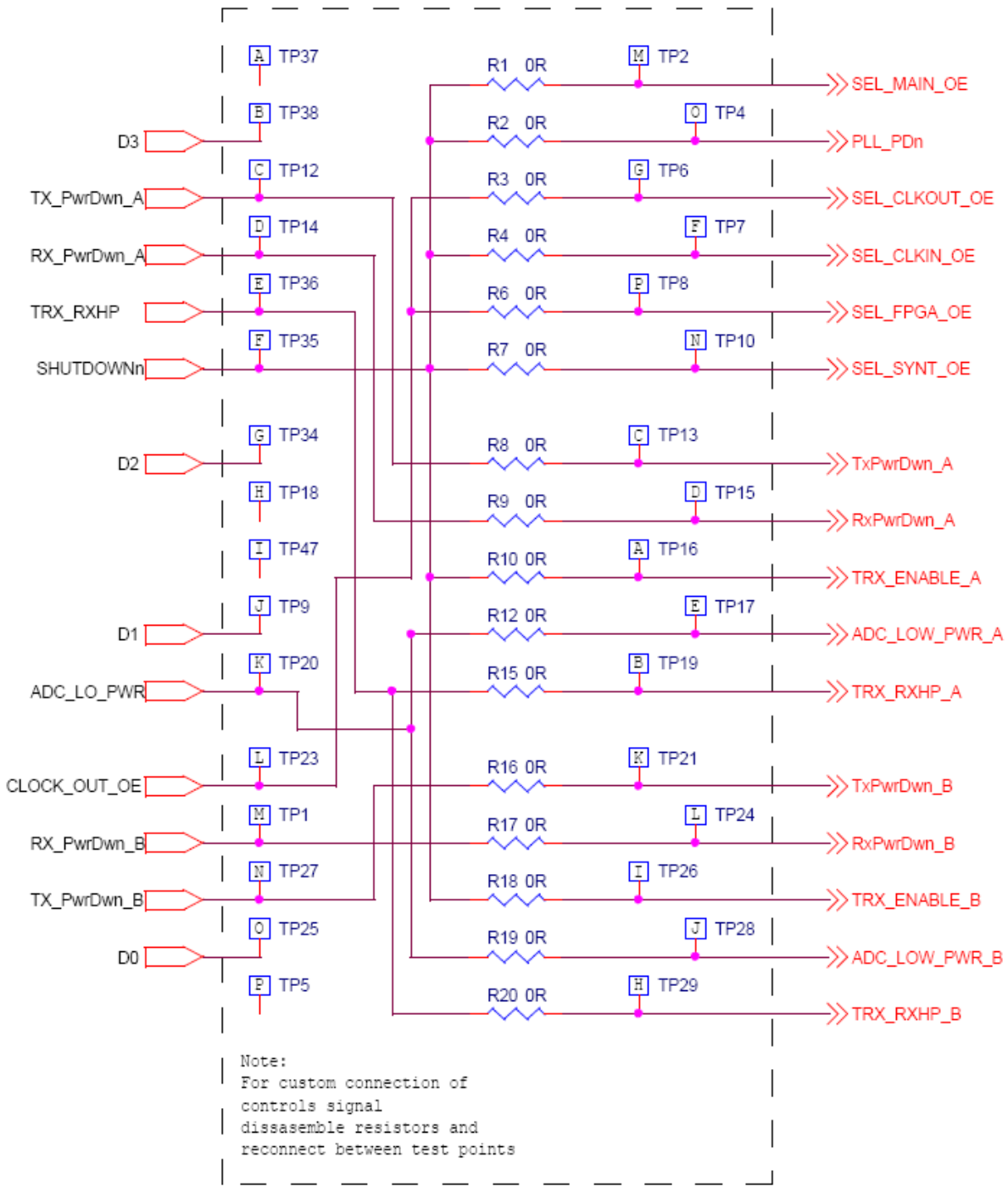


Figure 8 – Custom routing schematics

Row	Input connection			Output connection				Default
	SLB pin #	SMT903 net name		SMT903 net name	Component	pin name		Routing
A	No connection			TRX_ENABLE_A	TRX_A	ENABLE		F
B	44	D3		TRX_RXHP_A	TRX_A	RXHP		E
C	27	RxPwrDwn_A		TXPWRDWN_A	MxFE_A	TxPWRDWN		C
D	25	TxPwrDwn_A		RXPWRDWN_A	MxFE_A	RxPWRDWN		D
E	62	TRX_RXHP		ADC_LOW_PWR_A	MxFE_A	ADC_LOW_PWR		K
F	69	SHUTDOWNn		SEL_CLKIN_OE	Clocking MUX	OE		F
G	43	D2		SEL_CLKOUT_OE	Clocking MUX	OE		L
H	No connection			TRX_RXHP_B	TRX_B	RXHP		E
I	No connection			TRX_ENABLE_B	TRX_B	ENABLE		F
J	42	D1		ADC_LOW_PWR_B	MxFE_B	ADC_LOW_PWR		K
K	56	ADC_LO_PWR		TXPWRDWN_B	MxFE_B	TxPWRDWN		N
L	50	CLOCK_OUT_OE		RXPWRDWN_B	MxFE_B	RxPWRDWN		M
M	107	RxPwrDwn_B		SEL_MAIN_OE	Clocking MUX	OE		F
N	111	TxPwrDwn_B		SEL_SYNT_OE	Clocking MUX	OE		F
O	41	D0		PLL_PDN	PLL	PDN		F
P	No connection			SEL_FPGA_OE	Clocking MUX	OE		L

Table 1 – Custom routing

Default routing

Row A of custom routing matrix indicate no input is connected to row A and the output is connected to Enable signal of Transceiver of channel A. The defult routing indicate that it is connected to input row F, i.e. to the signal **SHUTDOWNn**. This signal is typically assert to '1' when module is active and assert to '0' when the module is non-active. As can be seen from the routing table **SHUTDOWNn** signal is connected to rows F, I, M, N and O as well shouting down Transceiver of channel B, PLL and several clock multiplexers in the same time. RXHP signal of TRX A and B are connected together as well as ADC_LOW_PWR of channel A and B MxFE. The Tx and Rx power down control signals of the MxFE are connected to dedicated signal in the SLB connector and the multiplexers of the clock outputs from the module to the connector and the FPGA can be shutdown using the signal **CLOCK_OUT_OE** coming from pin 50 of the SLB.

Default routing is designed to be suited for most applications. However, if one wishes to control specific control signal differently one need to disconnect the resistor on that row and connect the output test point to the selected input test point. Four signals: 2 general purpose led signal and two general purpose IO signals can be utilized for that purpose.

11.3 Connectors list

Reference	Type	Remarks
J1	MMCX	Trigger in 3.3V LVCMOS
J2	SMA	ANTENNA B
J3	SMA	ANTENNA A
J4	MMCX	CLK OUT
J5	MMCX	CLK IN
JP1	7x2 Header	JTAG
JP2	4x1 Header	GPIO
J3	2x1 Header	FAN Drive
SLB1	Samtec QSH-060-01-F-D-DP-A	120 pin SLB control con.
SLBPWR1	Samtec BKT-133-03-F-V-A	SLB power con.

Table 2 – connector list

The male differential connector is located on the mezzanine card. The Samtec Part Number for this connector is QSH-060-01-F-D-DP-A

The male power connector is located on the mezzanine card. The Samtec Part Number for this connector is BKT-133-03-F-V-A

11.4 Clocking configuration

Clock out source selection:

SEL_CLKIN_1	SEL_CLKOUT_1	SEL_CLKOUT_2	
0	0	0	CLK IN
X	0	1	PLL OUT 1
X	1	0	TRX CLK OUT
X	1	1	Not Valid
1	0	0	40MHz VCXO

Table 3 –Clock out source selection

FPGA clock in (SLP pin # 49) source selection

SEL_SYNT_1	SEL_FPGA_1	SEL_FPGA_2	
X	0	0	TRX CLK OUT
0	0	1	PLL OUT 3
1	0	1	FPGA CLK
X	1	0	Not Valid
X	1	1	PLL OUT 2

Table 4 – FPGA clock in source selection

TRX clock in source selection

SEL_TRX	SEL_CLKIN_2	SEL_SYNT_2	
0	0	X	CLK IN
0	1	X	40MHz VCXO
1	X	0	PLL OUT 3
1	X	1	FPGA CLK

Table 5 – TRX clock in source selection

ADC clock in source selection

SEL_ADC	SEL_CLKIN_2	SEL_SYNT_2	
0	0	X	CLK IN

0	1	X	40MHz VCXO
1	X	0	PLL OUT 3
1	X	1	FPGA CLK

Table 6 – ADC clock in source selection

DAC clock in source selection

SEL_DAC	SEL_CLKIN_2	SEL_SYNT_2	
0	0	X	CLK IN
0	1	X	40MHz VCXO
1	X	0	PLL OUT 3
1	X	1	FPGA CLK

Table 7 – DAC clock in source selection

12 Support Packages

The SMT903 is provided with an example code and the FPGA source to implement main interfaces in order for the user to get started quickly. Note that no Wimax FPGA core is provided.

13 Physical Properties

Dimensions	2.5" x 4.2" x	
Weight		
Supply Voltages		
Supply Current	+12V	0
	+5V	2A
	+3.3V	200mA
	-5V	0
	-12V	0
MTBF		

14 Safety

This module presents no hazard to the user when in normal use.

15 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.