Unit / Module Description:	This Document provides an overview of the developed system key features.
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SMT9091

SMT148-FX-SMT351T/SMT391

Abstract

This document describes the system, the necessary tools and the examples provided to get started

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Revision History

Issue	Changes Made	Date	Initials
1.0.0		22/06/08	E.P
1.0.1	Addition of Hardware revision table	25/06/08	E.P

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1 Introduction

The *SMT9091* is a demonstration software for the evaluation of the *SMT148-FX*, *SMT351T*, *SMt362* and *SMT391* modules. It can be used for Broadband cable modem head-end systems, Wireless infrastructure applications, 3G/4G Radio transceivers, Software Defined Radio systems, Medical imaging systems, Spectrum analysers, High-speed data acquisition system with or without digital processor.

2 Related Documents

2.1 Referenced Documents

Atmel Dual Channel ADC: AT84AD001

3LDiamond© User Guide

2.2 Applicable Documents

All the Sundance products User Guides are available from our website:

http://www.sundance.com/web/files/doc.asp

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

TIM	Texas Instruments Module
TI© DSP	Texas Instrument Digital Signal Processor
Comport	Communication Port. Standard communication interface developped by T.I
Xilinx© FPGA	Xilinx© Field Programmable Gate Array.
SLink	Sundance link
CP	ComPort. Communication interface
RSL	Rocket Serial Link
SHB	Sundance High-Speed Bus. Communication interface
DDR	Dual Data Rate
TxCy	Denomination for TIM site x Comport y. x=0, 1, 2, 3 and y=0, 1, 2, 3, 4, 5 on a TIM carrier board.

3.2 Definitions

DSP Module	Typically a TIM module hosting a TI DSP and, a Xilinx FPGA.
FPGA-only Module	A TIM with no on-board DSP, where the FPGA provides all functionality.
Firmware	A proprietary FPGA design providing some sort of functionality. Sundance Firmware is the firmware running in an FPGA of a DSP module.
Source Synchronous	The timing of unidirectional data signals is referenced to a clock sourced by the same device that generates those signals, and not to a global clock
Dual Data Rate	data toggles on both the rising and falling edges of the clock signal
Root	The starting point in every Diamond application is a processor (DSP or FPGA) called **root**. The root acts as the base of the network and a reference for locating all other processors.
Node	It is a processor (DSP or FPGA) that can be reached from the root by following wires through other processors

4 Tools Overview

Software Tools used for the system development and release:

Tools	Version
Sundance	
Wizard	v3.01.0000
SMT6001	v7.05.0000
SMT6012	v 5.03.0000
SMT6300	V5.00.0000
SMT6048	V3.03.0000
3L Diamond	
Diamond DSP+FPGA	V3.1.10 + sp4 available from 3L Diamond
Diamond IDE	V1.0.0 + update available from 3L Diamond
Texas instrument	
Code Composer Studio	V3.3
Xilinx	
ISE	9.2 sp4, IP udate 4.

Table 1: Tools

4.1 Sundance Wizard

The Sundance Wizard (http://support.sundance.com/updates/wizard/setup.exe.) will automatically install the latest version of the support packages required by your system.

In particular:

- SMT6012: Drivers for T.I Code Composer Studio
- SMT6001: Download Utility tool for the DSP module Flash.
- SMT6300: Drivers for Sundance PCI Hardware and server utility.

The Sundance help file (Sundance.chm) describes the hardware, firmware and software tools needed to use your Sundance Products. It is automatically installed by the "Sundance Wizard", but can be downloaded separately from
http://www.sundance.com/docs/Sundance.chm

4.2 SMT6048

This package (http://support.sundance.com/updates/smt6048/v3_03_0000/setup.exe.) is not yet part of the Wizard installation procedure and must be installed separately.

It provides the Host side USB interface to Sundance Hardware.

5 Hardware Overview

5.1 Hardware Set-up

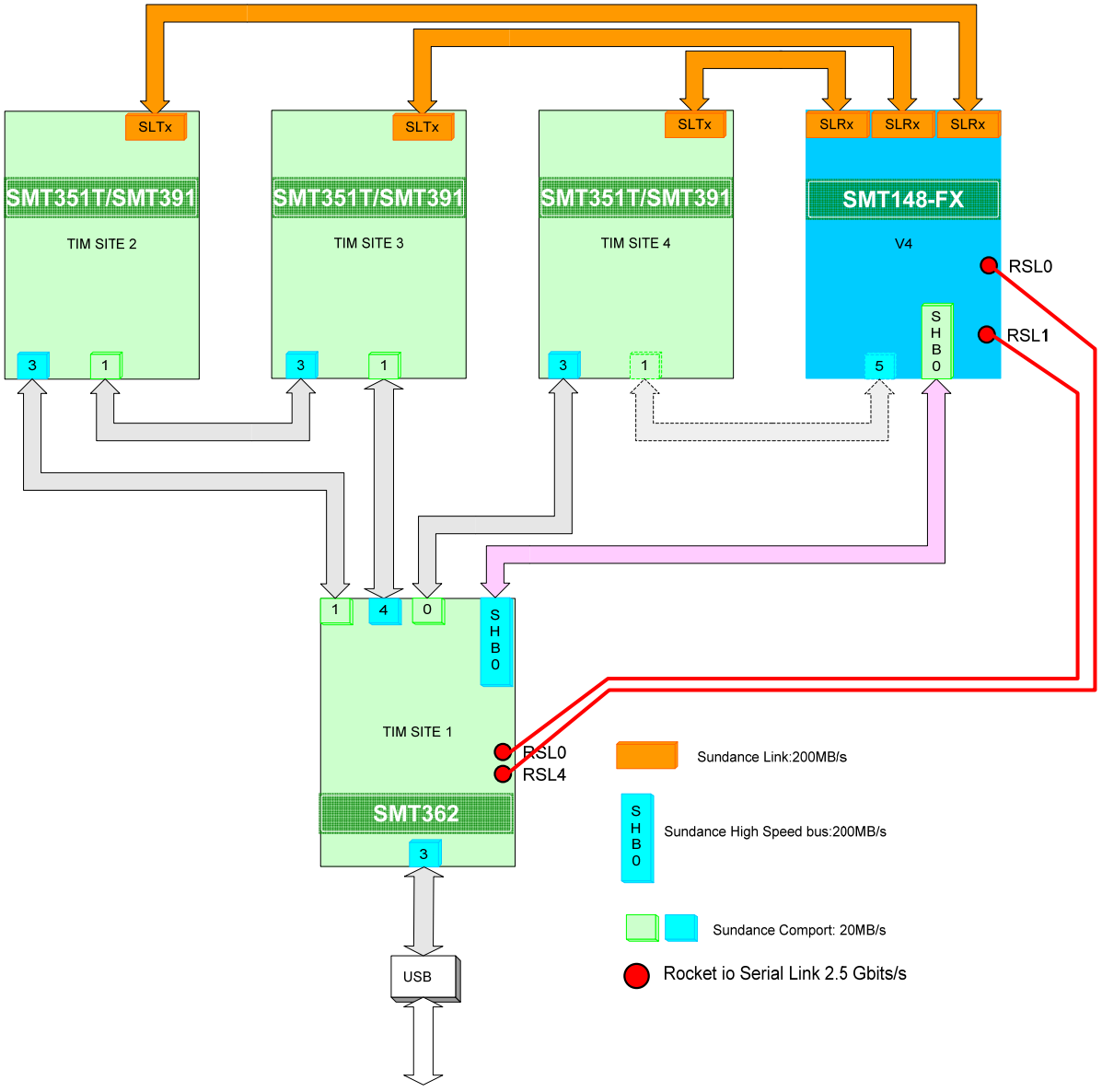

Figure 1: System Block Diagram

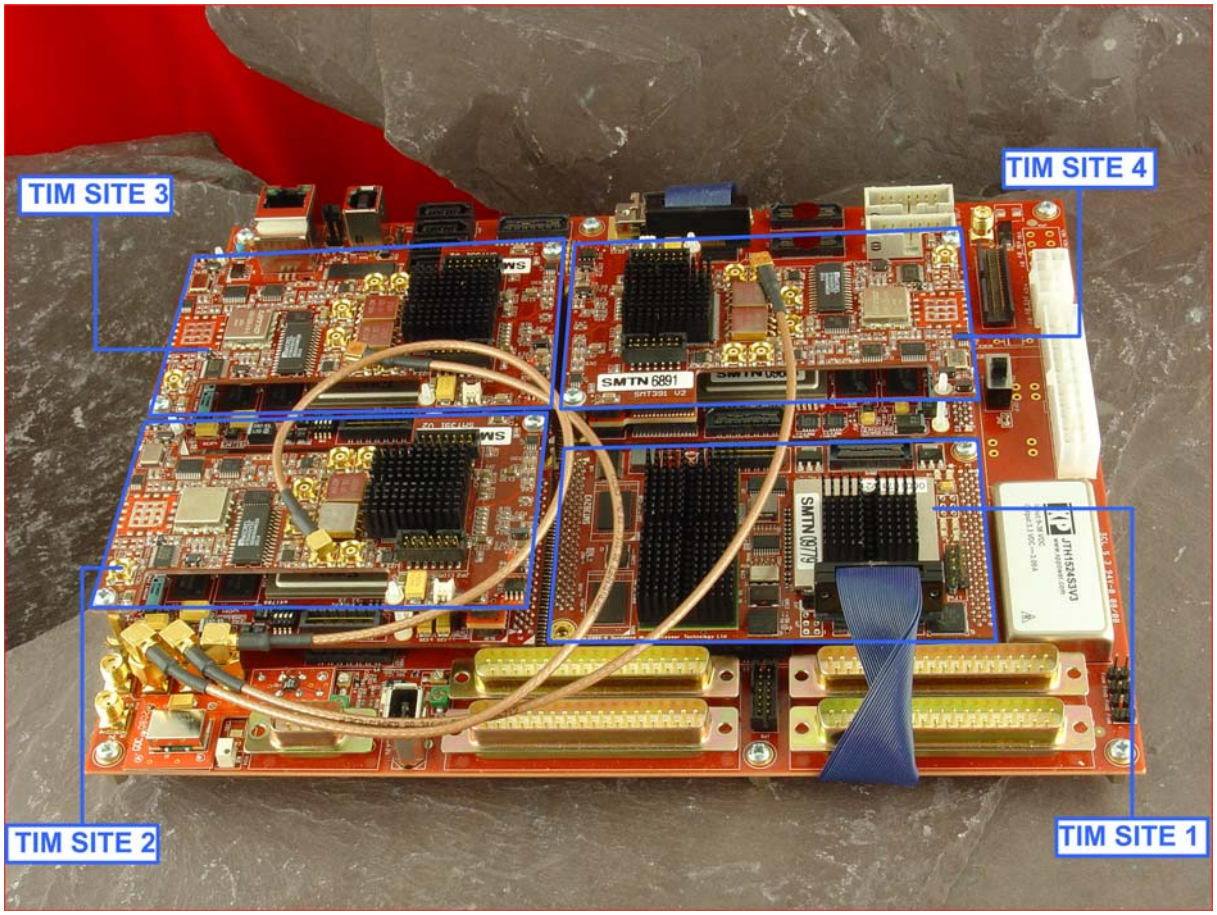

Figure 2: Top Hardware platform

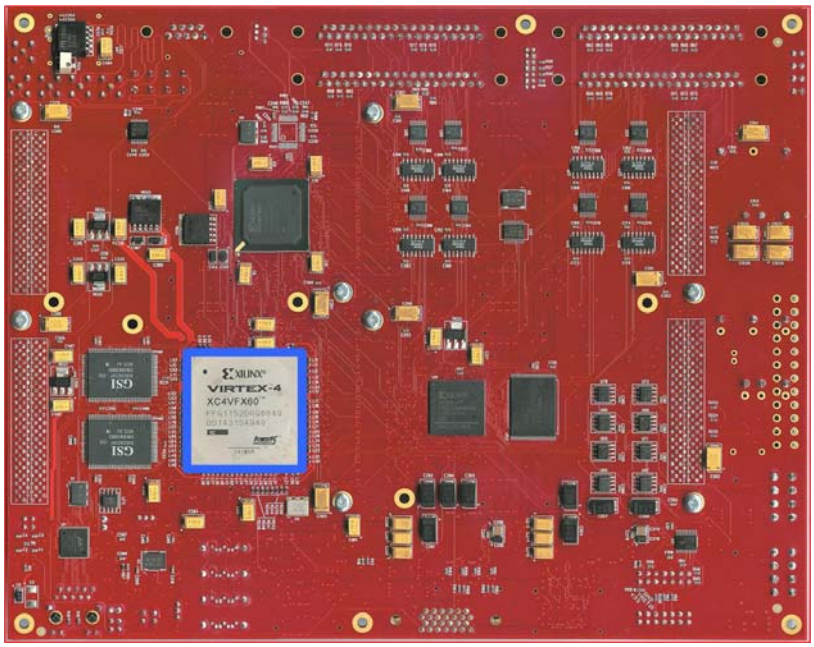

Figure 3: Bottom Hardware platform

5.2 Hardware Overview

Board	PCB revision	FPGA Firmware	CPLD code version
SMT148-FX	PCB version 3	SMT9091 v1.00	V4.0
SMT351T	PCB version 2	SMT9091 v1.00	V4.0
SMT362	PCB version 2	SMT9091 v1.00	Cpld_readback_hpi
SMT391	PCB version 1	N/A	N/A

Table 2: Boards Hardware status.

5.3 Digital Connections.

Four different types of links are used in this system:

Comports	
T1C0	T4C3
T1C1	T2C3
T1C3	USB
T1C4	T2C1
T2C1	T3C3
Sundance Links	
T2C0	Virtex4C0
T3C0	Virtex4C1
T4C0	Virtex4C3
SHB	
Virtex4SHB0	SMT362SHB0
RSLs	
Virtex4RSL0	SMT362RSL4
Virtex4RSL1	SMT362RSL0

Table 3: hardware connections

5.3.1 Sundance Link

A unidirectional source synchronous DDR Link.

The Sundance Links do not have a dedicated physical Slink Bus, but are mapped onto Comport pins.

The data travels in DDR at the transmitter's frequency.

The links have been tested for frequencies up to 125MHz.

The data bus is 8-bit wide.

5.3.2 Comports

A bidirectional half-duplex asynchronous link.

These links are used to load the Diamond application from the Host onto the network of processors (can be a DSP or an FPGA) and to provide control/status information from/to the root processor to/from the node processors

The maximum data rate expected does not exceed 20MB/s

5.3.3 SHB

A bidirectional half-duplex source synchronous link.

It is used to communicate via cable between the SMT148-FX Virtex 4 and a TIM module equipped with an SHB connector. (i.e SMT362)

The SHB has been tested for frequencies up to 133 MHz.

The data bus is 32-bit wide.

5.3.4 RSLs

A bidirectional full-duplex serial link.

An RSL lane transfers data at 2.5Gbit/s with 8/10bit Encoding.

It has dedicated paths on the SMT148-FX PCB between the TIM sites and the Virtex4.

For the time being we only support communications between Virtex-4 FPGAs.

5.3.5 SLB

A bidirectional link.

It is not a specific bus but a general purpose interconnection bus.

It is split into data bus and control bus.

It interfaces the SMT391 to the SMT351T.

5.4 Analog connections

They are all relative to the SMT391 ADC mezzanines input signals with the following specifications:

ADC Analogue inputs	
Signal format	Single ended
Input voltage range	0.5Vp-p
Impedance	50Ω - terminated to ground
Analogue Bandwidth	ADC Bandwidth: 1500MHz RF Transformer: 500kHz to 1.5GHz (AC Coupled) RF Transformer: 500kHz to 1.0GHz (DC Coupled)
External sampling clock inputs	
Signal format	Single ended, 0.5Vp-p min; 0.9Vp-p max.
Frequency range	Up to 1000 MHz
External trigger inputs	
Signal format	LVPECL
Frequency range	Up to 250 MHz
***SMT391* Output**	
Output Data Width	8-Bits
Data Format	Binary
ADC Performance @ FS = 1 GSPS, FIN = 500 MHz (from Atmel datasheet)	
Spurious Free Dynamic Range (SFDR)	-57dBc
Signal to Noise and Distortion (SINAD)	45dB
Effective Number Of Bits (ENOB)	7.1 Bits
Total Harmonic Distortion (THD)	-55dB
Cross-talk channel I versus channel Q (Cr) FIN = 250 MHz, FS = 1 GHz	< -65dBc

Table 4: Analogue specifications

Note that the SMT148-FX can provide an external clock at the desired frequency synchronised foall all the SMT391s via

6 Application

A system demo based on this setup has been developed to illustrate the hardware capabilities and to provide a starting point for developers.

6.1 Software application

This application runs on the SMT362 root DSP only.

It configures the FPGA of the three SMT351Ts and configures the three SMT391s to sample the incoming signals. The samples are stored in a 16KB FIFO inside the FPGA of each SMT351T. The content of the FIFO is sent to the SMT362 for further processing (FFT) and display.

A GUI running on the host allows control of the system settings.

Everytime new settings are applied via the GUI, they are broadcasted to the three nodes.

The Host displays the three digitised analogue inputs and the FFT results of channel1 and 2.

The GUI allows the selection of:

- the sampling clock source: external, or onboard clock generators.
- The sampling clock Frequency.
- The analog gain
- The Offset compensation: refer to the ADC User Manual.
- The DRDA: The phase shift between the clock and data coming out of the ADC; refer to the ADC user Manual
- The Built in Test: Switches on the ADC test mode; refer to the ADC user Manual.

6.2 The root

It is represented by the SMT362.

To simplify the software application, only one DSP is used and controls all the FPGA communication resources, so the SMT362 standard firmware is not used in this demo.

The project to build a custom firmware is available.

The custom firmware is placed in the SMT362 flash using the SMT6001, so that the module loads this custom configuration at power up.

6.3 The Nodes

6.3.1 The TIM modules

They all implement the data acquisition and data transfer towards the SMT362.

The FPGA functionality is likely to be custom made with user tasks added to the original firmware.

So it is interesting to be able to try various bitstreams before the final version could be loaded in the SMT351T flash.

That is why the nodes are part of the network of processors being reprogrammed everytime the application is launched.

6.3.2 The SMT148-FX Virtex-4

It is mentioned as a node because it can be part of the network of processors being configured from the root in a Diamond application.

Nevertheless, this demo does not use the Virtex-4 for any other means than routing the data to the SMT362.

So its bitstream has been stored on the SMT148-FX flash to configure the Virtex-4 automatically at power up.

Nevertheless, it is possible to use it for more advanced functions and have it reconfigured everytime the application is loaded.

In this case, a link needs to be added, between TIM site 4 and Virtex-4 as in Figure 1 (dotted link).

6.4 The Data flow

3 Channels are implemented and are represented in 3 different colours on Figure 4.

Data flows from the ADC output on the SMT391, through the SMT351T, to the SMT148-FX Virtex-4, arrive on the SMT362 where it is sent via the USB to the HOST for display.

: Channel 1

: Channel 2

: Channel 3

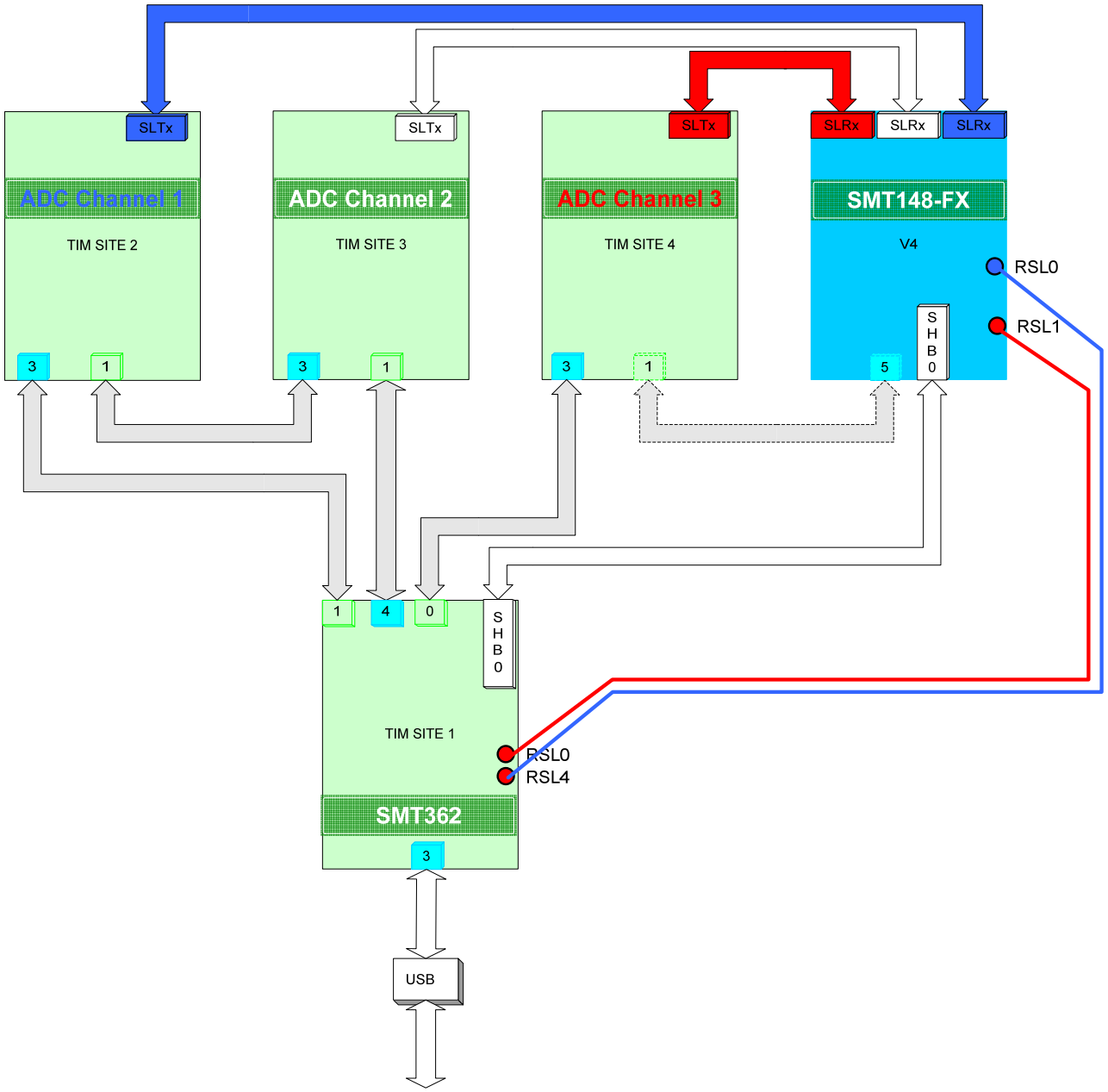

Figure 4: Data flow