Unit / Module Description:	Quad ADC (14bits/250MSPS) SLB Module
Unit / Module Number:	SMT941
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Product Specification for SMT941

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Revision History

Issue	Changes Made	Date	Initials
1	Initial Document created	26/05/08	PhSR
2	Part numbers corrected	20/04/09	PhSR

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1 Introduction

The *SMT941* is a single width expansion TIM that plugs onto an SLB base module, the SMT351T (Virtex-5 LXT or SXT FPGA) as an example and incorporates 2 dual-channel Analog-to-Digital Converters (ADS62P49). The *SMT941* implements a comprehensive clock circuitry based on a chip (CDCE72010) from Texas instrument that allows synchronisation among the converters and the use of an external reference clock. It provides a complete conversion solution and stands as a platform that can be part of a transmit/receive base station. The SMT941 has an on-board VCXO of 245.76MHz.

ADCs are 14-bit and can sample at up to 250 MHz. All converters are 1.8/3.3-Volt.

The Xilinx FPGA (Virtex-5 LXT or SXT series in the case of the SMT351T) on the base module is responsible for handling data going to one of the following destinations: converters, Comports, **R**ocket **S**erial **L**ink (RSL). These interfaces are compatible with a wide range of Sundance's modules.

The memory (DDR2) on the base module can store incoming and/or outgoing samples.

Converter configuration, sampling and transferring modes are set via internal control registers stored inside the FPGA and accessible via Comport.

The SMT941 module is well-suited for multi-carrier, wide bandwidth communication applications.

2 Related Documents

2.1 Referenced Documents

ADC datasheet: Texas Instrument ADS62P49.

Clock datasheet: Texas Instrument CDCE72010.

2.2 Applicable Documents

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

3.2 Definitions

4 Functional Description

4.1 Block Diagram

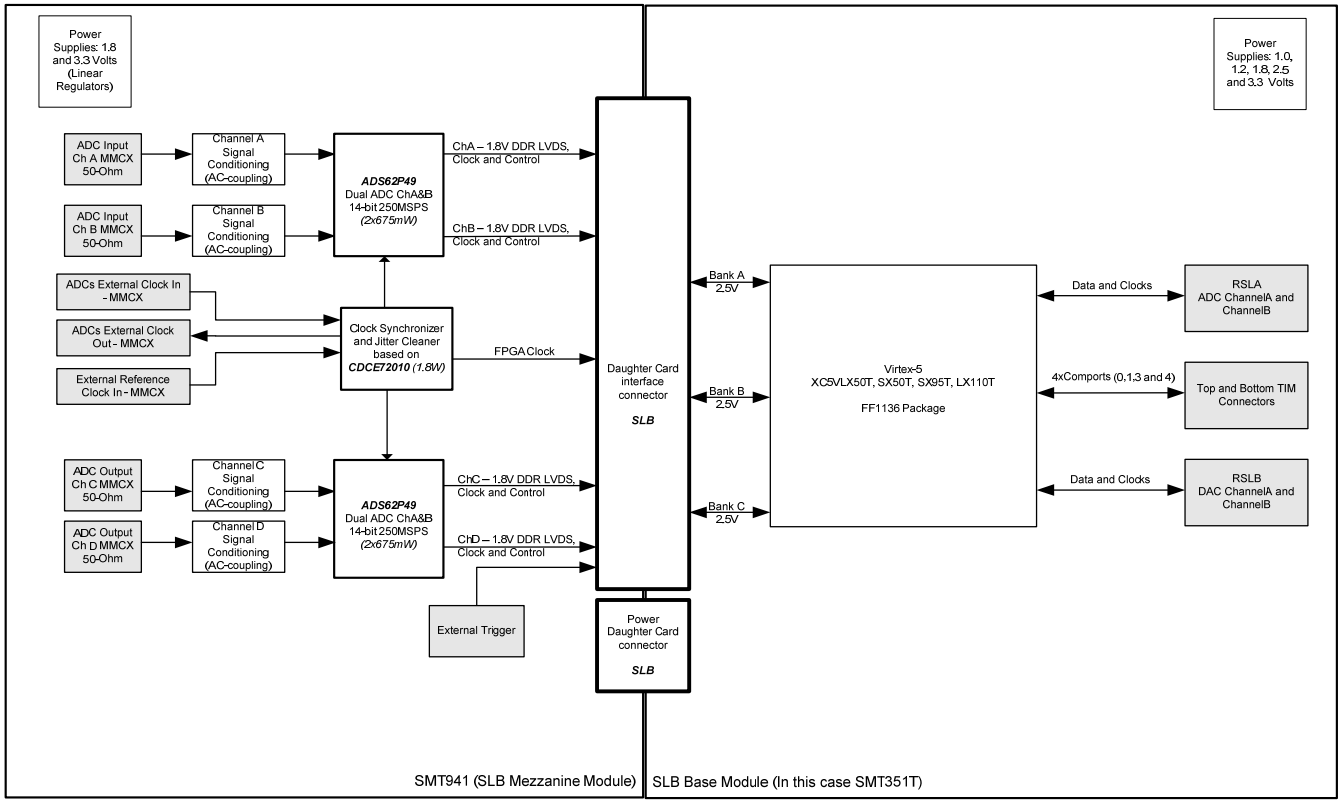

Figure 1 - Block diagram.

4.2 Module Description

The dual channel ADC (ADS62P49) has a resolution of 14 bits and can sample at up to 250 MHz. The chip incorporates a programmable fine gain of up to 6dBs for SNR/SFDR trade-off, a DC offset correction and an internal voltage reference. The ADC has got internal registers to implement the above functionalities and are accessible via a serial interface controlled by the FPGA on the SLB base module.

10 Footprint

10.1 Top View

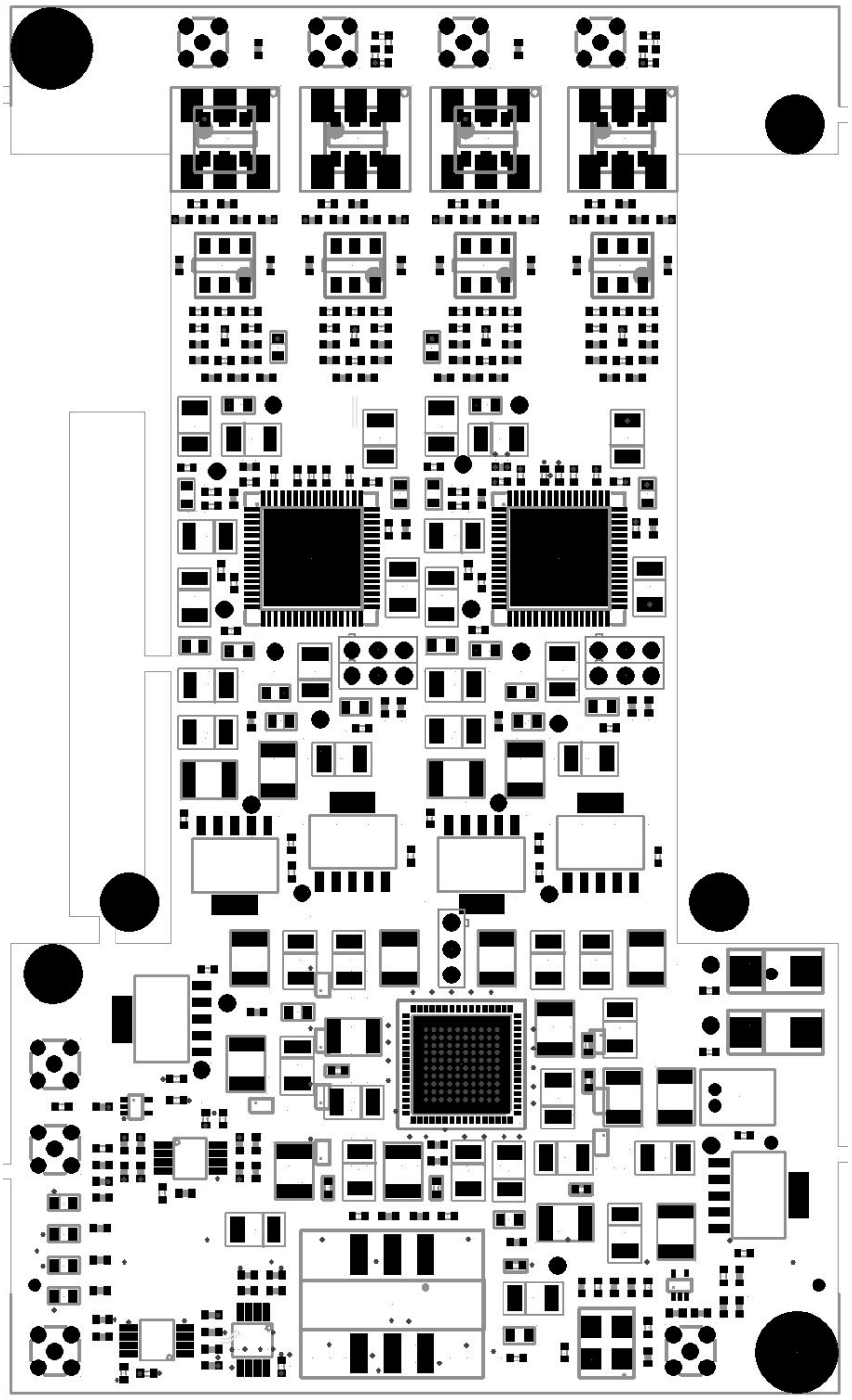

Figure 2 - Layout - Top Layer.

10.2 Bottom View

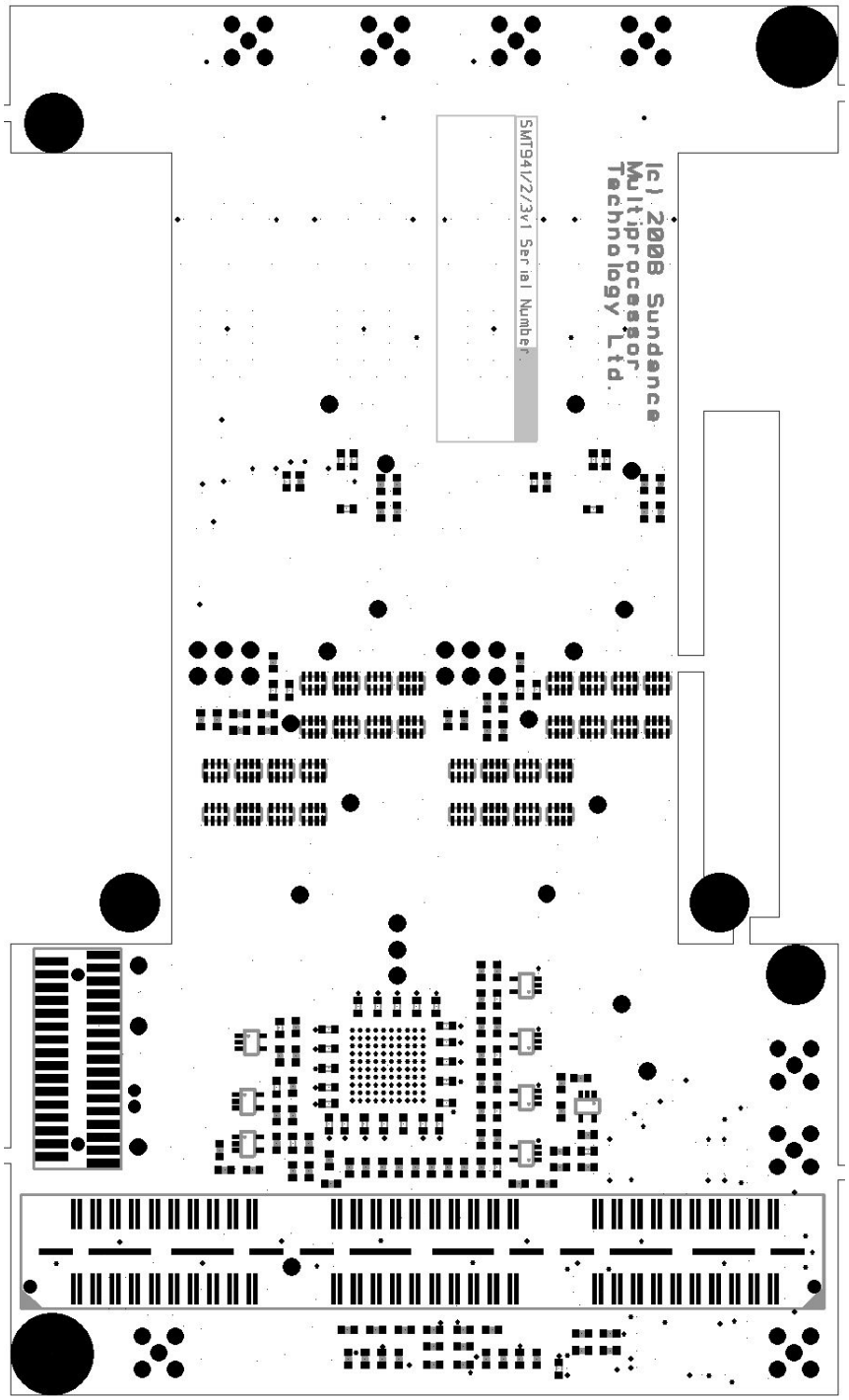

Figure 3 - Layout - Bottom Layer.

11 Pinout

12 Support Packages

13 Physical Properties

Dimensions		
Weight		
Supply Voltages		
Supply Current	+12V	
	+5V	
	+3.3V	
	-5V	
	-12V	
MTBF		

14 Safety

This module presents no hazard to the user when in normal use.

15 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.