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User Manual for SMT942

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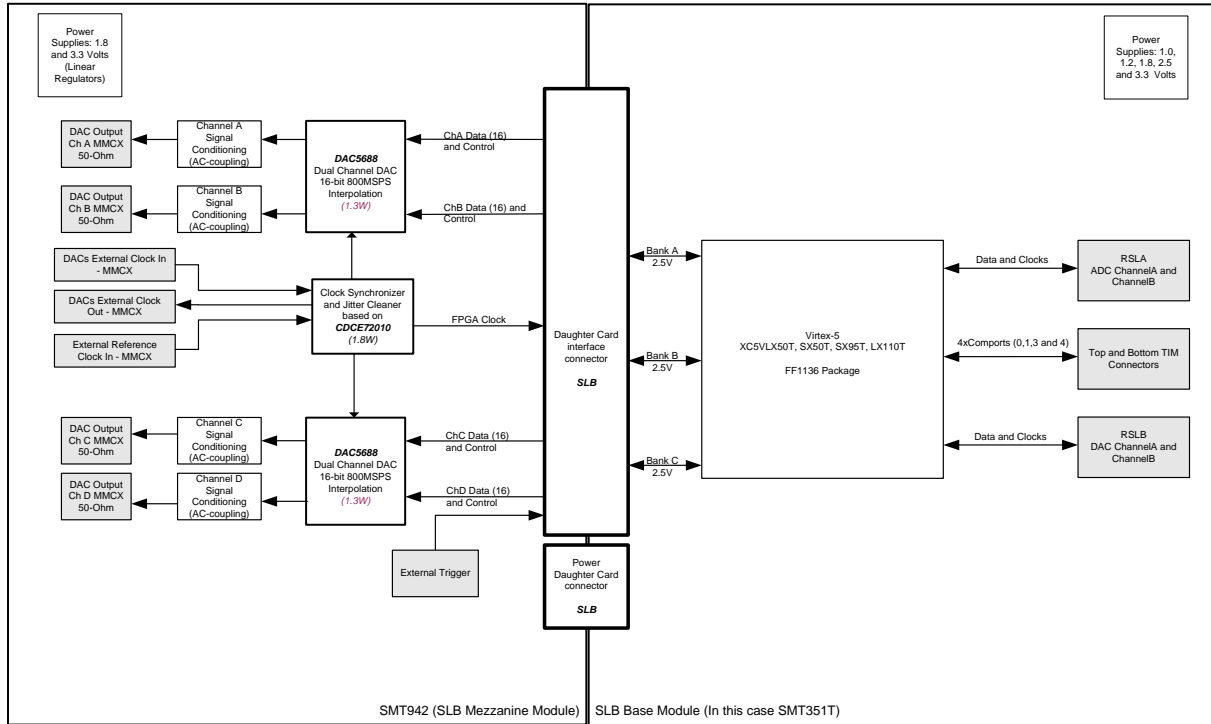


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Precautions

In order to guarantee that Sundance’s boards function correctly and to protect the module from damage, the following precautions should be taken:

- They are static sensitive products and should be handled accordingly. Always place the modules in a static protective bag during storage and transition.

Introduction

The *SMT942* is a single width expansion TIM that plugs onto an [SLB](#) base module, the [SMT351T](#) (Virtex-5 LXT, SXT or even FXT FPGA) as an example and incorporates 2 Texas Instrument dual-channel Digital-to-Analog Converters ([DAC5688](#)). The *SMT942* implements a comprehensive clock circuitry based on a chip ([CDCE72010](#)) from Texas instrument that allows synchronisation among the converters and the use of an external reference clock or sampling clock. It provides a complete conversion solution and stands as a platform that can be part of a transmit/receive base station. The *SMT942* has an on-board VCXO of frequency 245.76MHz.

DACs have a resolution of 16 bits and are able to update outputs at up to 800MSamples per second. All converters are 1.8/3.3-Volt. Among the features of the [DAC5688](#) are integrated interpolation filters, a fine frequency mixer with a complex NCO, a clock multiplier and IQ compensation. No DC-coupled version is currently available.

The [Xilinx FPGA](#) (Virtex-5 LXT or SXT series in the case of the *SMT351T*) on the base module is responsible for handling data coming from one of the following sources: Comports or Rocket Serial Link ([RSL](#)). These interfaces are compatible with a wide range of Sundance's modules.

The memory (DDR2) on the base module (still based on the case where using an *SMT351T* SLB base module) can store outgoing samples.

Converter configuration, sampling and transferring modes are set via internal control registers stored inside the FPGA and accessible via Comport.

The *SMT942* module is well-suited for multi-carrier, wide bandwidth communication applications.

The main features of the *SMT942* are listed below:

- Two Dual 16-bit 800MSPS DAC ([DAC5688](#)),
- On-board low-jitter clock distribution chip ([CDCE72010](#)),
- On-board 491.52MHz VCXO,
- On-board 10MHz reference crystal,
- One external clock, one external trigger and one reference clock inputs via [MMCX](#) connector,
- One external clock output via [MMCX](#) connector,
- One [SLB](#) connector to link *SMT942* and *SMT351T* as an example,
- All Analogue inputs to be connected to 50-Ohm sources.
- All Analogue outputs to be connected to 50-Ohm loads.
- Optional fan.

1 Related Documents

1.1 Referenced Documents

DAC datasheet: [Texas Instrument DAC5688](#).

Clock datasheet: [Texas Instrument CDCE72010](#).

1.2 Applicable Documents

2 Acronyms, Abbreviations and Definitions

2.1 Acronyms and Abbreviations

2.2 Definitions

3 Functional Description

3.1 Block Diagram

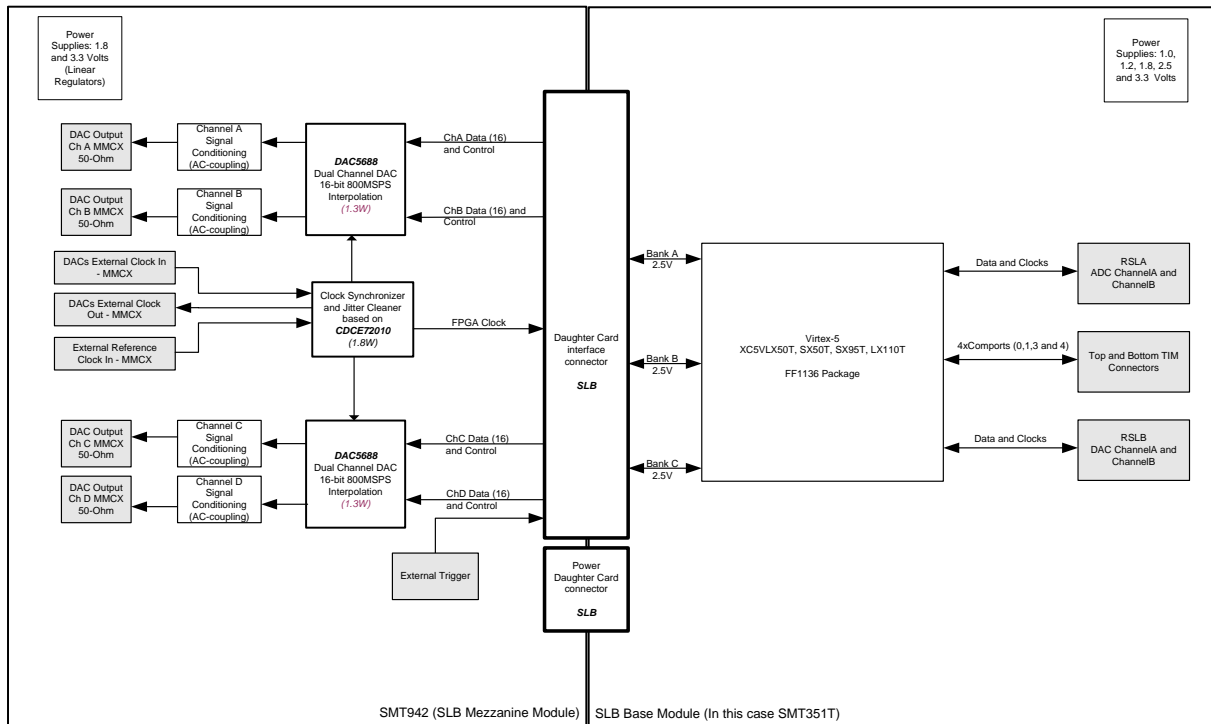


Figure 1 - SMT942 Block diagram.

3.2 Module Description

The SMT943 has got 2 dual channel DACs ([DAC5688](#) – Texas Instrument) that have integrated 2x-8x interpolation filters, a fine frequency mixer with a 32-bit complex numerically controlled oscillator, an on-board clock multiplier, an IQ compensation and an internal voltage reference.

A clock distribution chip ensures that all converters sample synchronously to a single clock source. The clock source can be external or internal (on-board 245.76-MHz VCXO). The distribution chip also allows synchronising the on-board VCXO to a reference signal that can be external or internal (on-board 10-MHz crystal). External reference, external sampling clock input and output are accessible on MMCX connectors. An external trigger input is also available on the board.

All control, data and clock lines are mapped onto an SLB connector so the card can be fully controlled by an SLB FPGA base module (SMT351T for example).

Some green LEDs are available on the board. A group of four LEDs is driven directly from the SLB base FPGA module and can be used to return status bits. Other individual LEDs should be lit and show that local power supplies are on.

3.2.1 D/A converters

The main characteristics of the SMT942 are gathered into the following table.

Analogue Outputs	
Output voltage range	1 V _{p-p} – Full scale - AC coupled
Impedance	DAC single-ended outputs are to be connected to a 50Ω load, which impedance matching implemented between DAC and RF transformers.
SFDR	89dBs maximum (manufacturer)
SNR	80dBs maximum (manufacturer)
Bandwidth	TBD
DAC Input	
Output Data Width per channel	16-Bits
Data Format	2's Compliment or offset binary (Changeable via control register)
SFDR	85dBs maximum (manufacturer)
SNR	73dBs maximum (manufacturer)
Maximum input data rate	250 MSPS (Clk1 – DAC5687)
Maximum Sampling rate	500 MSPS (Clk2 – DAC5687)

Jumper J1 disables (position 1-2; also called External Clock Mode) or enables (position 2-3; also called Internal Clock Mode) the DAC internal PLL.

3.2.2 Clock structure

External Reference Input	
Input Voltage Level	1 – 3.3 Volts peak-to-peak (AC-coupled)
Frequency Range	0 – 100 MHz
External Reference Output	
Output Voltage Level	1.6 Volts peak-to-peak (AC-coupled)
Output Impedance	50-Ohm (Termination implemented at the connector)
External Sampling Clock Input	
Input Voltage Level	1.5 – 3.3 Volts peak-to-peak (AC-coupled)
Input Format	Single-ended.
Frequency range	10-500 MHz
External Sampling Clock Output	
Output Voltage Level	0-2.4 Volts fixed amplitude
Output Format	LVTTTL
External Trigger Inputs	

Input Voltage Level	1.5-3.3 Volts peak-to-peak.
Format	DC-coupled and Single-ended (Termination implemented at the connector). Differential on option (3.3 V PECL).
Impedance	50-Ohm.
Frequency range	62.5 MHz maximum
Delay	
External Ref. Input to Ext Ref. Out	
External Clk Input to Ext Clk Out	9ns (between J29 and J4)

Figure 2 - Clock Architecture Main Characteristics.

3.3 Interface Description

3.3.1 Mechanical Interface

3.3.2 Electrical Interface

3.4 FPGA Design

3.4.1 Control Register Settings

The Control Registers control the complete functionality of the *SMT942*. They are setup via the Comport3 (standard firmware provided). The settings of the DACs, triggers, clocks and the configuration of the interfaces and the internal FPGA data path settings can be configured via the Control Registers.

3.4.1.1 Control Packet Structure

The data passed on to the *SMT942* over the Comport must conform to a certain packet structure. Only valid packets will be accepted and only after acceptance of a packet will the appropriate settings be implemented. Each packet will start with a command (4 bits - 0x1 for a write operation - 0x2 for a read operation) information, followed by a register address (12 bits - see table Memory Map), followed by a 16-bit data. This structure is illustrated in the following figure:

Byte	Byte Content							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	Command 3	Command 2	Command 1	Command 0	Address 11	Address 10	Address 9	Address 8
2	Address 7	Address 6	Address 5	Address 4	Address 3	Address 2	Address 1	Address 0
1	Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

Figure 3 – Setup Packet Structure.

3.4.1.2 Reading and Writing Registers

Control packets are sent to the *SMT942* over Comport3. This is a bi-directional interface. The format of a 'Read Packet' is the same as that of a write packet.

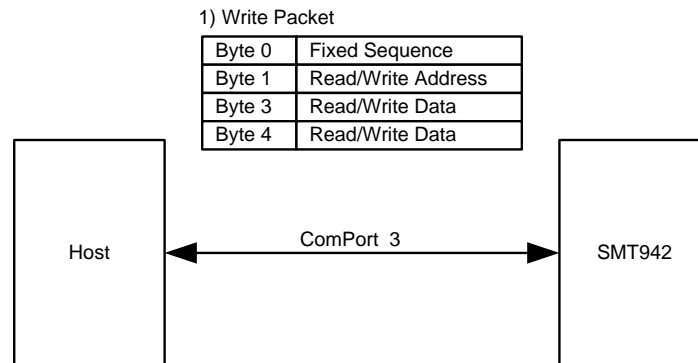


Figure 4 – Control Register Read Sequence.

3.4.1.3 Memory Map

The write packets must contain the address where the data must be written to and the read packets must contain the address where the required data must be read. The following figure shows the memory map for the writable and readable Control Registers on the *SMT942*:

Address	Writable Registers	Readable Registers
0x00	Reserved.	Reserved.
0x01	Board Control Register.	Firmware Version.
0x02	Reserved.	Clock Readback Register.
0x03	Reserved.	Board Status Register
Clock Section		
0x10	Clock Register 0x0.	Read-back (FPGA Register) Clock Register 0x0.
0x11	Clock Register 0x1.	Read-back (FPGA Register) Clock Register 0x1.
...
0x28	Clock Register 0x18.	Read-back (FPGA Register) Clock Register 0x18.
0x29	Clock Register 0x19.	Read-back (FPGA Register) Clock Register 0x19.
0x2A	Clock Readback Address Register (LSB)	
0x2B	Clock Readback Address Register (MSB)	
DACab Section		
0x30	DACab Register 0x0.	Read-back (FPGA Register) DACab Register 0x0.
0x31	DACab Register 0x1.	Read-back (FPGA Register) DACab Register 0x1.
...
0x3D	DACab Register 0xD.	Read-back (FPGA Register) DACab Register 0xD.

0x3E	DACab Register 0xE.	Read-back (FPGA Register) DACab Register 0xE.
DACcd Section		
0x40	DACcd Register 0x0.	Read-back (FPGA Register) DACcd Register 0x0.
0x41	DACcd Register 0x1.	Read-back (FPGA Register) DACcd Register 0x1.
...
0x4D	DACcd Register 0xD.	Read-back (FPGA Register) DACcd Register 0xD.
0x4E	DACcd Register 0xE.	Read-back (FPGA Register) DACcd Register 0xE.

Figure 5 – Register Memory Map.

Register Descriptions

3.4.2 Control Register – 0x1.

Control Register – 0x01								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Sync (chcd)	TxEnable (chcd)	Sync (chab)	TxEnable (chab)		Chcd_ReadnWrite	Chab_ReadnWrite	Clk_Readback
Default								
0	Chcd trigger selection	Chcd internal trigger	Chab trigger selection	Chab internal trigger		Chcd update	Chab update	clk update
Default	'0'	'0'	'0'	'0'		'0'	'0'	'0'

Clock Register 0 – 0x10		
Setting	Bit 0	Description clk update – clock chip register update
0	0	No action.
1	1	All clock registers are sent to the clock chip via its serial interface.
Setting	Bit 1	Description chab update – channel a and b register update
0	0	No action.
1	1	All registers (chab) are sent to the converter via its serial interface.
Setting	Bit 2	Description chcd update – channel c and d register update
0	1	No action.
1	1	All registers (chcd) are sent to the converter via its serial interface.
Setting	Bit 4	Description chab Internal trigger
0	0	No action.
1	1	Starts the data flow (converter chab).
Setting	Bit 5	Description chab trigger selection
0	0	Trigger from control register selected.
1	1	Trigger from external source selected.
Setting	Bit 6	Description chcd Internal trigger
0	0	No action.
1	1	Starts the data flow (converter chcd).

Setting	Bit 7	Description chcd trigger selection
0	0	Trigger from control register selected.
1	1	Trigger from external source selected.

CLOCK Register 0 – 0x10.

Clock Register 0 – 0x10								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved	Reserved	CP_DIR	CP_MODE	DELAY_PFD		REFSELCNTRL	VCXO_AUX_SEL
Default	'0'	'0'	'0'	'0'	'00'		'0'	'0'
0	SECSEL_PRISEL		Reserved		Reserved			
Default	'00'		'00'		'0000'			

Clock Register 0 – 0x10		
Setting	Bit 7:6	Description SECSEL_PRISEL – Reference Input Selection
0	00	Nothing Selected
1	01	On-board Reference selected
2	10	External Reference selected
3	11	Auto Selection (Not recommended)
Setting	Bit 8	Description VCXO_AUX_SEL – VCXO/AUX Selection
0	0	On-board or External Reference. Selected (SECSEL_PRI_SEL)
1	1	On-board VCXO or External Clock selected.
Setting	Bit 9	Description REFSELCNTRL – Reference selection mode
0	0	Reference selection made externally.
1	1	Reference selection made internally (using SECSEL_PRISEL.).
Setting	Bit 11:10	Description DELAY_PFD – PFD pulse width
0	00	
1	01	
2	10	
3	11	
Setting	Bit 12	Description CP_MODE
0	0	3V.
1	1	5V
Setting	Bit 13	Description CP_DIR
0	0	Positive CP current output
1	1	Negative CP current output

CLOCK Register 1 – 0x11.

Clock Register 1 – 0x11	
-------------------------	--

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Output0 (DAC chc&d clk1) Mode						PECLOHISWING	Reserved
Default	'100000'						'0'	'0'
0	Reserved		ICP				CP_PRE	Reserved
Default	'00'		'0000'				'0'	'0'

Reset Register 1 – 0x11		
Setting	Bit 1	Description CP_PRE - Preset charge pump output voltage to vcc/2
0	0	OFF.
1	1	ON.
Setting	Bit 5:2	Description ICP – Charge pump current setting
0	0	
1	1	
Setting	Bit 9	Description PECLOHISWING – PECL output voltage swing (DAC chc&d clk1)
0	0	Normal Operation.
1	1	High PECL output voltage.
Setting	Bit 15:10	Description Output0 (DAC chc&d clk1) mode
0	0	LVPECL only: '100000'.

CLOCK Register 2 – 0x12.

Clock Register 2 – 0x12									
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	Coarse Phase Adjustment[5:0] (Output DAC chc&d clk1 and clk2)						Reserved		
Default	'000000'						'00'		
0	Reserved				Reserved				
Default	'0011'				'0001'				

Reset Register 2 – 0x12		
Setting	Bit 15:10	Description Coarse Phase Adjustment[5:0] DAC chc&d clk1 and clk2
0	0	
1	1	

CLOCK Register 3 – 0x13.

Clock Register 3 – 0x13								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Output0 (DAC chc&d clk2) Mode						PECL1HISWING	Output Divider Enable

Default	'100000'	'0'	'0'
0	Output Divider Ratio DAC chc&d clk1 and clk2		Coarse Phase Adjustment[6]
Default	'0000000'		'0'

Reset Register 3 – 0x13		
Setting	Bit 0	Description – Coarse Phase Adjustment[6] DAC chc&d clk1 and clk2
0	0	
1	1	
Setting	Bit 7:1	Description – Output Divider Ratio DAC chc&d clk1 and clk2
0	0	
1	1	
Setting	Bit 8	Description – Output Divider Enable DAC chc&d clk1 and clk2
0	0	Divider disabled.
1	1	Divider enabled.
Setting	Bit 9	Description PECL1HISWING – PECL output voltage swing (DAC chc&d clk2)
0	0	Normal Operation.
1	1	High PECL output voltage.
Setting	Bit 15:10	Description Output1 (DAC chc&d clk2) mode
0	0	LVPECL only: '100000'.

CLOCK Register 4 – 0x14.

Clock Register 4 – 0x14								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Coarse Phase Adjustment[5:0] (Output DAC cha&b clk1)						Delay N[2:1]	
Default	'000000'						'00'	
0	Delay N[0]	Delay M			Reserved			
Default	'0'	'0'			'0010'			

Reset Register 4 – 0x14		
Setting	Bit 6:4	Description – Delay M
0	0	
1	1	
Setting	Bit 9:7	Description – Delay N
0	0	
1	1	
Setting	Bit 15:10	Description Coarse Phase Adjustment[5:0] DAC cha&b clk1
0	0	
1	1	

CLOCK Register 5 – 0x15.

Clock Register 5 – 0x15								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Output0 (DAC cha&b clk1) Mode						PECL2HISWING	Output Divider Enable
Default	'100000'						'0'	'0'
0	Output Divider Ratio DAC cha&b clk1							Coarse Phase Adjustment[6]
Default	'0000000'							'0'

Reset Register 5 – 0x15		
Setting	Bit 0	Description - Coarse Phase Adjustment[6] DAC cha&b clk1
0	0	
1	1	
Setting	Bit 7:1	Description – Output Divider Ratio DAC cha&b clk1
0	0	
1	1	
Setting	Bit 8	Description – Output Divider Enable DAC cha&b clk1
0	0	Divider disabled.
1	1	Divider enabled.
Setting	Bit 9	Description PECL2HISWING – PECL output voltage swing (DAC cha&b clk1)
0	0	Normal Operation.
1	1	High PECL output voltage.
Setting	Bit 15:10	Description Output2 (DAC cha&b clk1) mode
0	0	LVPECL only: '100000'.

CLOCK Register 6 – 0x16.

Clock Register 6 – 0x16								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Coarse Phase Adjustment[5:0] (Output DAC cha&b clk2)						BIAS_DIV23	
Default	'000000'						'00'	
0	BIAS_DIV01		Reserved	DIS_FDET_REF	Reserved			
Default	'00'		'0'	'0'	'0011'			

Reset Register 6 – 0x16		
Setting	Bit 4	Description – DIS_FDET_REF
0	0	Reference Clock detector is ON
1	1	Reference Clock detector is OFF
Setting	Bit 7:6	Description – BIAS_DIV01 – Current reduction output dividers 0 and 1
0	'00'	No current output reduction
1	'01'	20% output current reduction
2	'10'	30% output current reduction
Setting	Bit 9:8	Description – BIAS_DIV23 – Current reduction output dividers 2 and 3

0	'00'	No current output reduction
1	'01'	20% output current reduction
2	'10'	30% output current reduction
Setting	Bit 15:10	Description Coarse Phase Adjustment[5:0] DAC cha&b clk1
0	0	
1	1	

CLOCK Register 7 – 0x17.

Clock Register 7 – 0x17								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Output0 (DAC cha&b clk2) Mode						PECL3HISWING	Output Divider Enable
Default	'100000'						'0'	'0'
0	Output Divider Ratio DAC cha&b clk1 and clk2							Coarse Phase Adjustment[6]
Default	'0000000'							'0'

Reset Register 7 – 0x17		
Setting	Bit 0	Description - Coarse Phase Adjustment[6] DAC cha&b clk2
0	0	
1	1	
Setting	Bit 7:1	Description - Output Divider Ratio DAC cha&b clk2
0	0	
1	1	
Setting	Bit 8	Description - Output Divider Enable DAC cha&b clk2
0	0	Divider disabled.
1	1	Divider enabled.
Setting	Bit 9	Description PECL3HISWING - PECL output voltage swing (DAC cha&b clk2)
0	0	Normal Operation.
1	1	High PECL output voltage.
Setting	Bit 15:10	Description Output3 (DAC cha&b clk2) mode
0	0	LVPECL only: '100000'.

CLOCK Register 8 – 0x18.

Clock Register 8 – 0x18								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Coarse Phase Adjustment[5:0] (External Clock)						Reserved	HOLD_ON_LOR
Default	'000000'						'0'	'0'
0	Reserved				Reserved			

Default	'0000'	'0011'
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Reset Register 8 – 0x18		
Setting	Bit 8	Description – HOLD_ON_LOR
0	0	Normal mode of operation
1	1	Charge pump in tri-state mode
Setting	Bit 15:10	Description Coarse Phase Adjustment[5:0] External Clock
0	0	
1	1	

CLOCK Register 9 – 0x19.

Clock Register 9 – 0x19								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Output0 (External Clock) Mode						PECL4HISWING	Output Divider Enable
Default	'100000'						'0'	'0'
0	Output Divider Ratio External Clock							Coarse Phase Adjustment[6]
Default	'0000000'							'0'

Reset Register 9 – 0x19		
Setting	Bit 0	Description – Coarse Phase Adjustment[6] External Clock
0	0	
1	1	
Setting	Bit 7:1	Description – Output Divider Ratio External Clock
0	0	
1	1	
Setting	Bit 8	Description – Output Divider Enable External Clock
0	0	Divider disabled.
1	1	Divider enabled.
Setting	Bit 9	Description PECL4HISWING – PECL output voltage swing (External Clock)
0	0	Normal Operation.
1	1	High PECL output voltage.
Setting	Bit 15:10	Description Output4 (External Clock) mode
0	0	LVPECL only: '100000'.

CLOCK Register A – 0x1A.

Clock Register A – 0x1A								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

1	Reserved		Reserved
Default	'000000'		'00'
0	Reserved	BIAS_DIV45	Reserved
Default	'00'	'00'	'0101'

Reset Register A – 0x1A		
Setting	Bit 5:4	Description – BIAS_DIV01 – Current reduction output dividers 0 and 1
0	'00'	No current output reduction
1	'01'	20% output current reduction
2	'10'	30% output current reduction

CLOCK Register B – 0x1B.

Clock Register B – 0x1B								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved							
Default	'01101000'							
0	Reserved							
Default	'00000000'							

CLOCK Register C – 0x1C.

Clock Register C – 0x1C								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved						DET_START_BYPASS	FB_START_BYPASS
Default	'000000'						'0'	'0'
0	DIV2_DIS	DIV_SEL	Reserved	FB_FD_DESEL	Reserved			
Default	'0'	'0'	'0'	'0'	'0110'			

Reset Register C – 0x1C		
Setting	Bit 4	Description – FB_FD_DESEL
0	'0'	Feedback frequency detector is connected to the lock detector
1	'1'	Feedback frequency detector is disconnected from the lock detector
Setting	Bit 6	Description – DIV_SEL
0	'0'	FB Clock divided by 1
1	'1'	FB Clock divided by 2
Setting	Bit 7	Description – DIV2_DIS
0	'0'	Normal mode of operation
1	'1'	FB Div2 in reset
Setting	Bit 8	Description – FB_START_BYPASS

0	'0'	Normal mode of operation
1	'1'	FB Divider can be started with external REF_SEL (pin)
Setting	Bit 9	Description – DET_START_BYPASS
0	'0'	Normal mode of operation
1	'1'	FB Divider can be started with external NRESET (pin)

CLOCK Register D – 0x1D.

Clock Register D – 0x1D								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved							
Default	'01101000'							
0	Reserved							
Default	'00000000'							

CLOCK Register E – 0x1E.

Clock Register E – 0x1E								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved						ADLOCK	LOCK_C[1]
Default	'000000'						'0'	'0'
0	LOCK_C[0]	Reserved	LOCK_WINDOW		Reserved			
Default	'0'	'0'	'00'		'0111'			

Reset Register E – 0x1E		
Setting	Bit 5:4	Description – Lock detect window – LOCK_WINDOW
0	'0'	
1	'1'	
Setting	Bit 8:7	Description – Number of coherent lock events – LOCK_C
0	'0'	
1	'1'	
Setting	Bit 9	Description ADLOCK
0	'0'	Digital PLL Lock
1	'1'	Analog PLL Lock

CLOCK Register F – 0x1F.

Clock Register F – 0x1F								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved							

Default	'01101000'
0	Reserved
Default	'00000000'

CLOCK Register 10 – 0x20.

Clock Register 10 – 0x20								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved							
Default	'00000001'							
0	Reserved				Reserved			
Default	'0111'				'1000'			

CLOCK Register 11 – 0x21.

Clock Register 11 – 0x21								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved							
Default	'01101000'							
0	Reserved				Reserved			
Default	'0000'				'0000'			

CLOCK Register 12 – 0x22.

Clock Register 12 – 0x22								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	INDET_BP	START_BYPASS	DIVSYNC_DIS	Reserved	LOCKW		HOLD_CNT	
Default	'0'	'0'	'0'	'0'	'00'		'00'	
0	Reserved	HOLD	Reserved	HOLDF	Reserved			
Default	'0'	'0'	'0'	'0'	'1001'			

Reset Register 12 – 0x22		
Setting	Bit 4	Description – Frequency Hold Over (External) enable – HOLDF
0	'0'	Off
1	'1'	On
Setting	Bit 6	Description – equals to HOLD pin – HOLD
0	'0'	Tri-state charge pump
1	'1'	
Setting	Bit 6	Description – equals to HOLD pin – HOLD
0	'0'	Tri-state charge pump
1	'1'	

Setting	Bit 9:8	Description – Hold function reactivates after a number of reference clock cycles - HOLD_CNT
0	'00'	64 clock cycles
1	'01'	128 clock cycles
2	'10'	256 clock cycles
3	'11'	512 clock cycles
Setting	Bit 11:10	Description – Extended lock detect window - LOCKW
0	'00'	
1	'01'	
2	'10'	
3	'11'	
Setting	Bit 13	Description – DIVSYNC_DIS
0	'0'	Start signal is synchronised to N/M divider input clock
1	'1'	
Setting	Bit 14	Description – START_BYPASS
0	'0'	Start signal is synchronised to VCXO clock
1	'1'	Start synch block is bypassed
Setting	Bit 15	Description – INDET_BP
0	'0'	Synch logic active when VCXO/AUX clocks are available
1	'1'	Synch logic is independent from VCXO/AUX

CLOCK Register 13 – 0x23.

Clock Register 13 – 0x23									
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	Reserved								
Default	'00000000'								
0	Reserved			BIAS_DIV_FB		NPRESET_MDIV	LOW_FD_FB_EN	PLL_LOCK_BP	
Default	'000'			'00'		'0'	'0'	'0'	

Reset Register 13 – 0x23		
Setting	Bit	Description
Setting	Bit 0	Description – PLL_LOCK_BP
0	'0'	Synch logic waits for the first PLL lock state
1	'1'	Synch logic independent from first PLL lock state
Setting	Bit 1	Description – LOW_FD_FB_EN
0	'0'	Synch logic is independent from VCXO/DIV_FB frequency
1	'1'	Synch logic is started for VCXO/DIV_FB > 600khz
Setting	Bit 2	Description – NPRESET_MDIV
0	'0'	M-divider uses nHOLD as NPRESET
1	'1'	M-divider not preset by nHOLD
Setting	Bit 4:3	Description – BIAS_DIV_FB
0	'00'	No current reduction
1	'01'	20% current reduction

2	'10'	30% current reduction
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CLOCK Register 14 – 0x24.

Clock Register 14 – 0x24								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reference Divider[11:4]							
Default	'00000000'							
0	Reference Divider M[3:0]				Reserved			
Default	'0000'				'1010'			

Reset Register 14 – 0x24		
Setting	Bit 11:4	Description – Reference Divider M[11:0]
0		
1		

CLOCK Register 15 – 0x25.

Clock Register 15 – 0x25								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	VCXO Divider N[13:6]							
Default	'000000'							
0	VCXO Divider N[5:0]					Reference Divider M[13:12]		
Default	'000000'					'00'		

Reset Register 15 – 0x25		
Setting	Bit 1:0	Description – Reference Divider M[13:12]
0		
1		
Setting	Bit 15:2	Description – VCXO Divider N[13:0]
0		
1		

CLOCK Register 16 – 0x26.

Clock Register 16 – 0x26								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	FB_COUNTER							FB_INCLK_I NV
Default	'00000000'							'0'
0	FB_CML_SE L	FB_DIS	SEC_DIV2	PRI_DIV2	Reserved			

Default	'0'	'0'	'0'	'0'	'1011'
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Reset Register 16 – 0x26		
Setting	Bit 4	Description – PRI_DIV2
0	'0'	Primary reference divider disabled
1	'1'	Primary reference divider enabled
Setting	Bit 5	Description – SEC_DIV2
0	'0'	Secondary reference divider disabled
1	'1'	Secondary reference divider enabled
Setting	Bit 6	Description – FB_DIS
0	'0'	FB Divider is active
1	'1'	FB Divider is disabled
Setting	Bit 7	Description – FB_CML_SEL
0	'0'	FB is CMOS type
1	'1'	FB is CML type
Setting	Bit 8	Description – FB_INCLK_INV
0	'0'	Input clock for FB not inverted (normal/low speed mode)
1	'1'	Input for FB inverted (high speed mode)
Setting	Bit 15:9	Description – FB_COUNTER
0	'0'	FB Path integer counter
1		

CLOCK Register 17 – 0x27.

Clock Register 17 – 0x27								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1				RESET_HO LD	SEL_DELA Y	RESHAPE	Reserved	OUT_MUX_S EL
Default				'0'	'0'	'0'	'0'	'0'
0	FB_MUX_S EL	PD_PLL	FB_PHASE_ADJ					
Default	'0'	'0'	'000000'					

Reset Register 17 – 0x27		
Setting	Bit 5:0	Description – FB_PHASE_ADJ
0	'0'	Feedback phase adjustment
Setting	Bit 6	Description – PD_PLL
0	'0'	PLL in normal mode
1	'1'	PLL powered down
Setting	Bit 7	Description – FB_MUX_SEL
0	'0'	VCXO selected for clock tree and FB
1	'1'	External Clock selected for clock tree and FB
Setting	Bit 8	Description – OUT_MUX_SEL

0	'0'	VCXO selected
1	'1'	External clock selected
Setting	Bit 10	Description – RESHAPE
0	'0'	Reference clock reshaped
1	'1'	Reference clock not reshaped
Setting	Bit 11	Description – SEL_DELAY
0	'0'	Enables short delay for fast operation
1	'1'	Long delay – recommended for reference below 150mhz.
Setting	Bit 12	Description – RESET_HOLD
0	'0'	RESET or HOLD acts as nRESET pin
1	'1'	RESET or HOLD acts as nHOLD pin

CLOCK Register 18 – 0x28.

Clock Register 18 – 0x28								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved			nRESET_nHOLD	nPD	Reserved		
Default	'000'			'0'	'1'	'000'		
0	Reserved				Reserved			
Default	'0000'				'1100'			

Reset Register 18 – 0x28		
Setting	Bit 11	Description – nPD
0	'0'	Power-down mode active
1	'1'	Normal mode of operation
Setting	Bit 12	Description – nRESET_nHOLD
0	'0'	Forces RESET or HOLD
1	'1'	Normal mode of operation

CLOCK Register 19 – 0x29.

Clock Register 19 – 0x29								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1								
Default								
0								
Default								

Reset Register 19 – 0x29		
Setting	Bit 11	Description – nPD
0		

1		
Setting	Bit 12	Description – nRESET_nHOLD
0		
1		

DAC Status

DAC Chab Register 0 – 0x30		
Setting	Bit 1:0	Description - Version
0	0	Read-only - Returns '00' for DAC5688
Setting	Bit 4:2	Description – Divice ID
0	0	Read Only - returns '000' for DAC5688
Setting	Bit 7	Description – PLL Lock Status
0	0	Read-only - PLL not locked.
1	1	Read-Only - PLL locked.

DAC Chab Register 0 – 0x30.

DAC Chab Register 0 – 0x30								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved	Clk1_in_ena	Clk1c_in_ena	Reserved	Fir4_en	qmc_offset_ena	qmc_corr_ena	mixer_ena
Default	'1'	'1'	'1'	'0'	'0'	'0'	'0'	'0'
0	inset_mode		Reserved	Synchr_clkin	Twos	inv_clk	interp_value	
Default	'00'		'0'	'0'	'0'	'0'	'00'	

DAC Chab Register 0 – 0x30		
Setting	Bit 1:0	Description – interpolation value
0	00	1x.
1	01	2x.
2	10	4x.
3	11	8x.
Setting	Bit 2	Description – inv_clk
0	0	Input clock not inverted.
1	1	Input clock inverted.
Setting	Bit 2	Description – twos
0	0	Binary format
1	1	Two's complement format.

Setting	Bit 2	Description – synchr_clkln
0	0	Synchronous mode off.
1	1	Synchronous mode on. Clk1 and Clk2 must synchronous in phase and frequency when reaching the DAC
Setting	Bit 7:6	Description – insel mode
0	00	Normal input on Port A and Port B.
1	01	Interleaved input on Port A.
2	10	Interleaved input on Port B.
3	11	Half rate on Port A and B.
Setting	Bit 8	Description – mixer_ena
0	0	Mixer bypassed.
1	1	Mixer enabled.
Setting	Bit 9	Description – qmc_corr_ena
0	0	QMC phase and gain correction bypasses.
1	1	QNC phase and gain correction enabled.
Setting	Bit 10	Description – qmc_offset_ena
0	0	QMC offset correction bypasses.
1	1	QNC offset correction enabled.
Setting	Bit 11	Description – fir4_ena
0	0	Filter bypassed.
1	1	FIR4 Inverse Sinc filter enabled.
Setting	Bit 13	Description – clk1c_in_ena
0	0	Pin used as PLL_LOCK status output.
1	1	Pin used as a clock input.
Setting	Bit 14	Description – clk1_in_ena
0	0	Pin used as CLK0 clock output.
1	1	Pin used as a clock input.

DAC Chab Register 1 – 0x31.

DAC Chab Register 1 – 0x31								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Ser_dac_data_ena	Output delay		b_equals_a	A_equals_b	reserved	revb	reva
Default	'0'	'00'		'0'	'0'	'0'	'0'	'0'
0	Diffclk_dly		Clk0_dly		Reserved			
Default	'00'		'00'		'0000'			

DAC Chab Register 1 – 0x31		
Setting	Bit 5:4	Description – clk0_dly
0	00	0ns delay.
1	01	1ns delay.

2	10	2ns delay.
3	11	3ns delay.
Setting	Bit 7:6	Description – diffclk_dly
0	00	0ns delay.
1	01	1ns delay.
2	10	2ns delay.
3	11	3ns delay.
Setting	Bit 8	Description - reva
0	0	Normal mode.
1	1	PortA reversed.
Setting	Bit 9	Description – revb
0	0	Normal mode.
1	1	PortB reversed.
Setting	Bit 11	Description – a_equals_b
0	0	Normal mode.
1	1	DACA driven by DACB data.
Setting	Bit 12	Description – b_equals_a
0	0	Normal mode.
1	1	DACB driven by DACA data
Setting	Bit 14:13	Description - output_delay – delay the output to both DACs
0	0	0 clock cycles
1	1	1 clock cycles
2	2	2 clock cycles
3	3	3 clock cycles
Setting	Bit 15	Description – ser_dac_data_ena
0	0	Normal mode of operation.
1	1	Muxes ser_dac_data to both DACs.

DAC Chab Register 2 – 0x32.

DAC Chab Register 2 – 0x32								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Phase Offset [7:0]							
Default	‘00000000							
0	Sif4	Sif_sync_sig	Clkdiv_syn_c_ena	Clkdiv_syn_c_sel	Reserved	Clkdiv_shift	Mixer gain	Reserved
Default	‘0’	‘0’	‘1’	‘0’	‘0’	‘0’	‘1’	‘0’

DAC Chab Register 2 – 0x32		
Setting	Bit 1	Description – Mixer gain
0	0	Nothing added.

1	1	Adds 6dbs to the mixer gain output.
Setting	Bit 2	Description – clkdiv shift
0	0	
1	1	A rising edge on the selected sync for the clock dividers will cause a slip in the synchronous counter by one period (used for multi DAC time alignment).
Setting	Bit 4	Description – clkdiv sync sel
0	0	SYNC selected as input to sync clock dividers
1	1	TXENABLE selected as input to sync clock dividers
Setting	Bit 5	Description – clkdiv sync ena
0	0	
1	1	Enables syncing of the clock divider using the sync or TXENABLE pins
Setting	Bit 6	Description – sif sync sig
0	0	Clears sync
1	1	Causes a sync
Setting	Bit 7	Description – sif4
0	0	3-bit serial interface
1	1	4-bit serial interface
Setting	Bit 15:8	Description – Phase Offset[7:0]
0	0	

DAC Chab Register 3 – 0x33.

DAC Chab Register 3 – 0x33								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Phase add [7:0]							
Default	'00000000							
0	Phase Offset [15:8]							
Default	'00000000							

DAC Chab Register 3 – 0x33		
Setting	Bit 7:0	Description – Phase Offset[15:8]
0	0	
Setting	Bit 15:8	Description – Phase add[7:0]
0	0	

DAC Chab Register 4 – 0x34.

DAC Chab Register 4 – 0x34								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Phase add [23:16]							
Default	'00000000							

0	Phase add [15:8]
Default	'00000000

DAC Chab Register 4 – 0x34		
Setting	Bit 15:0	Description – Phase add[23:8]
0	0	

DAC Chab Register 5 – 0x35.

DAC Chab Register 5 – 0x35								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Qmc gain a[7:0]							
Default	'00000000							
0	Phase add [31:24]							
Default	'00000000							

DAC Chab Register 5 – 0x35		
Setting	Bit 7:0	Description – Phase add[31:24]
0	0	
Setting	Bit 15:8	Description – QMC gain a[7:0]
0	0	

DAC Chab Register 6 – 0x36.

DAC Chab Register 6 – 0x36								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Qmc phase[7:0]							
Default	'00000000							
0	Qmc gain b [7:0]							
Default	'00000000							

DAC Chab Register 6 – 0x36		
Setting	Bit 7:0	Description – QMC gain b[7:0]
0	0	
Setting	Bit 15:8	Description – QMC Phase[7:0]
0	0	

DAC Chab Register 7 – 0x37.

DAC Chab Register 7 – 0x37									
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	Qmc offset a [7:0]								
Default	'00000000								
0	Qmc Phase[9:8]		Qmc gain a[10:8]			Qmc gain b[10:8]			
Default	'00'		'100'			'100'			

DAC Chab Register 7 – 0x37		
Setting	Bit 15:8	Description – QMC offset a[7:0]
0	0	
Setting	Bit 2:0	Description – QMC gain b[10:8]
0	0	
Setting	Bit 5:3	Description – QMC gain a[10:8]
0	0	
Setting	Bit 7:6	Description – QMC Phase[9:8]
0	0	

DAC Chab Register 8 – 0x38.

DAC Chab Register 8 – 0x38									
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	Qmc offset a[12:8]					Reserved			
Default	'00000'					'000'			
0	Qmc offset b [7:0]								
Default	'00000000								

DAC Chab Register 8 – 0x38		
Setting	Bit 7:0	Description – QMC offset b[7:0]
0	0	
Setting	Bit 15:11	Description – QMC offset a[12:8]
0	0	

DAC Chab Register 9 – 0x39.

DAC Chab Register 9 – 0x39									
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	Ser_dac_data[7:0]								
Default	'00000000'								
0	Qmc offset b[12:8]					Reserved			
Default	'00000'					'000'			

DAC Chab Register 9 – 0x39		
Setting	Bit 7:3	Description – QMC offset b[12:8]
0	0	
Setting	Bit 15:8	Description Ser_dac_data[7:0]
0	0	

DAC Chab Register A – 0x3A.

DAC Chab Register A – 0x3A								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Nco_sel		Nco_reg_sel		Qmcorr_reg_sel		Qmoffset_reg_sel	
Default	'00'		'01'		'01'		'01'	
0	Ser_dac_data[15:8]							
Default	'00000000'							

DAC Chab Register A – 0x3A		
Setting	Bit 7:0	Description Ser_dac_data[7:0]
0	0	
Setting	Bit 9:8	Description qmoffset_reg_sel – selects sync for loading the QM offset register
0	'00'	TXENABLE from FIFO output
0	'01'	SYNC from FIFO output
1	'10'	Sync_sif_sig
1	'11'	Always 0
Setting	Bit 11:10	Description qmcorr_reg_sel – selects sync for loading the QM correction register
0	'00'	TXENABLE from FIFO output
0	'01'	SYNC from FIFO output
1	'10'	Sync_sif_sig
1	'11'	Always 0
Setting	Bit 13:12	Description nco_reg_sel – selects sync for loading the NCO register
0	'00'	TXENABLE from FIFO output
0	'01'	SYNC from FIFO output
1	'10'	Sync_sif_sig
1	'11'	Always 0
Setting	Bit 15:14	Description nco_sel – selects sync for loading the NCO accumulator
0	'00'	TXENABLE from FIFO output
0	'01'	SYNC from FIFO output
1	'10'	Sync_sif_sig
1	'11'	Always 0

DAC Chab Register B – 0x3B.

DAC Chab Register B – 0x3B								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Fifo_sync_strt				Reserved			
Default	'1000'				'0000'			
0	Reserved		Fifo_sel			Aflag_sel	Reserved	
Default	'00'		'010'			'1'	'00'	

DAC Chab Register B – 0x3B		
Setting	Bit 2	Description aflag_sel
0	'0'	The rising edge of TXENABLE is used to determine the A sample.
0	'1'	The MSB of the input opposite of incoming data is used to determine the A sample.
Setting	Bit 15:12	Description fifo_sync_strt
0		When the sync fifo to the fifo occurs, this is the values loaded into the fifo output counter.

DAC Chab Register C – 0x3C.

DAC Chab Register C – 0x3C								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Io_1p8_3p3	Reserved	sleepb	sleepa	isbiaslpf_b_a	isbiaslpf_b	PLL_sleep	PLL_ena
Default	'0'	'0'	'0'	'0'	'1'	'1'	'0'	'1'
0	Reserved							
Default	'00000000'							

DAC Chab Register C – 0x3C		
Setting	Bit 8	Description pll_ena
0	'0'	PLL is off.
1	'1'	PLL is on and its output clock is used to clock the DAC.
Setting	Bit 9	Description pll_sleep
0	'0'	PLL is not in sleep mode.
1	'1'	PLL is in sleep mode.
Setting	Bit 10	Description isbiaslpf_b
0	'0'	Low pass filter for the current source bias in DACB is off.
1	'1'	Low pass filter for the current source bias in DACB is on. The low pass filter will set a corner at 472Hz when low and 95KHz when high
Setting	Bit 11	Description isbiaslpf_a
0	'0'	Low pass filter for the current source bias in DACA is off.
1	'1'	Low pass filter for the current source bias in DACA is on. The low pass filter will set a corner at 472Hz when low and 95KHz when high

Setting	Bit 12	Description sleepa
0	'0'	DACA not in sleep mode.
1	'1'	DACA in sleep mode.
Setting	Bit 13	Description sleepb
0	'0'	DACB not in sleep mode.
1	'1'	DACB in sleep mode.
Setting	Bit 15	Description io_1p8_3p3
0	'0'	3.3V tolerate pads
1	'1'	1.8V tolerate pads

DAC Chab Register D – 0x3D.

DAC Chab Register D – 0x3D								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved							
Default	'00000000'							
0	Coarse_daca				Coarse_dacb			
Default	'1111'				'1111'			

DAC Chab Register D – 0x3D		
Setting	Bit 3:0	Description Coarse_dacb
0		DACB Output current scale.
Setting	Bit 7:4	Description Coarse_daca
0		DACA Output current scale.

DAC Chab Register D – 0x3D.

DAC Chab Register D – 0x3D								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved							
Default	'00000000'							
0	Coarse_daca				Coarse_dacb			
Default	'1111'				'1111'			

DAC Chab Register D – 0x3D		
Setting	Bit 3:0	Description Coarse_dacb
0		DACB Output current scale.
Setting	Bit 7:4	Description Coarse_daca

0	DACA Output current scale.
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DAC Chab Register E – 0x3E.

DAC Chab Register E – 0x3E								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	PLL_lpf_r reset	Vco_div2	PLL_gain		PLL_range			
Default	'0'	'0'	'00'		'0000'			
0	PLL_m				PLL_n			
Default	'00000'				'000'			

DAC Chab Register E – 0x3E		
Setting	Bit 2:0	Description - pll_n
0	'000'	n value=1.
1	'001'	n value=2.
2	'011'	n value=4.
3	'111'	n value=8.
Setting	Bit 7:3	Description - pll_m
0	'00000'	m value=1.
1	'00001'	m value=2.
2	'00011'	m value=4.
3	'00111'	m value=8.
4	'01111'	m value=16.
5	'11111'	m value=32.
Setting	Bit 11:8	Description - pll_range - to adjust the vco current
0	'0000'	Minimum bias current and lowest VCO frequency range.
1	'1111'	Maximum bias current and highest VCO frequency range.
Setting	Bit 13:12	Description - pll_gain - to adjust the vco gain (Kvco)
0	'00'	
1	'01'	
2	'10'	
3	'11'	
Setting	Bit 14	Description - vco_div2
0	'0'	PLL clock output is not divided.
1	'1'	PLL clock output is divided by 2.
Setting	Bit 15	Description - pll_lpf_reset
0	'0'	
1	'1'	Holds the pll loop filter at 0 volts

DAC Chab Register 0 – 0x40.

DAC Chab Register 0 – 0x40								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved	Clk1_in_ena	Clk1c_in_ena	Reserved	Fir4_en	qmc_offset_ena	qmc_corr_ena	mixer_ena
Default	'1'	'1'	'1'	'0'	'0'	'0'	'0'	'0'
0	inset_mode		Reserved	Synchr_clkln	Twos	inv_clk	interp_value	
Default	'00'		'0'	'0'	'0'	'0'	'00'	

DAC Chab Register 0 – 0x40		
Setting	Bit 1:0	Description – interpolation value
0	00	1x.
1	01	2x.
2	10	4x.
3	11	8x.
Setting	Bit 2	Description – inv_clk
0	0	Input clock not inverted.
1	1	Input clock inverted.
Setting	Bit 2	Description – twos
0	0	Binary format
1	1	Two's complement format.
Setting	Bit 2	Description – synchr_clkln
0	0	Synchronous mode off.
1	1	Synchronous mode on. Clk1 and Clk2 must synchronous in phase and frequency when reaching the DAC
Setting	Bit 7:6	Description – inset mode
0	00	Normal input on Port A and Port B.
1	01	Interleaved input on Port A.
2	10	Interleaved input on Port B.
3	11	Half rate on Port A and B.
Setting	Bit 8	Description – mixer_ena
0	0	Mixer bypassed.
1	1	Mixer enabled.
Setting	Bit 9	Description – qmc_corr_ena
0	0	QMC phase and gain correction bypasses.
1	1	QNC phase and gain correction enabled.
Setting	Bit 10	Description – qmc_offset_ena
0	0	QMC offset correction bypasses.
1	1	QNC offset correction enabled.
Setting	Bit 11	Description – fir4_ena
0	0	Filter bypassed.
1	1	FIR4 Inverse Sinc filter enabled.

Setting	Bit 13	Description – clk1c_in_ena
0	0	Pin used as PLL_LOCK status output.
1	1	Pin used as a clock input.
Setting	Bit 14	Description – clk1_in_ena
0	0	Pin used as CLK0 clock output.
1	1	Pin used as a clock input.

DAC Chab Register 1 – 0x41.

DAC Chab Register 1 – 0x41								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Ser_dac_data_ena	Output delay		b_equals_a	A_equals_b	reserved	revb	reva
Default	'0'	'00'		'0'	'0'	'0'	'0'	'0'
0	Diffclk_dly		Clk0_dly		Reserved			
Default	'00'		'00'		'0000'			

DAC Chab Register 1 – 0x41		
Setting	Bit 5:4	Description – clk0_dly
0	00	0ns delay.
1	01	1ns delay.
2	10	2ns delay.
3	11	3ns delay.
Setting	Bit 7:6	Description – diffclk_dly
0	00	0ns delay.
1	01	1ns delay.
2	10	2ns delay.
3	11	3ns delay.
Setting	Bit 8	Description - reva
0	0	Normal mode.
1	1	PortA reversed.
Setting	Bit 9	Description – revb
0	0	Normal mode.
1	1	PortB reversed.
Setting	Bit 11	Description – a_equals_b
0	0	Normal mode.
1	1	DACA driven by DACB data.
Setting	Bit 12	Description – b_equals_a
0	0	Normal mode.
1	1	DACB driven by DACA data
Setting	Bit 14:13	Description - output_delay – delay the output to both DACs
0	0	0 clock cycles

1	1	1 clock cycles
2	2	2 clock cycles
3	3	3 clock cycles
Setting	Bit 15	Description – ser_dac_data_ena
0	0	Normal mode of operation.
1	1	Muxes ser_dac_data to both DACs.

DAC Chab Register 2 – 0x42.

DAC Chab Register 2 – 0x42								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Phase Offset [7:0]							
Default	‘00000000							
0	Sif4	Sif_sync_sig	Clkdiv_sync_ena	Clkdiv_sync_sel	Reserve d	Clkdiv_shift	Mixer gain	Reserved
Default	‘0’	‘0’	‘1’	‘0’	‘0’	‘0’	‘1’	‘0’

DAC Chab Register 2 – 0x42		
Setting	Bit 1	Description – Mixer gain
0	0	Nothing added.
1	1	Adds 6dbs to the mixer gain output.
Setting	Bit 2	Description – clkdiv shift
0	0	
1	1	A rising edge on the selected sync for the clock dividers will cause a slip in the synchronous counter by one period (used for multi DAC time alignment).
Setting	Bit 4	Description – clkdiv sync sel
0	0	SYNC selected as input to sync clock dividers
1	1	TXENABLE selected as input to sync clock dividers
Setting	Bit 5	Description – clkdiv sync ena
0	0	
1	1	Enables syncing of the clock divider using the sync or TXENABLE pins
Setting	Bit 6	Description – sif sync sig
0	0	Clears sync
1	1	Causes a sync
Setting	Bit 7	Description – sif4
0	0	3-bit serial interface
1	1	4-bit serial interface
Setting	Bit 15:8	Description – Phase Offset[7:0]
0	0	

DAC Chab Register 3 – 0x43.

DAC Chab Register 3 – 0x43								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Phase add [7:0]							
Default	'00000000							
0	Phase Offset [15:8]							
Default	'00000000							

DAC Chab Register 3 – 0x43		
Setting	Bit 7:0	Description – Phase Offset[15:8]
0	0	
Setting	Bit 15:8	Description – Phase add[7:0]
0	0	

DAC Chab Register 4 – 0x44.

DAC Chab Register 4 – 0x44								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Phase add [23:16]							
Default	'00000000							
0	Phase add [15:8]							
Default	'00000000							

DAC Chab Register 4 – 0x44		
Setting	Bit 15:0	Description – Phase add[23:8]
0	0	

DAC Chab Register 5 – 0x45.

DAC Chab Register 5 – 0x45								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Qmc gain a[7:0]							
Default	'00000000							
0	Phase add [31:24]							
Default	'00000000							

DAC Chab Register 5 – 0x45		
Setting	Bit 7:0	Description – Phase add[31:24]

0	0	
Setting	Bit 15:8	Description – QMC gain a[7:0]
0	0	

DAC Chab Register 6 – 0x46.

DAC Chab Register 6 – 0x46								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Qmc phase[7:0]							
Default	'00000000							
0	Qmc gain b [7:0]							
Default	'00000000							

DAC Chab Register 6 – 0x46		
Setting	Bit 7:0	Description – QMC gain b[7:0]
0	0	
Setting	Bit 15:8	Description – QMC Phase[7:0]
0	0	

DAC Chab Register 7 – 0x47.

DAC Chab Register 7 – 0x47								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Qmc offset a [7:0]							
Default	'00000000							
0	Qmc Phase[9:8]		Qmc gain a[10:8]			Qmc gain b[10:8]		
Default	'00'		'100'			'100'		

DAC Chab Register 7 – 0x47		
Setting	Bit 15:8	Description – QMC offset a[7:0]
0	0	
Setting	Bit 2:0	Description – QMC gain b[10:8]
0	0	
Setting	Bit 5:3	Description – QMC gain a[10:8]
0	0	
Setting	Bit 7:6	Description – QMC Phase[9:8]
0	0	

DAC Chab Register 8 – 0x48.

DAC Chab Register 8 – 0x48								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Qmc offset a[12:8]					Reserved		
Default	'00000'					'000'		
0	Qmc offset b [7:0]							
Default	'00000000							

DAC Chab Register 8 – 0x48		
Setting	Bit 7:0	Description – QMC offset b[7:0]
0	0	
Setting	Bit 15:11	Description – QMC offset a[12:8]
0	0	

DAC Chab Register 9 – 0x49.

DAC Chab Register 9 – 0x49								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Ser_dac_data[7:0]							
Default	'00000000'							
0	Qmc offset b[12:8]					Reserved		
Default	'00000'					'000'		

DAC Chab Register 9 – 0x49		
Setting	Bit 7:3	Description – QMC offset b[12:8]
0	0	
Setting	Bit 15:8	Description Ser_dac_data[7:0]
0	0	

DAC Chab Register A – 0x4A.

DAC Chab Register A – 0x4A								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Nco_sel		Nco_reg_sel		Qmcorr_reg_sel		Qmoffset_reg_sel	
Default	'00'		'01'		'01'		'01'	
0	Ser_dac_data[15:8]							
Default	'00000000'							

DAC Chab Register A – 0x4A		
Setting	Bit 7:0	Description Ser_dac_data[7:0]
0	0	
Setting	Bit 9:8	Description qmoffset_reg_sel – selects sync for loading the QM offset register
0	'00'	TXENABLE from FIFO output
0	'01'	SYNC from FIFO output
1	'10'	Sync_sif_sig
1	'11'	Always 0
Setting	Bit 11:10	Description qmcorr_reg_sel – selects sync for loading the QM correction register
0	'00'	TXENABLE from FIFO output
0	'01'	SYNC from FIFO output
1	'10'	Sync_sif_sig
1	'11'	Always 0
Setting	Bit 13:12	Description nco_reg_sel – selects sync for loading the NCO register
0	'00'	TXENABLE from FIFO output
0	'01'	SYNC from FIFO output
1	'10'	Sync_sif_sig
1	'11'	Always 0
Setting	Bit 15:14	Description nco_sel – selects sync for loading the NCO accumulator
0	'00'	TXENABLE from FIFO output
0	'01'	SYNC from FIFO output
1	'10'	Sync_sif_sig
1	'11'	Always 0

DAC Chab Register B – 0x4B.

DAC Chab Register B – 0x4B								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Fifo_sync_strt				Reserved			
Default	'1000'				'0000'			
0	Reserved		Fifo_sel			Aflag_sel	Reserved	
Default	'00'		'010'			'1'	'00'	

DAC Chab Register B – 0x4B		
Setting	Bit 2	Description aflag_sel
0	'0'	The rising edge of TXENABLE is used to determine the A sample.
0	'1'	The MSB of the inputopposite of incoming data is used to determine the A sample.
Setting	Bit 15:12	Description fifo_sync_strt
0		When the sync fifo to the fifo occurs, this is the values loaded into the fifo output counter.

DAC Chab Register C – 0x4C.

DAC Chab Register C – 0x4C								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Io_1p8_3p3	Reserved	sleepb	sleepa	isbiaslpfb_a	isbiaslpf_b	PLL_sleep	PLL_ena
Default	'0'	'0'	'0'	'0'	'1'	'1'	'0'	'1'
0	Reserved							
Default	'00000000'							

DAC Chab Register C – 0x4C		
Setting	Bit	Description
0	8	PLL is off.
1	8	PLL is on and its output clock is used to clock the DAC.
0	9	PLL is not in sleep mode.
1	9	PLL is in sleep mode.
0	10	Low pass filter for the current source bias in DACB is off.
1	10	Low pass filter for the current source bias in DACB is on. The low pass filter will set a corner at 472Hz when low and 95KHz when high
0	11	Low pass filter for the current source bias in DACA is off.
1	11	Low pass filter for the current source bias in DACA is on. The low pass filter will set a corner at 472Hz when low and 95KHz when high
0	12	DACA not in sleep mode.
1	12	DACA in sleep mode.
0	13	DACB not in sleep mode.
1	13	DACB in sleep mode.
0	15	3.3V tolerate pads
1	15	1.8V tolerate pads

DAC Chab Register D – 0x4D.

DAC Chab Register D – 0x4D								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved							
Default	'00000000'							

0	Coarse_daca	Coarse_dacb
Default	'1111'	'1111'

DAC Chab Register D – 0x4D		
Setting	Bit 3:0	Description Coarse_dacb
0		DACB Output current scale.
Setting	Bit 7:4	Description Coarse_daca
0		DACA Output current scale.

DAC Chab Register D – 0x4D.

DAC Chab Register D – 0x4D								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Reserved							
Default	'00000000'							
0	Coarse_daca				Coarse_dacb			
Default	'1111'				'1111'			

DAC Chab Register D – 0x4D		
Setting	Bit 3:0	Description Coarse_dacb
0		DACB Output current scale.
Setting	Bit 7:4	Description Coarse_daca
0		DACA Output current scale.

DAC Chab Register E – 0x4E.

DAC Chab Register E – 0x4E								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	PLL_lpf_r reset	Vco_div2	PLL_gain		PLL_range			
Default	'0'	'0'	'00'		'0000'			
0	PLL_m					PLL_n		
Default	'00000'					'000'		

DAC Chab Register E – 0x4E		
Setting	Bit 2:0	Description - pll_n
0	'000'	n value=1.
1	'001'	n value=2.
2	'011'	n value=4.

3	'111'	n value=8.
Setting	Bit 7:3	Description - pll_m
0	'00000'	m value=1.
1	'00001'	m value=2.
2	'00011'	m value=4.
3	'00111'	m value=8.
4	'01111'	m value=16.
5	'11111'	m value=32.
Setting	Bit 11:8	Description - pll_range - to adjust the vco current
0	'0000'	Minimum bias current and lowest VCO frequency range.
1	'1111'	Maximum bias current and highest VCO frequency range.
Setting	Bit 13:12	Description - pll_gain - to adjust the vco gain (Kvco)
0	'00'	
1	'01'	
2	'10'	
3	'11'	
Setting	Bit 14	Description - vco_div2
0	'0'	PLL clock output is not divided.
1	'1'	PLL clock output is divided by 2.
Setting	Bit 15	Description - pll_lpf_reset
0	'0'	
1	'1'	Holds the pll loop filter at 0 volts

4 Connectors

4.1 Description

The following table gathers all connectors on the board and describes their function.

Connector (silkscreen schematics)	name and	Description	Location on the board
J16		DACA Analog Output	Top / Left
J15		DACB Analog Output	Top / Left
J1016		DACC Analog Output	Top / Right
J1015		DACD Analog Output	Top / Right
J30		External Reference Input	Bottom / Right
J29		External Clock Input	Bottom / Left
J4		External Clock Output	Bottom / Left
J24		External Trigger	Bottom / Left

4.2 Location on the board

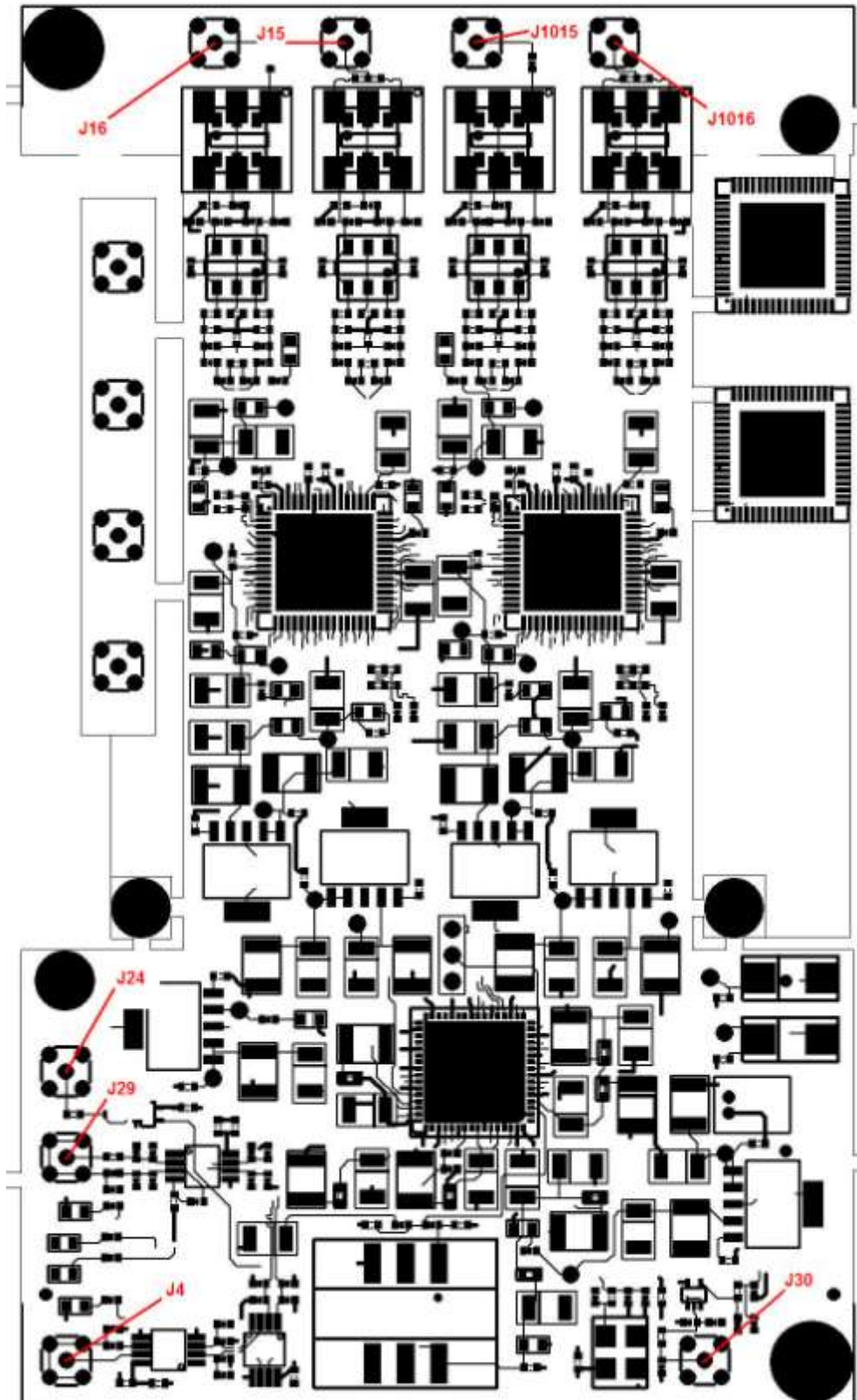


Figure 6 - Connectors

5 Footprint

5.1 Top View

5.2 Bottom View

6 Pinout

7 Support Packages

8 Physical Properties

Dimensions		
Weight		
Supply Voltages		
Supply Current	+12V	
	+5V	
	+3.3V	
	-5V	
	-12V	
MTBF		

9 Safety

This module presents no hazard to the user when in normal use.

10 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.