

Unit / Module Description:	Quad ADC/DAC SLB Mezzanine
Unit / Module Number:	SMT944
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Product Specification

for

SMT944

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Certificate Number FM 55022

Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	12/07/07	GKP
1.1	Updated board layout	17/7/07	GKP

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1 Introduction

The SMT944 is a single width expansion SLB mezzanine that plugs onto base TIM that incorporates an [SLB](#) (eg [SMT368](#)).

It uses a Texas Instruments Analog-to-Digital Converter ([ADS6455](#)) and 2 Texas Instruments dual-channel Digital-to-Analog Converters ([DAC5672](#)).

The SMT944 has a local 125MHz oscillator and an external clock input. These feed a multiplexer/buffer circuit, and are distributed to all ADC/DACs. A clock output signal is also present on an MMCX connector.

ADCs are 14-bit and can sample at up to 125 MHz. The DACs have a resolution of 14 bits and use the same clock source as the ADC. All converters are 3.3-Volt.

Controlling the ADC and DACs is performed by the base TIM. Typically this utilizes an Xilinx FPGA which includes interfaces to the ADC/DAC control, TIM ComPorts, and the SLB's data interfaces.

The main features of the *SMT944* are listed below:

- Quad 14-bit 125MSPS ADC ([ADS6445](#)),
- Quad 14-bit 125MSPS DAC (2 x [DAC5672](#)),
- On-board 125MHz clock,
- External clock and external triggers,
- [SLB](#) connector to link SMT944 to base TIM,
- Synchronisation signals,
- All Analogue inputs/outputs are 50- Ohm terminated.

2 Related Documents

[Sundance RSL specification](#) (hyperlink to: http://www.sundance.com/docs/Specification_RSL.pdf).

[Xilinx Virtex5 datasheets](#) (hyperlink to: http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?category=Data+Sheets/FPGA+Device+Families/Virtex-5).

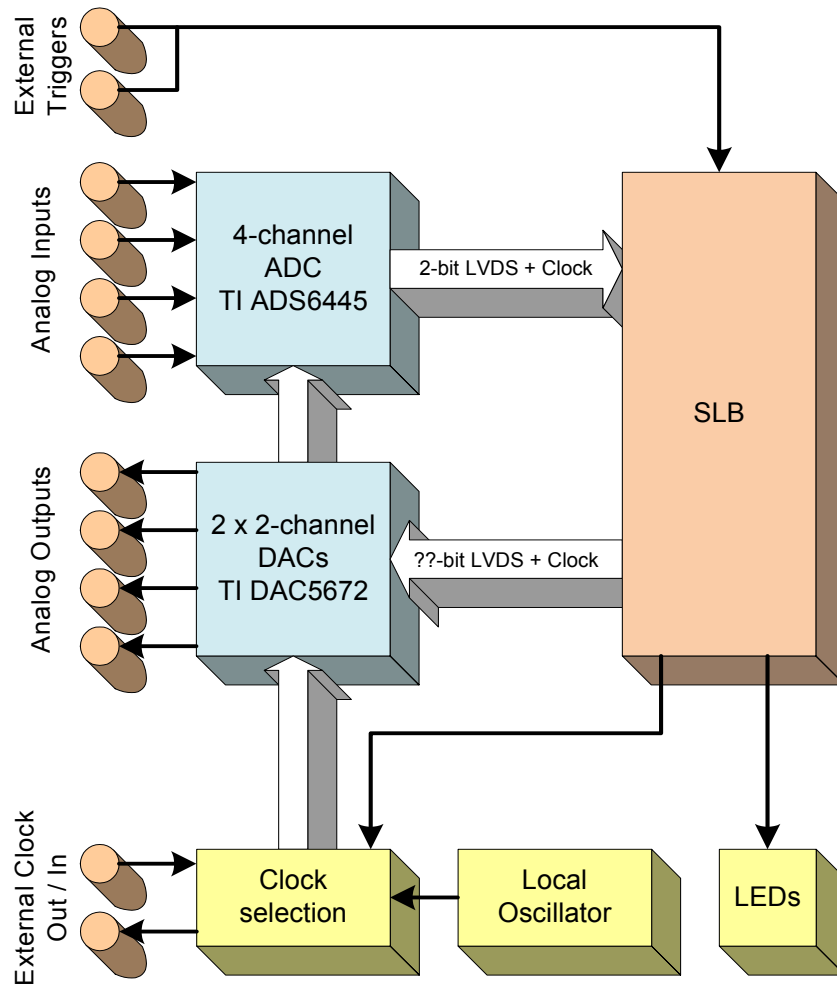
3 Acronyms, Abbreviations and Definitions

[A list of acronyms etc](#) (hyperlink to <http://www.sundance.com/web/files/static.asp?pagename=acc>).

4 Functional Description

The major elements of the SMT944 are shown in the block diagram below.

4.1 Block Diagram



4.2 Module Description

4.2.1 ADC

The ADC section uses an ADS6445 quad ADC from Texas Instruments.

This device outputs data on 2-bit LVDS buses. These are typically connected directly to an FPGA SERDES.

All inputs are terminated to 50 Ohms and can be ordered as AC coupled (utilizing back-to-back 1:1 transformers) or DC coupled (using [THS4509](#) wideband differential amplifiers).

4.2.2 DAC

Two Texas Instruments DAC5672 devices are used to provide 4 channels of output.

Each DAC channel is designed to drive 50 Ohm terminated load.

The output can be transformer coupled (AC coupling), or via an amplifier (DC coupled).

4.2.3 FPGA

The SMT944 typically interfaces to an FPGA on a TIM module. This FPGA is responsible for collecting serial data from the ADC and outputting parallel data to the DACs.

4.2.4 LEDs

Four LEDs are available and connected directly to the TIMs FPGA.

4.2.5 Clock Multiplexer Control

The clock multiplexer is directly controlled using an LV-TTL signal from the SLB interface.

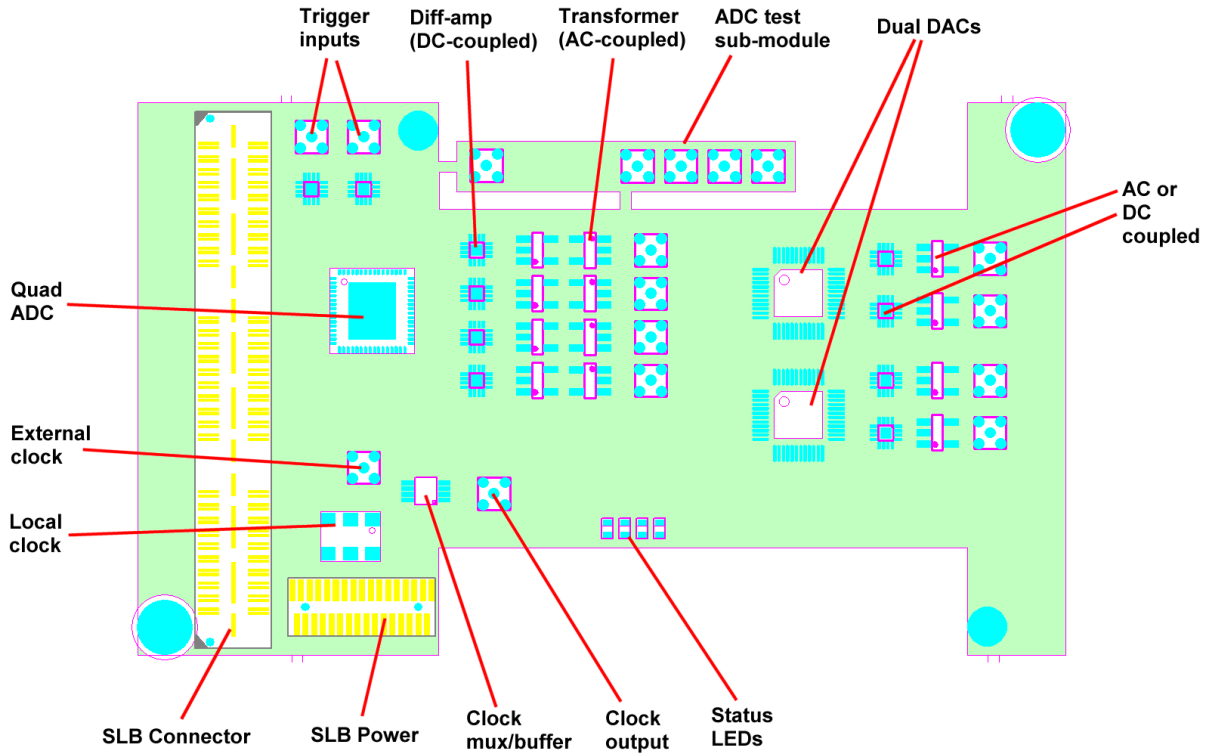
5 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

6 Circuit Description / Diagrams

7 Footprint

7.1 Top View



8 Support Packages

9 Physical Properties

Dimensions		
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Weight	
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Voltage	Current
+ 12V	0
+ 5V	0
+ 3.3V	1.2A
- 5V	0
- 12V	0

MTBF	
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10 Safety

This module presents no hazard to the user when in normal use.

11 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

12 Ordering Information

Variations of this product are available for AC and DC coupled inputs/outputs

Eg. SMT944- ac, or SMT944- dc