Unit / Module Description:	Quad 16-bit ADC/DAC SLB Mezzanine
Unit / Module Number:	SMT946
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Product Specification for SMT946

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Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	6-Feb-08	GKP
1.1	Update to SLB pin-out. Added IO connector.	26-Feb-06	GKP
1.2	Added drawing for uni/bi-polar output selection.	8-Apr-10	GKP

Table of Contents

1 Introduction / Description

The SMT946 (16 bit) is a single width expansion SLB mezzanine that plugs onto a base TIM that incorporates the SLB (eg SMT368, SMT111).

It uses 4 TI ADS8372 16-bit ADCs and 4 TI DAC8831 16-bit DACs. Input and output is via MMCX co-axial connectors.

All ADC and DAC channels sample simultaneously (no input multiplexers).

2 Related Documents

Xilinx Virtex5 datasheets:
http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?category=Data+Sheets/FPGA+Device+Families/Virtex-5

Sundance Local Bus (SLB) specification:
http://www.sundance.com/docs/SLB%20-%20Sundance%20Local%20Bus%20Specification.pdf

ADS8372 ADC
http://focus.ti.com/docs/prod/folders/print/ads8372.html

DAC8831 DAC
http://focus.ti.com/docs/prod/folders/print/dac8831.html

REF3025 voltage reference
http://focus.ti.com/docs/prod/folders/print/ref3025.html

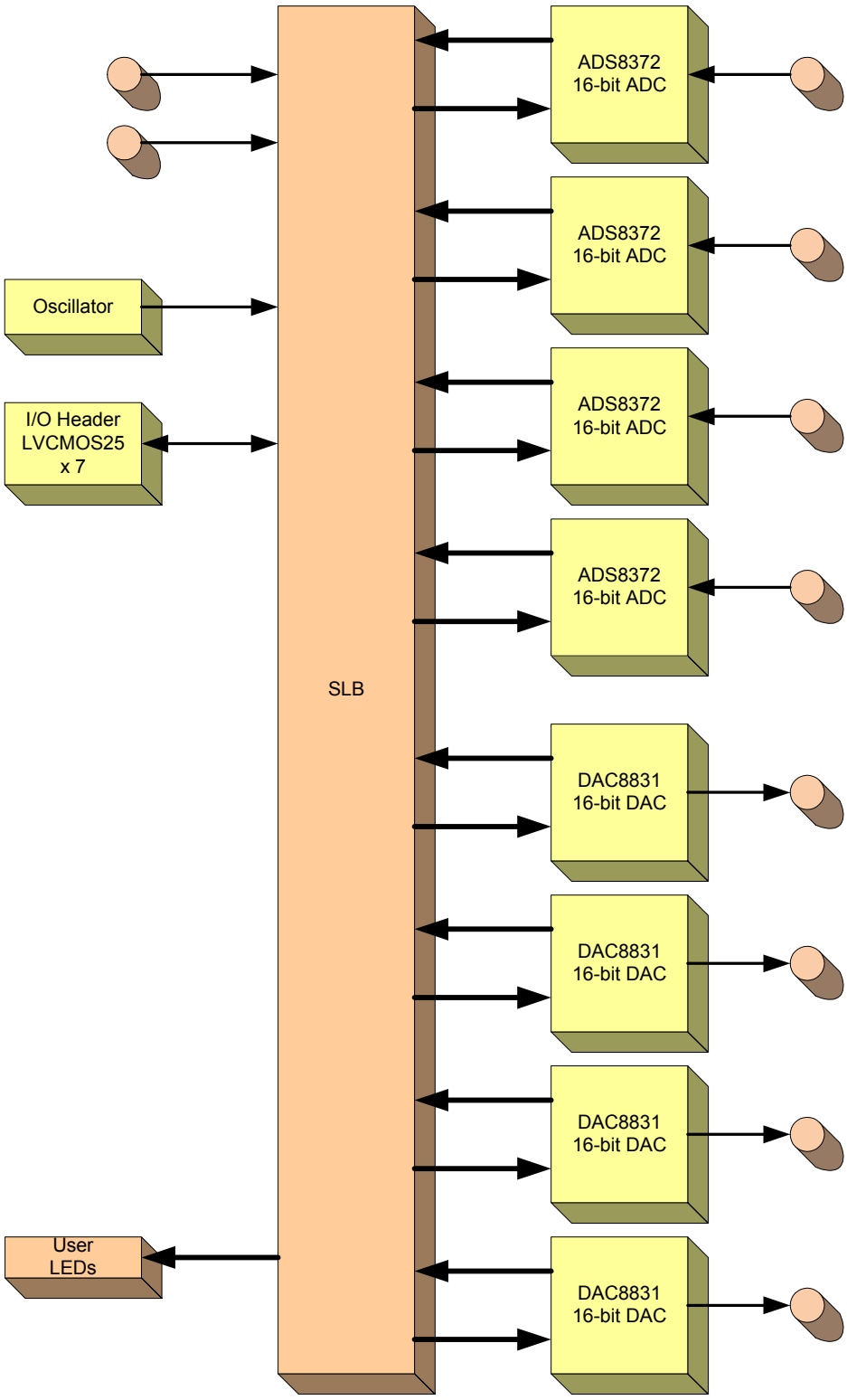
3 Acronyms, Abbreviations and Definitions

A list of acronyms etc: http://www.sundance.com/web/files/static.asp?pagename=acc

4 Functional Description

The major elements of the SMT946 are shown in the block diagram below.

4.1 Block Diagram



4.2 Module Description

4.2.1 SLB

The SMT946 typically interfaces to an FPGA on a TIM module. This FPGA is responsible for all communication to and from the ADCs and DACs.

The pin-out of this connector is compatible with the reduced set available on the SMT111.

4.2.2 ADC

The input to the ADC is via a unity gain single-ended to differential op-amp. The common mode voltage of this device can be adjusted using a potentiometer. The input range is defined by the voltage reference, and by default is +/-2V.

The ADC's reference voltage can be either supplied from its internal source or from an external REF3025 (2.5V) device. The external voltage reference is multiplied by 1.6 using an op-amp before entering the ADC. The default setting is for internal reference.

Each of the TI ADC8372 ADCs connect to the SLB using a serial interface.

The conversion time of the ADC is set internally in the device at 600kHz.
Conversions are started by the assertion of the ADC's CS and CONVST signals. These signals are common to all 4 ADCs.
At the end of conversion, a BUSY signal is returned to the SLB. Individual BUSY signals from each ADC are provided.
Data is read from the ADCs using a serial clock (common to all ADCs) and separate serial data signals.

4.2.3 DAC

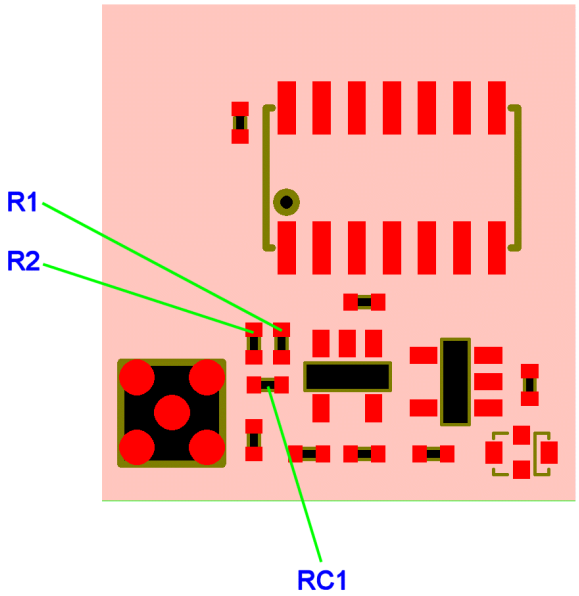
Each of the TI DAC8831 DACs connect to the SLB using a serial interface.

A serial data stream is clocked into each device using a common clock and independent data signals.
The DAC output registers are updated at the same time using the LDAC signal.

The DAC's output signal is buffered by an op-amp which results in an output voltage of +/-2.5V. Alternatively, the output can be switched (resistor jumper setting) to uni-polar mode.

An external 2.5V reference is used for the DACs.

The DAC components for each of the 4 channels are shown here:



For uni-polar operation, R1 and R2 should not be fitted. RC1 should be fitted as a 0 Ohm resistor link.
For bi-polar operation, R1 and R2 should be fitted as 0 Ohm resistor links, and RC1 should be a 5pF capacitor.

4.2.4 LEDs

Four LEDs are directly connected to the SLB connector.

4.2.5 Oscillator

An on-board oscillator connects to the SLB.

This device can be fitted with the exact frequency (or multiple of) required for the sample rate. Note that the SLB carrier's FPGA provides the ADC convert signal and the DAC update signal.

4.2.6 User MMCX Connectors

Two MMCX connectors are provided which connect to the SLB. These can carry an LVCMOS 2.5V signal to/from the SLB carrier's FPGA.

These could be used to provide an external sample clock or trigger type signal.

4.2.7 I/O Header

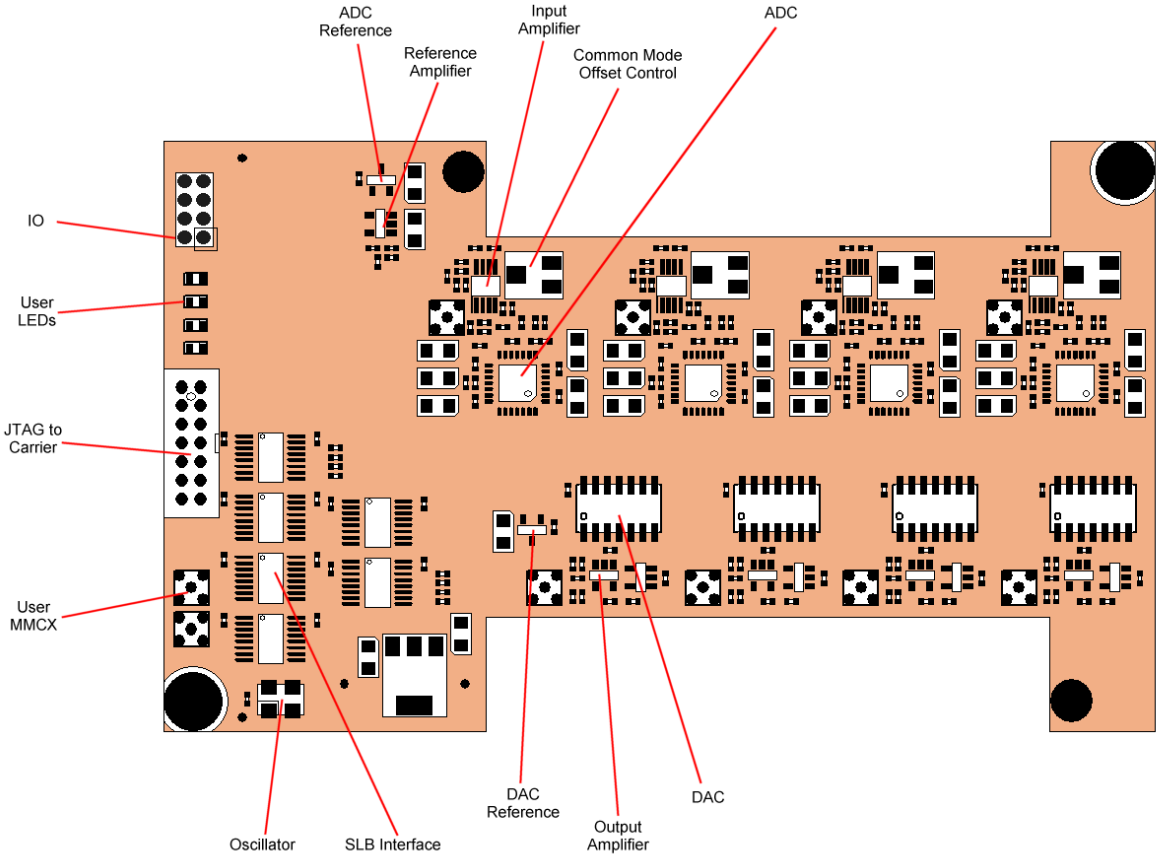
Seven 2.5V LVCMOS signals are available on a 2mm 4x2 pin-header.
These pins are connected directly to the SLB connector.

Pin	Signal	Signal	Pin
1	GND	IO1	2
3	IO2	IO3	4
5	IO4	IO5	6
7	IO6	IO7	8

5 SLB Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1		2	IO6	3		4	IO7
5		6	IO4	7		8	IO5
9		10	IO2	11		12	IO3
13		14	IO1	15		16	
17		18		19		20	
21		22		23		24	
25		26		27		28	
29		30		31		32	
33		34		35		36	
37		38		39		40	
41	LED0	42	LED1	43	LED2	44	LED3
45		46		47		48	
49		50		51		52	
53		54		55		56	
57		58		59		60	
61		62		63		64	
65		66		67		68	
69	User MMCX	70		71		72	
73		74		75		76	
77		78		79		80	
81	ADC CONVST	82		83	ADC CS	84	
85	DAC CS	86		87	Load DAC	88	
89	ADC SCLK	90		91	ADC BUSY1	92	
93	ADC BUSY2	94		95	ADC BUSY3	96	
97	ADC BUSY4	98		99	ADC Data1	100	
101	ADC Data2	102		102	ADC Data3	104	
105	ADC Data4	106		107	DAC Data1	108	
109	DAC Data2	110		111	DAC Data3	112	
113	DAC Data4	114		115	DAC SCLK	116	
117	Oscillator	118		119	User MMCX	120	

6 Footprint


ADC Reference
Reference Amplifier
Input Amplifier
Common Mode Offset Control
ADC
IO
User LEDs
JTAG to Carrier
User MMCX
Oscillator
SLB Interface
DAC Reference
Output Amplifier
DAC

7 How It Works

7.1 ADC

ADC sampling starts with the assertion of ADC CONVST and ADC CS.
The ADC BUSY signals (one per ADC) will indicate when sampling is complete.
During the sample process, TI define quiet periods where no digital access is made (see data sheet for full timing details).

At the end of sampling (de-assertion of ADC BUSY), and outside of the quiet period, the sampled data may be clocked into the FPGA using the ADC SCLK and ADC Data signals, whilst ADC CS is asserted. Data is transferred serially.

7.2 DAC

DAC data is transferred from the FPGA serially using DAC SCLK and DAC Data, whilst DAC CS is asserted. There is one data signal per DAC device.

The DAC outputs all change to the most recent clocked data as the assertion of the Load DAC signal (DAC CS does not need to be asserted).

7.3 Sample Clock

The ADC sampling rate is controlled by the FPGA and the assertion of the ADC CONVST and ADC CS signals. The ADC uses a successive approximation technique to provide the 16-bit digital sample value. An external clock is not required as the ADC has a built-in oscillator.

To assist in obtaining an exact required sample rate, an on-board oscillator is provided which feeds the FPGA via the SLB. Typically, the value of this oscillator is set to a multiple of 2 of the required sample rate. Contact Sundance for information on available frequencies.

DAC output update rate is directly controlled by the Load DAC signal.

8 Support Packages

9 Physical Properties

Dimensions	107mm	64mm

Weight	

Voltage	Current
+12V	TBD
+5V	TBD
+3.3V	TBD
-12V	TBD

MTBF	

10 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

11 Safety

This module presents no hazard to the user when in normal use.

12 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.
This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.
Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

13 Ordering Information

Variations of this product are available with uni- or bi-polar DAC outputs.

Eg. SMT946-uni, SMT946-bi