Unit / Module Description:	Octal ADC SLB Mezzanine
Unit / Module Number:	SMT980
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Product Specification for SMT980

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Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	18/7/07	GKP
1.1	Specified input stages as passive filters. Added external SLB power connector.	23/10/07	GKP
1.2	Added TCXO	30/10/07	GKP

Table of Contents

1 Introduction

The SMT980 is a single width expansion SLB mezzanine that plugs onto base TIM that incorporates an SLB (eg SMT368).

It uses two Texas Instruments Analog-to-Digital Converters (ADS6455).

The SMT980 has a local 125MHz oscillator and an external clock input. These feed a multiplexer/buffer circuit, and are distributed to both ADCs. A clock output signal is also present on an MMCX connector.

ADCs are 14-bit and can sample at up to 125 MHz. All converters are 3.3-Volt.

Controlling of the ADCs is performed by the base TIM. Typically this utilizes a Xilinx FPGA which includes interfaces to the ADC control, TIM ComPorts, and the SLB's data interfaces.

The main features of the *SMT944* are listed below:

Eight 14-bit 125MSPS ADC (ADS6445),

On-board clock,

External clock and external triggers,

SLB connector to link SMT980 to base TIM,

Synchronisation signals,

All Analogue inputs are 50-Ohm terminated.

2 Related Documents

Sundance RSL specification (hyperlink to: http://www.sundance.com/docs/Specification_RSL.pdf).

Xilinx Virtex5 datasheets (hyperlink to: http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?category=Data+Sheets/FPGA+Device+Families/Virtex-5).

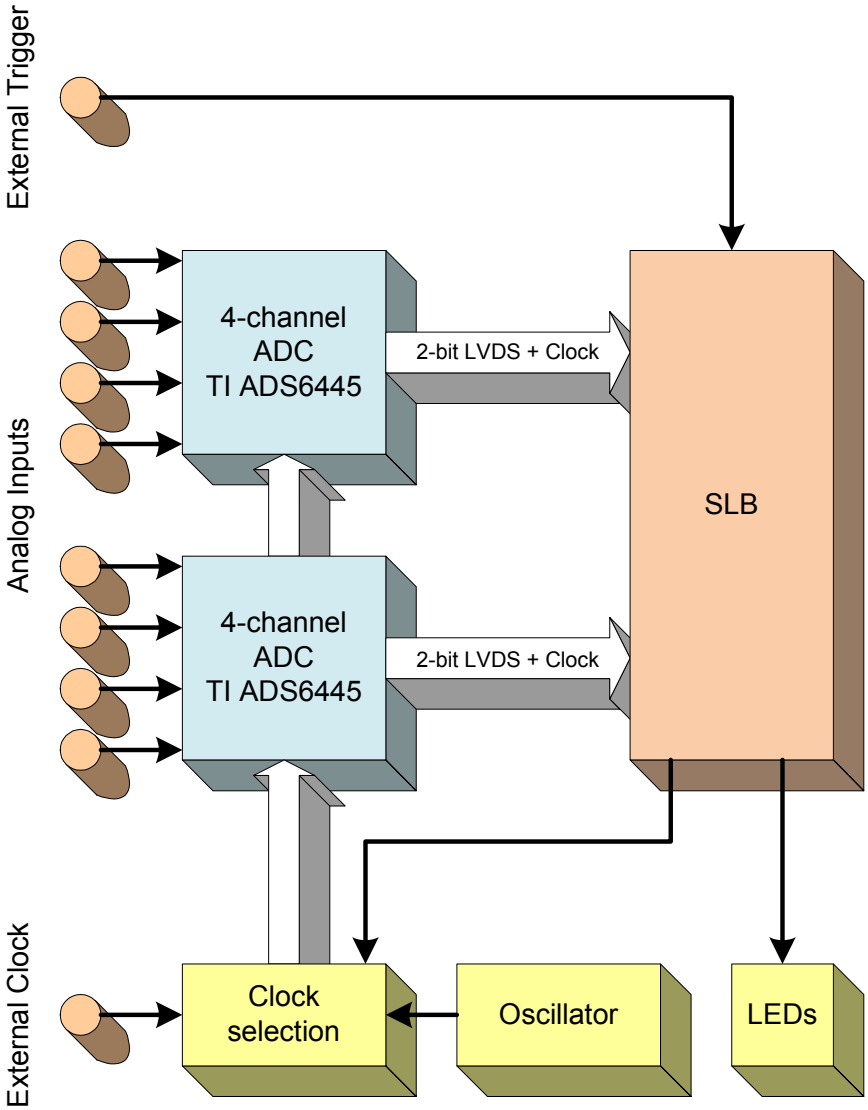
3 Acronyms, Abbreviations and Definitions

A list of acronyms etc (hyperlink to http://www.sundance.com/web/files/static.asp?pagename=acc).

4 Functional Description

The major elements of the SMT980 are shown in the block diagram below.

4.1 Block Diagram



4.2 Module Description

4.2.1 ADC

The ADC section uses two ADS6445 quad ADCs from Texas Instruments.

These devices output data on 2-bit LVDS buses. These are typically connected directly to an FPGA SERDES.

All inputs are via a differential passive filter.

4.2.2 FPGA

The SMT980 typically interfaces to an FPGA on a TIM module. This FPGA is responsible for collecting serial data from the ADCs.

Each ADC channel outputs 2-bit differential serial data. Each ADC device also outputs a differential clock and frame signal.

These serial signals are input to SERDES components within the FPGA. Xilinx application note xapp866 details how this interfacing works. (hyperlink: http://direct.xilinx.com/bvdocs/appnotes/xapp866.pdf)

4.2.3 LEDs

Four LEDs are available and connected directly to the TIMs FPGA.

4.2.4 Clock Control

The ADC clock is provided by a CFPT-9050 series TCVCXO.

An external co-ax connector can also supply the ADC clock.

Selection between the different clock sources is by means of a 0 Ohm resistor link.

4.2.5 SLB

The SLB data connector carries the LVDS signals from the two ADCs to the base TIM.

Signals are also available to control the LEDs and to select the clock source (local oscillator or external).

Power is provided via the SLB power connector and the external power connector.

Flat ribbon type cable assemblies are available which enable the SMT980 to be mounted away from the TIM.

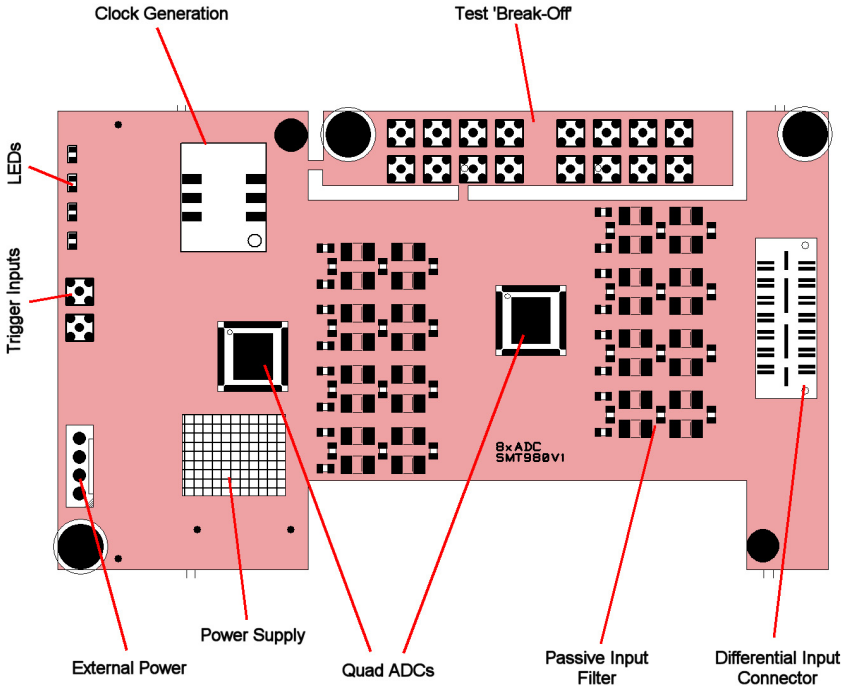
5 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

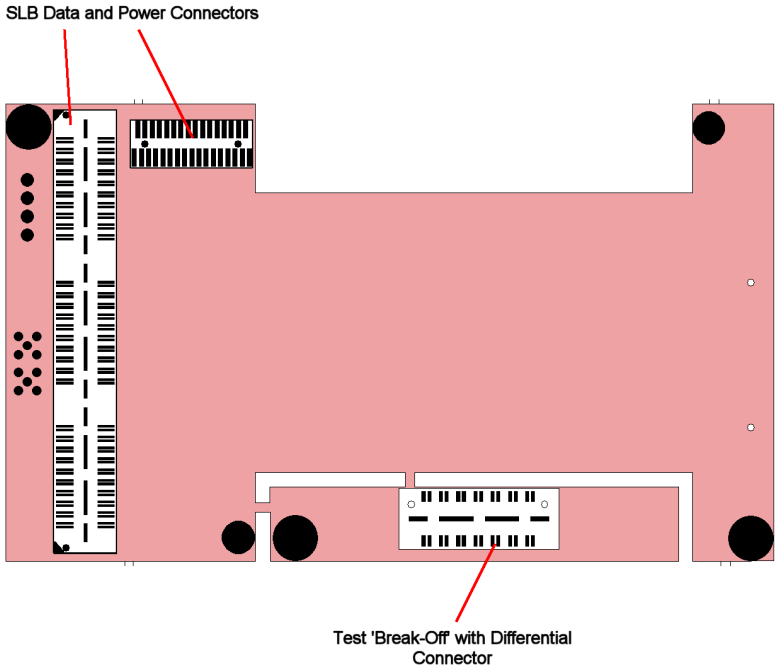
6 Circuit Description / Diagrams

7 Footprint

7.1 Top View



7.2 Bottom View



8 Support Packages

9 Physical Properties

Dimensions		

Weight	

Voltage	Current
+12V	0
+5V	TBD
+3.3V	TBD
-5V	0
-12V	0

MTBF	

10 Safety

This module presents no hazard to the user when in normal use.

11 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

12 Ordering Information

Part number:	SMT980	- both clock sources
	SMT980-OSC	- local oscillator option only
	SMT980-EXT	- external clock option only