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SMT SLB-FMC
User Manual

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Revision History

Issue	Changes Made	Date	Initials
1.0	First draft.	4/6/13	GKP

Table of Contents

1 Introduction

This module is used to allow an FMC mezzanine to be placed onto a Sundance SLB site. SLB sites are available on a range of carrier cards and TIM modules.

The SLB interface consists of two 16-bit differential synchronous buses. These buses can be split into two resulting in four 8-bit differential buses each with an independent clock.

In addition to the differential interfaces the SLB defines LVTTL signals and power rails.

Note that as all of the SLB signals are typically connected directly to an FPGA, then the signalling scheme (voltage level, single-ended/differential, etc) can be altered to suit the SLB mezzanine hardware design.

The FMC connector is the LPC (low pin count) type.

1.1 Power Supplies

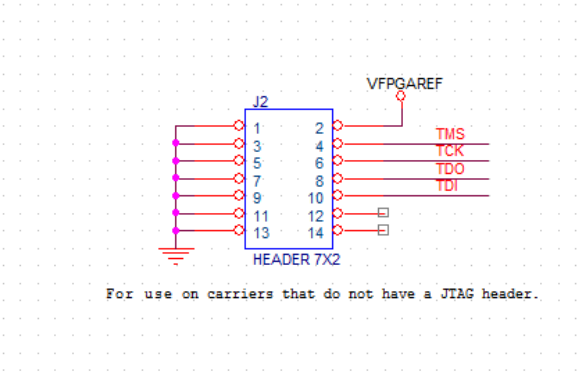
Power to the FMC is taken directly from the SLB power connector. This supplies +/-12V and +3.3V. Vadj for the FMC is provided via a linear regulator on the module. The output voltage is fixed at +2.5V

1.2 JTAG

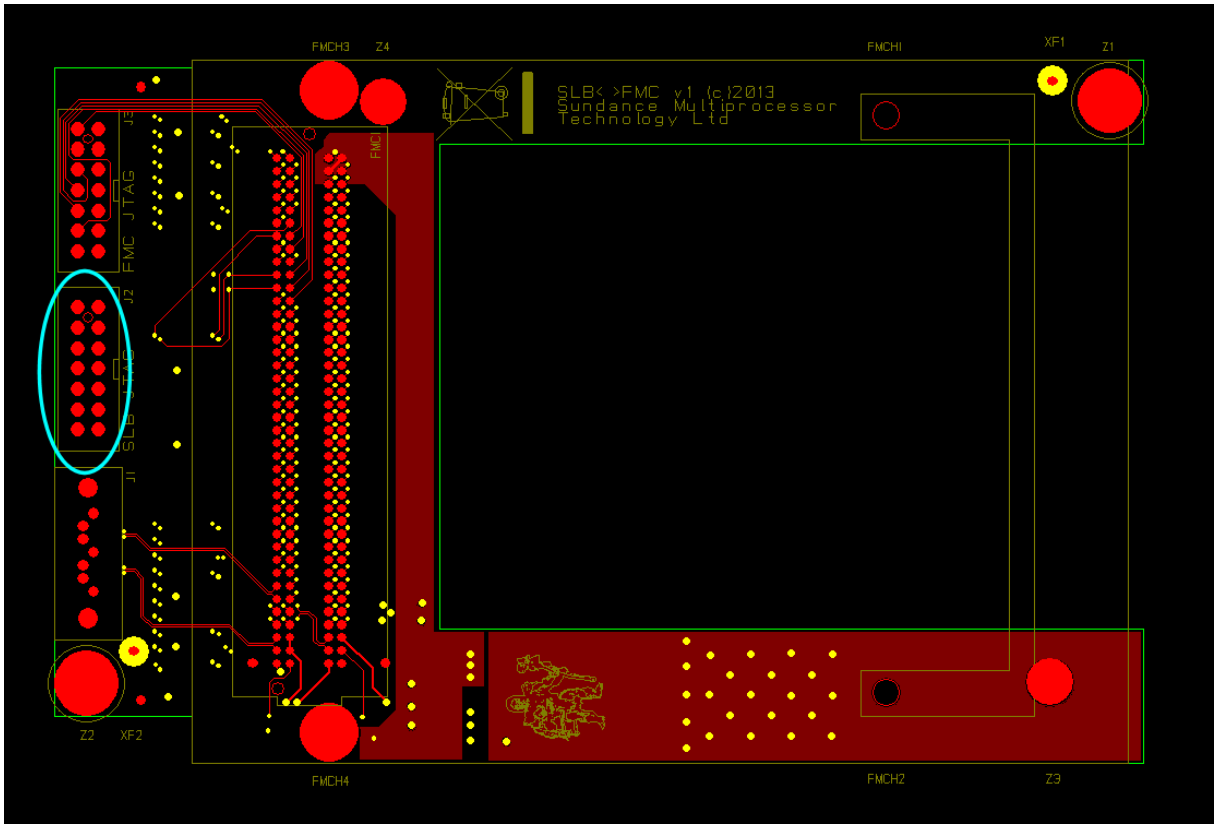
Two JTAG connectors are provided.

Header J2 is used to access the FPGA (if available) on the carrier card. This header may be in parallel to any that is present on the carrier. Only use one in such circumstances.

The pin-out of J2 is shown here:

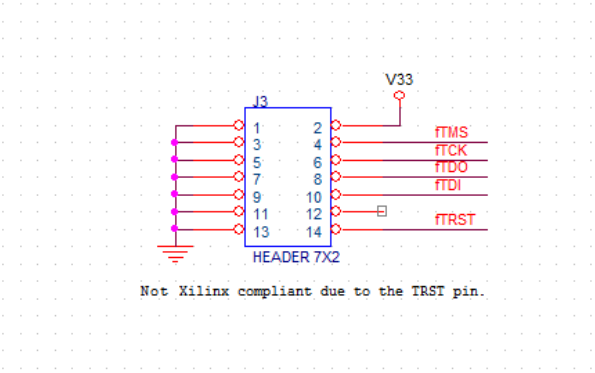


J2 is located here:

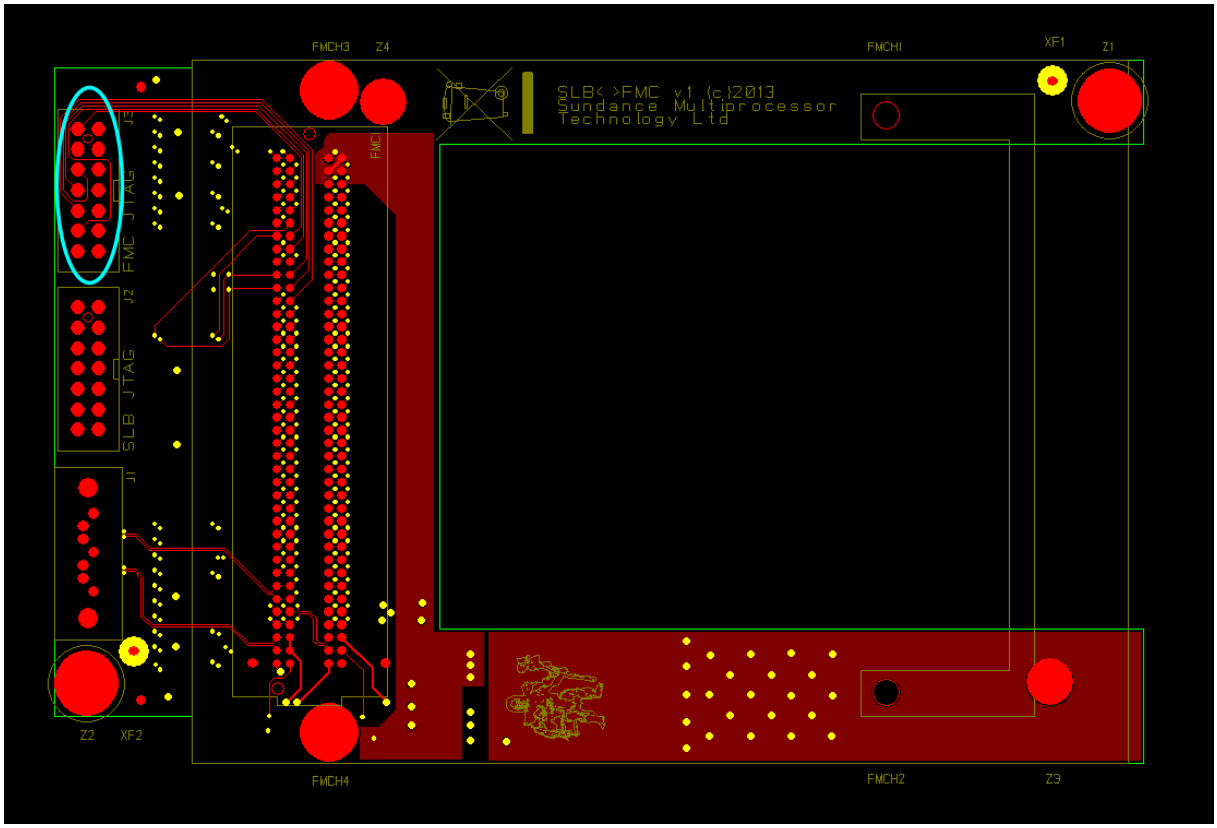


The second JTAG connector, J3, is for access to the FMC mezzanine. Note that not all mezzanines will include any devices that are accessible using JTAG.

The pin-out of J3 is shown here:

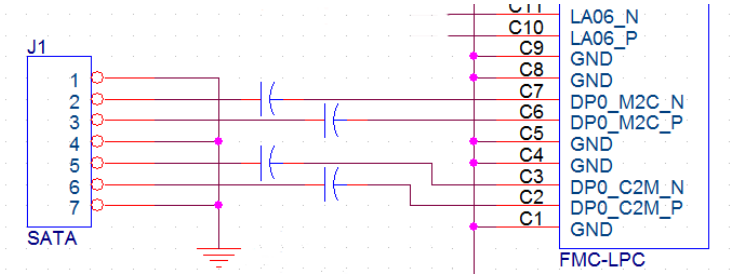


J3 is located here:



2 SATA

A SATA connector, J1, is provided that connects (via 100nF series capacitors) to the FMC connector. The connectivity is shown here:



3 SLB / FMC Signals

The majority of the signals are shown in the tables below. These list the FMC-LPC pin reference together with the SLB pin name and number.

C1	GND
C3	See SATA
C5	GND
C7	See SATA
C9	GND
C11	DOBQ4n / 100
C13	GND
C15	DOAQ2n / 91
C17	GND
C19	DOBQ0n / 84
C21	GND
C23	DOAI4n / 19
C25	GND
C27	DOBI3n / 16
C29	GND
C31	CNTRL1 / 47
C33	GND
C35	+12V
C37	+12V
C39	+3.3V

C2	See SATA
C4	GND
C6	See SATA
C8	GND
C10	DOBQ4p / 98
C12	GND
C14	DOAQ2p / 89
C16	GND
C18	DOBQ0p / 82
C20	GND
C22	DOAI4p / 17
C24	GND
C26	DOBI3p / 14
C28	GND
C30	CNTRL3 / 48
C32	GND
C34	CNTRL0 / 45
C36	GND
C38	GND
C40	GND

D1	10k Pull-up
D3	GND
D5	DOIRQn / 116
D7	GND
D9	DOAQ4n / 99
D11	DOBQ5p / 102
D13	GND
D15	DOBQ3n / 96
D17	DOBQ1p / 86
D19	GND
D21	ClkOIn / 35
D23	DOBI6p / 26
D25	GND
D27	DOAI6n / 27
D29	TCK
D31	TDO
D33	TMS
D35	CNTRL2 / 46
D37	GND
D39	GND

D2	GND
D4	DOIRQp / 114
D6	GND
D8	DOAQ4p / 97
D10	GND
D12	DOBQ5n / 104
D14	DOBQ3p / 94
D16	GND
D18	DOBQ1n / 88
D20	ClkOIp / 33
D22	GND
D24	DOBI6n / 28
D26	DOAI6p / 25
D28	GND
D30	TDI
D32	+3.3V
D34	TRST
D36	+3.3V
D38	+3.3V
D40	+3.3V

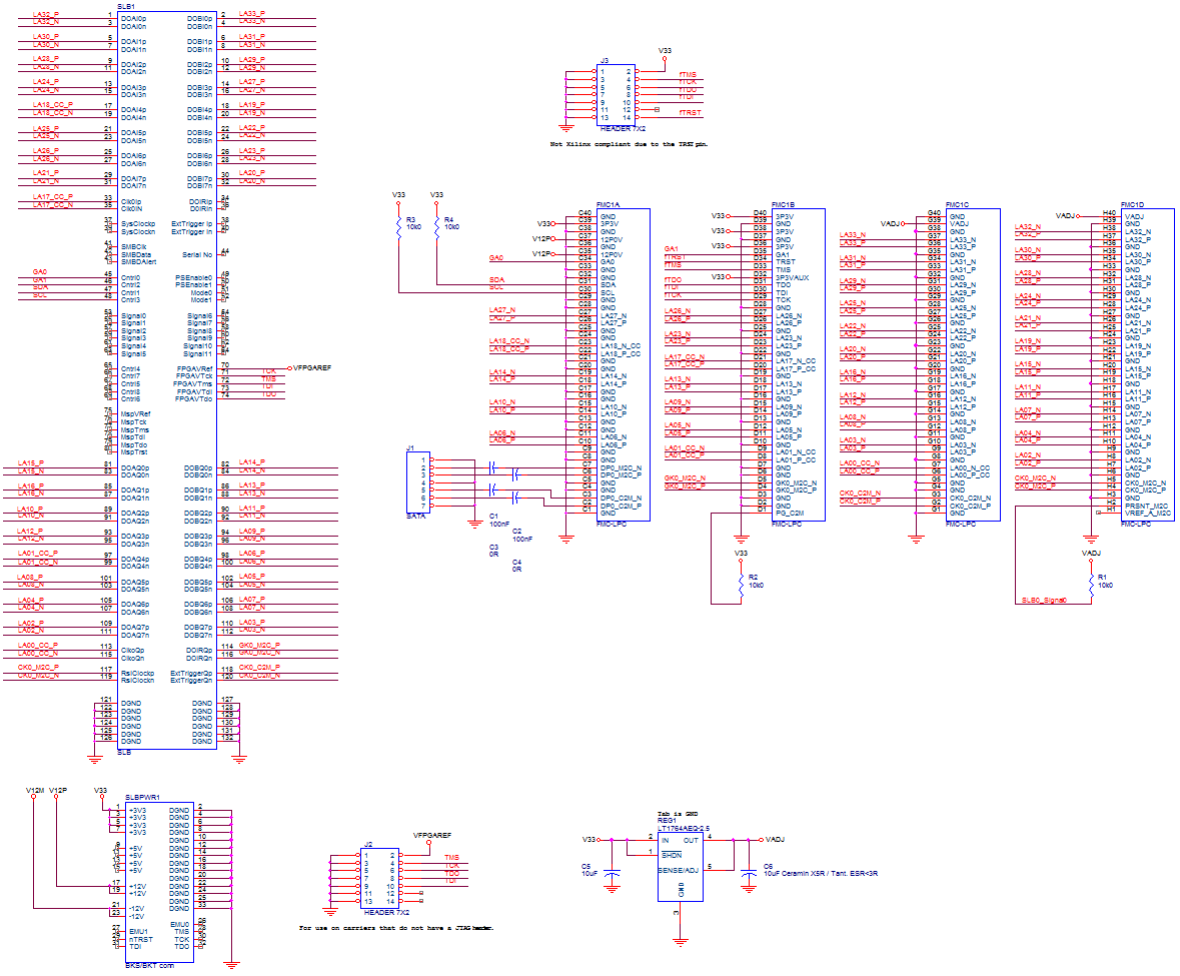
G1	GND
G3	ExTrgQn / 120
G5	GND
G7	ClkOQn / 115
G9	DOBQ7p / 110
G11	GND
G13	DOAQ5n / 103
G15	DOAQ3p / 93
G17	GND
G19	DOAQ1n / 87
G21	DOBI7p / 30
G23	GND
G25	DOBI5n / 24
G27	DOAI5p / 21
G29	GND
G31	DOBI2n / 12
G33	DOBI1p / 6
G35	GND
G37	DOBI0n / 4
G39	VADJ

G2	ExTrgQp / 118
G4	GND
G6	ClkOQp / 113
G8	GND
G10	DOBQ7n / 112
G12	DOAQ5p / 101
G14	GND
G16	DOAQ3n / 95
G18	DOAQ1p / 85
G20	GND
G22	DOBI7n / 32
G24	DOBI5p / 22
G26	GND
G28	DOAI5n / 23
G30	DOBI2p / 10
G32	GND
G34	DOBI1n / 8
G36	DOBI0p / 2
G38	GND
G40	GND

H1	NC
H3	GND
H5	RSLClkn / 119
H7	DOAQ7p / 109
H9	GND
H11	DOAQ6n / 107
H13	DOBQ6p / 106
H15	GND
H17	DOBQ2n / 92
H19	DOAQ0p / 81
H21	GND
H23	DOBI4n / 20
H25	DOAI7p / 29
H27	GND
H29	DOAI3n / 15
H31	DOAI2p / 9
H33	GND
H35	DOAI1n / 7
H37	DOAI0p / 1
H39	GND

H2	10k Pull-up
H4	RSLClkp / 117
H6	GND
H8	DOAQ7n / 111
H10	DOAQ6p / 105
H12	GND
H14	DOBQ6n / 108
H16	DOBQ2p / 90
H18	GND
H20	DOAQ0n / 83
H22	DOBI4p / 18
H24	GND
H26	DOAI7n / 31
H28	DOAI3p / 13
H30	GND
H32	DOAI2n / 11
H34	DOAI1p / 5
H36	GND
H38	DOAI0n / 3
H40	VADJ

4 Circuit Diagram



Full circuit details can be obtained under NDA from Sundance.