

ANALOGUE AND DIGITAL LOW LEVEL RF FOR THE ALBA SYNCHROTRON

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Abstract

ALBA is a 3 GeV, 400 mA, 3rd generation Synchrotron Light Source that is in the construction phase in Cerdanyola, Spain. The RF System will have to provide 3.6 MV of accelerating voltage and restore up to 540 kW of power to the electron beam. Two LLRF prototypes are being developed in parallel, both following the IQ modulation/demodulation technique. One is fully based on analogue technologies; the other is based on digital FPGA processing. The advantages of the IQ technique will be summarised and the control loop logic described. The hardware implementation in analogue as well as in digital format will be presented and first test results shown. The implementation of the same logic with both technologies will give us a perfect bench to compare, and use the better of them, for the final LLRF of the ALBA synchrotron.

INTRODUCTION

The task of a LLRF system is to regulate the amplitude and phase of the RF field and the resonance frequency of the cavity to compensate for transient beam loading, ripples of the high voltage power supply and temperature variations.

The specifications of the ALBA RF and LLRF are summarized in Table 1.

Table 1: RF/LLRF specifications of the storage ring

| | | |
|-------------------------|----------------------|-----|
| Frequency | 499.654 | MHz |
| No. of cavities | 6 | |
| RF power (per cavity) | 150 | kW |
| RF voltage (per cavity) | 600 | kV |
| Over-voltage factor | 2.8 | |
| Amplitude stability | ± 1 to ± 0.1 | % |
| Phase stability | ± 1 to ± 0.1 | ° |
| Bandwidth | > 200 kHz | kHz |
| Dynamic range | > 23 | dB |

LLRF SOLUTION FOR ALBA

While in the past traditional amplitude and phase loops were used for RF field regulation, today the IQ (In-phase, Quadrature) demodulation technique is favoured for modern accelerating structures. The translation of amplitude and phase information into IQ is advantageous because of the symmetry of the I/Q signal paths, less-complicated nature of the electronics and wider phase control range.

In the IQ method [1], an IQ demodulator is utilized at the input stage of the LLRF system to demodulate the cavity signal and convert the amplitude/phase information into I/Q. The I/Q components are then compared to their set values to generate the I/Q errors which feed the corresponding PID (Proportional-Integral-Derivative) regulators. The outputs of the PIDs are applied to a controlled baseband phase shifter which makes the I/Q loops stable. This is done by generating a certain phase shift to compensate for the time delays in the I/Q loops so that the real I/Q is compared to the reference one with correct polarity and scaling. An IQ modulator is utilized at the output stage of the LLRF system to regenerate a RF signal which will ultimately drive the power amplifiers.

For the implementation of an IQ-based LLRF system one can follow analogue or digital alternatives. The analogue solution is rather simple and cheap and provides low loop-delay and large bandwidth which can easily meet the RF regulation demands. Nevertheless, an analogue LLRF can suffer from a number of inherent errors including DC-offsets, drifts and low accuracy. As a result of these, its application is typically limited to 1% and 1° of amplitude and phase stability.

A digital LLRF system on the other hand has the advantage of giving much more flexibility as most of its building blocks are program routines which are executed by a DSP or a FPGA. Substantial changes in the design are possible by changing the program without affecting the hardware. With digital LLRF, amplitude and phase stabilities better than 0.1% and 0.1° are achievable. The main drawbacks of digital LLRF systems are their higher cost and complexity.

For ALBA, to built both RF analog and digital in house know-how it was decided to develop one prototype for each of them, and then choose the one which appears to be better for ALBA. The two LLRF prototypes however are conceptually quite similar; they are both based on the IQ method and PID regulation.

ANALOGUE PROTOTYPE

Design of the analogue prototype is shown in Figure 1. The IQ mod/dem is AD8345/AD8348 Evaluation Board from Analog Devices. As these boards are designed for laboratory tests we intend to replace them in a later stage with in-house developed IQ mod/dem which shall have better shielding hence less susceptible to the environmental noise. The differential to single-ended converters, the PIDs, the base-band phase shifter and the single-ended to differential converter boards are developed in-house. The rest of the RF components (i.e. the splitters, the RF pre-amp, the filters, the frequency doubler, etc.) are mainly from Mini-circuits.

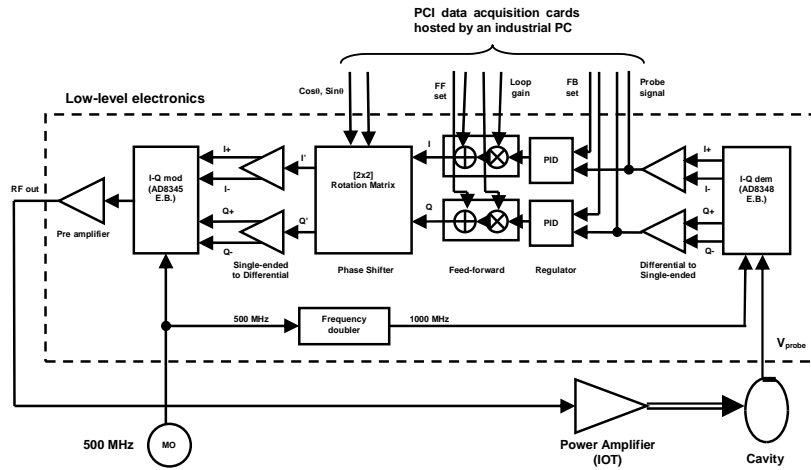


Figure 1: Analogue LLRF scheme

Test results

The analogue prototype was low-power tested with a cylindrical cavity made of Aluminium with a measured quality factor of 3300. Three types of closed loop tests were performed for tracking, amplitude and phase regulation.

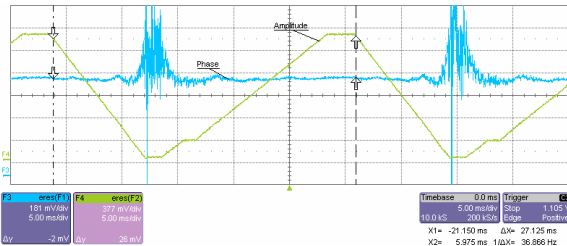


Figure 2: tracking test with a cycling frequency of 37 Hz.

For the amplitude and phase test, a rectangular amplitude and phase disturbance was imposed on the cavity probe signal. The loop was able to compensate the disturbance in 15 μ s.

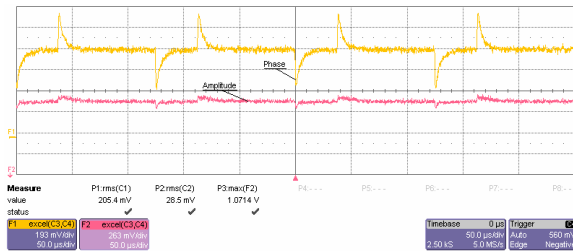


Figure 3: result of the phase test.

The results are promising except the high noise level ($\pm 3\%$ and $\pm 7^\circ$ for amplitude and phase respectively) which was due to the poor shielding of the signals from the control computer. A few solutions are currently being investigated to reduce the susceptibility of the electronics to noise and improve the short and long term stability.

DIGITAL PROTOTYPE

The Digital LLRF (DLLRF) of ALBA is based on digital IQ modulation/demodulation carried out by a FPGA board [2]. The DLLRF is intended to control de amplitude and phase of the RF Cavity voltage within 0.1% and 0.1 $^\circ$ respectively, as well as the resonance frequency of the cavity.

The main components of the DLLRF system are:

- Two analogue front ends for up/down conversion
- A commercial PCI board with two ADCs, two DACs, one FPGA and one DSP, from Sundance.
- An analogue and a digital timing system.

The design of the digital prototype is shown in Figure 4.

Analog Front Ends: Down and Upconversion

According to the scheme on Figure 4, two input signals are sent to the DLLRF System: the cavity voltage and the forward power.

The frequency of the RF input signals is 500MHz and they are downconverted to IF (20MHz) in the first analogue front end. The IF signals, which are equivalent in phase and amplitude to the RF signals, are sent to the ADCs of the board to be digitally demodulated into their I and Q components. To do so the signals are sampled at 80MHz, a frequency four times higher than the inputs, obtaining an alternative sequence of the I and Q components (I, Q, -I, -Q...) as shown in Fig. 5.

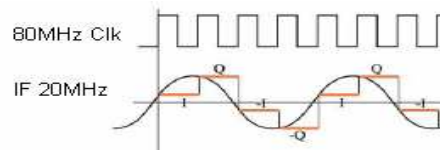


Figure 5. Digital IQ Demodulation

A PI control algorithm is applied to the I and Q cavity components to obtain the control actions that will be digitally upconverted again to IF.

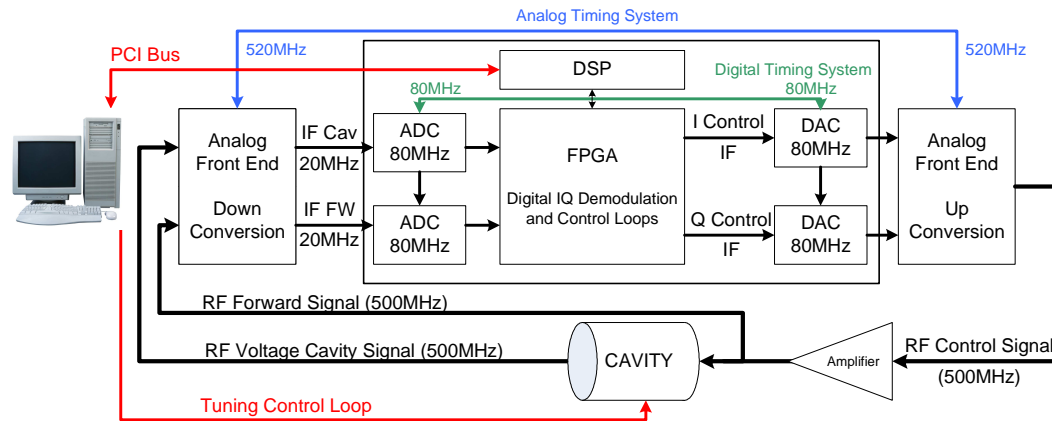


Figure 4: Digital LLRF Scheme.

The DACs transform the IF control signals into analogue, and finally those signals are upconverted to RF in the second analogue front end, using a single side band quadrature modulator [3], as shown in Figure 6.

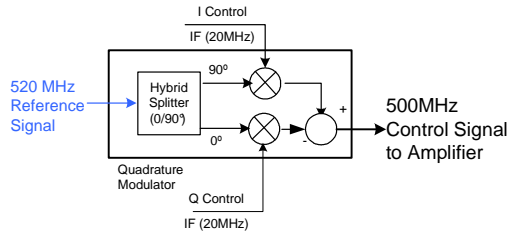


Figure 6. Upconversion of control signals to 500MHz

Control Loops

The amplitude and phase of the cavity voltage are controlled by a PI loop applied to the I and Q components of the cavity voltage signal.

The resonance frequency of the cavity is controlled by the tuning loop which calculates the phase difference between the cavity voltage and the forward voltage using the cross product of these two signals as phase discriminator. When both signals are in phase the product result is zero. Otherwise, the result is accumulated until it reaches certain value and the system sends a command through the PC to the tuner controller to move the tuner.

Timing Systems

The aim of the analogue timing system is to provide a reference signal (RF clock + 20MHz) for performing the down and upconversion in the analogue front ends. As the RF clock frequency will slightly vary (to perform close orbit corrections) and thus, affect the performance of the digital demodulation, the reference signal is generated by mixing the RF clock with a 20MHz signal. In this way the mixing product of the RF cavity signals and the RF reference signal will be always 20MHz, as it is requested for the digital demodulation.

The digital timing system consists of a clock synchronizer board with a VCXO of 80MHz. The board synchronizes the output of the VCXO with an external 10MHz signal and also it divides the VCXO output by four to generate the 20MHz signal to obtain the reference signal of the analogue front ends.

Interface

The DSP sends to the Host PC the signals generated in the FPGA during the digital processing. In overall 14 diagnostic signals are stored and displayed using a Matlab interface, including I&Q Reference Signals, I&Q Cavity Signals, I&Q Proportional Errors, I&Q Integral Errors, I&Q Control actions, I&Q Forward Signals and Cross Product and Accumulative Cross Product of the Cavity and Forward Signals [4].

Preliminary Test Results

We have analyzed the reaction of the loop when its reference set point is changed. The loop response time has been measured, with and without the cavity (2.24 μ s and 4.8 μ s respectively) as depicted in Figure 7. The time response without the cavity corresponds to the group delay of the analogue front ends, the digital board and the loop. The time response is larger with the cavity due to the filling time of the cavity which is around 2.5 μ s

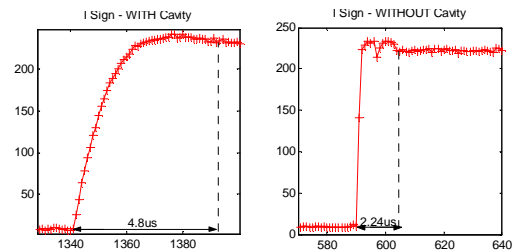


Figure 7. PI Loop Step response with & without cavity

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