```
sundance@sundance-Amd-Am5-Workstation:~/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards$ make BOARD=vcs-3
BOARD: vcs-3
VITIS_PLATFORM: /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/platform.xsa
bash check_env.sh
wget -O DPUCZDX8G.tar.gz
https://www.xilinx.com/bin/public/openDownload?filename=DPUCZDX8G_VAI_v3.0
.tar.gz && \
        tar xf DPUCZDX8G.tar.gz && \
mv DPUCZDX8G_VAI_v3.0 DPUCZDX8G && \
rm DPUCZDX8G.tar.gz
--2025-12-20 13:37:16--
https://www.xilinx.com/bin/public/openDownload?filename=DPUCZDX8G_VAI_v3.0
.tar.gz
Resolving www.xilinx.com (www.xilinx.com)... 2.23.210.138, 2.23.210.195
Connecting to www.xilinx.com (www.xilinx.com)|2.23.210.138|:443...
connected.
HTTP request sent, awaiting response... 301 Moved Permanently
Location:
https://download.amd.com/opendownload/xlnx/DPUCZDX8G_VAI_v3.0.tar.gz
[following]
--2025-12-20 13:37:16--
https://download.amd.com/opendownload/xlnx/DPUCZDX8G_VAI_v3.0.tar.gz
Resolving download.amd.com (download.amd.com)... 23.215.233.47
Connecting to download.amd.com (download.amd.com)|23.215.233.47|:443...
connected.
HTTP request sent, awaiting response... 200 OK
Length: 83014878 (79M) [application/x-gzip]
Saving to: ‘DPUCZDX8G.tar.gz’

DPUCZDX8G.tar.gz           100%[===================================>]
79.17M  25.8MB/s    in 3.1s

2025-12-20 13:37:19 (25.8 MB/s) - ‘DPUCZDX8G.tar.gz’ saved
[83014878/83014878]

cp -rf /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/DPUCZDX8G/prj/Vitis/kernel_xml/dpu/kernel.xml
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/kernel_xml/dpu/kernel.xml
cp -f /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/DPUCZDX8G/prj/Vitis/scripts/package_dpu_kernel.tcl
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/scripts/package_dpu_kernel.tcl
sed -i 's/set path_to_hdl "..\/..\/dpu_ip"/set path_to_hdl
```

```
"..\/DPUCZDX8G\/dpu_ip"/' /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/scripts/package_dpu_kernel.tcl
cp -f /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/DPUCZDX8G/prj/Vitis/scripts/gen_dpu_xo.tcl
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/scripts/gen_dpu_xo.tcl
cp -f /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/DPUCZDX8G/prj/Vitis/scripts/bip_proc.tcl
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/scripts/bip_proc.tcl
cd /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3 ;\
/tools/Xilinx/Vivado/2023.1/Vivado/2023.1/bin/vivado -mode batch -source
scripts/gen_dpu_xo.tcl -notrace -tclargs binary_container_1/dpu.xo
DPUCZDX8G hw vcs-3

****** Vivado v2023.1 (64-bit)
  **** SW Build 3865809 on Sun May  7 15:04:56 MDT 2023
  **** IP Build 3864474 on Sun May  7 20:36:21 MDT 2023
  **** SharedData Build 3865790 on Sun May 07 13:33:03 MDT 2023
    ** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
    ** Copyright 2022-2023 Advanced Micro Devices, Inc. All Rights
Reserved.

source scripts/gen_dpu_xo.tcl -notrace
binary_container_1/dpu.xo
INFO: [IP_Flow 19-5654] Module 'DPUCZDX8G' uses SystemVerilog sources with
a Verilog top file. These SystemVerilog files will not be analysed by the
packager.
INFO: [IP_Flow 19-1842] HDL Parser: Found include file "src/arch_def.vh"
from the top-level HDL file.
INFO: [IP_Flow 19-1842] HDL Parser: Found include file
"/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/dpu_conf.vh" from the top-level HDL file.
INFO: [IP_Flow 19-1841] HDL Parser: Add include file
"/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/dpu_conf.vh" to file group xilinx_anylanguagesynthesis.
INFO: [IP_Flow 19-1841] HDL Parser: Add include file
"/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/dpu_conf.vh" to file group
xilinx_anylanguagebehavioralsimulation.
INFO: [IP_Flow 19-1842] HDL Parser: Found include file "src/arch_para.vh"
from the top-level HDL file.
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
```

```
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/tools/Xilinx/Vivado/2023.1/Vivado/2023.1/data/ip'.
INFO: [IP_Flow 19-5107] Inferred bus interface 'aclk' of definition
'xilinx.com:signal:clock:1.0' (from X_INTERFACE_INFO parameter from HDL
file).
INFO: [IP_Flow 19-5107] Inferred bus interface 'aclk' of definition
'xilinx.com:signal:clock:1.0' (from 'X_INTERFACE_INFO' attribute).
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_clk_2' of definition
'xilinx.com:signal:clock:1.0' (from X_INTERFACE_INFO parameter from HDL
file).
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_clk_2' of definition
'xilinx.com:signal:clock:1.0' (from 'X_INTERFACE_INFO' attribute).
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_rst_n_2' of definition
'xilinx.com:signal:reset:1.0' (from X_INTERFACE_INFO parameter from HDL
file).
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_rst_n_2' of definition
'xilinx.com:signal:reset:1.0' (from 'X_INTERFACE_INFO' attribute).
INFO: [IP_Flow 19-5107] Inferred bus interface 'aresetn' of definition
'xilinx.com:signal:reset:1.0' (from X_INTERFACE_INFO parameter from HDL
file).
INFO: [IP_Flow 19-5107] Inferred bus interface 'aresetn' of definition
'xilinx.com:signal:reset:1.0' (from 'X_INTERFACE_INFO' attribute).
INFO: [IP_Flow 19-5107] Inferred bus interface 'M_AXI_GP0' of definition
'xilinx.com:interface:aximm:1.0' (from Xilinx Repository).
INFO: [IP_Flow 19-5107] Inferred bus interface 'M_AXI_HP0' of definition
'xilinx.com:interface:aximm:1.0' (from Xilinx Repository).
INFO: [IP_Flow 19-5107] Inferred bus interface 'M_AXI_HP2' of definition
'xilinx.com:interface:aximm:1.0' (from Xilinx Repository).
INFO: [IP_Flow 19-5107] Inferred bus interface 'S_AXI_CONTROL' of
definition 'xilinx.com:interface:aximm:1.0' (from Xilinx Repository).
INFO: [IP_Flow 19-5107] Inferred bus interface 'interrupt' of definition
'xilinx.com:signal:interrupt:1.0' (from Xilinx Repository).
INFO: [IP_Flow 19-4728] Bus Interface 'interrupt': Added interface
parameter 'SENSITIVITY' with value 'LEVEL_HIGH'.
INFO: [IP_Flow 19-4728] Bus Interface 'aclk': Added interface parameter
'ASSOCIATED_BUSIF' with value 'M_AXI_GP0'.
INFO: [IP_Flow 19-4728] Bus Interface 'aclk': Added interface parameter
'ASSOCIATED_RESET' with value 'aresetn'.
INFO: [IP_Flow 19-4728] Bus Interface 'ap_clk_2': Added interface
parameter 'ASSOCIATED_RESET' with value 'ap_rst_n_2'.
INFO: [IP_Flow 19-4728] Bus Interface 'ap_rst_n_2': Added interface
parameter 'POLARITY' with value 'ACTIVE_LOW'.
INFO: [IP_Flow 19-4728] Bus Interface 'aresetn': Added interface parameter
'POLARITY' with value 'ACTIVE_LOW'.
INFO: [IP_Flow 19-818] Not transferring value dependency attribute "((4 <
2) ? 4 : 2)" into user parameter "ELEW_PARALLEL".
```

```
INFO: [IP_Flow 19-818] Not transferring value dependency attribute "((4 <
2) ? 4 : 2)" into user parameter "ALU_PARALLEL".
WARNING: [IP_Flow 19-11770] Clock interface 'aclk' has no FREQ_HZ
parameter.
WARNING: [IP_Flow 19-5661] Bus Interface 'ap_clk_2' does not have any bus
interfaces associated with it.
WARNING: [IP_Flow 19-11770] Clock interface 'ap_clk_2' has no FREQ_HZ
parameter.
WARNING: [IP_Flow 19-3157] Bus Interface 'ap_rst_n_2': Bus parameter
POLARITY is ACTIVE_LOW but port 'ap_rst_n_2' is not *resetn - please
double check the POLARITY setting.
WARNING: [IP_Flow 19-731] File Group 'xilinx_anylanguagesynthesis
(Synthesis)': "/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/dpu_conf.vh" file path is not relative to
the IP root directory.
WARNING: [IP_Flow 19-4816] The Synthesis file group has two include files
that have the same base name. It is not guaranteed which of these two
files will be picked up during synthesis/simulation:   src/dpu_conf.vh
  /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/dpu_conf.vh
WARNING: [IP_Flow 19-991] Unrecognized or unsupported file
'src/fingerprint_json.ttcl' found in file group 'Synthesis'.
Resolution: Remove the file from the specified file group.
WARNING: [IP_Flow 19-731] File Group
'xilinx_anylanguagebehavioralsimulation (Simulation)':
"/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/dpu_conf.vh" file path is not relative to the IP root
directory.
WARNING: [IP_Flow 19-4816] The Simulation file group has two include files
that have the same base name. It is not guaranteed which of these two
files will be picked up during synthesis/simulation:   src/dpu_conf.vh
  /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/dpu_conf.vh
WARNING: [IP_Flow 19-991] Unrecognized or unsupported file
'src/fingerprint_json.ttcl' found in file group 'Simulation'.
Resolution: Remove the file from the specified file group.
INFO: [IP_Flow 19-2181] Payment Required is not set for this core.
INFO: [IP_Flow 19-2187] The Product Guide file is missing.
INFO: [IP_Flow 19-795] Syncing license key meta-data
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/tools/Xilinx/Vivado/2023.1/Vivado/2023.1/data/ip'.
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_clk_2' of definition
'xilinx.com:signal:clock:1.0' (from TCL Argument).
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_rst_n_2' of definition
```

```
'xilinx.com:signal:reset:1.0' (from TCL Argument).
WARNING: [Vivado 12-4404] The CPU emulation flow in v++ is only supported
when using a packaged XO file that contains C-model files, none were
found.
INFO: [Common 17-206] Exiting Vivado at Sat Dec 20 13:37:27 2025...
cd /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3 ;\
v++ -t hw --platform /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/platform.xsa --save-temps --config
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/prj_config --xp
param:compiler.userPostSysLinkOverlayTcl=/home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/DPUCZDX8G/prj/Vitis/syslink/strip_interconnects.tcl  -l --
temp_dir binary_container_1 \
      --log_dir binary_container_1/logs --package.no_image \
      --remote_ip_cache binary_container_1/ip_cache -o
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/dpu.xclbin binary_container_1/dpu.xo
WARNING: [v++ 60-1600] The option 'xp' was used directly on the command
line, where its usage is deprecated. To ensure input line works for
supported operating systems or shells, v++ supports specification for some
options in a configuration file. As an alternative, please use options
'advanced.*', 'vivado.*' in a configuration file. Use one or more
configuration files along with section headers to define key-value pairs
for the advanced properties or parameters. Specify a configuration file
using '--config'.
INFO: [v++ 82-185] Check out the auto-generated 'sample_link.ini'
configuration file. The file shows how to migrate from deprecated command
line --xp switches to configuration file directives.
Option Map File Used:
'/tools/Xilinx/Vivado/2023.1/Vitis/2023.1/data/vitis/vpp/optMap.xml'

****** v++ v2023.1 (64-bit)
  **** SW Build 3860322 on 2023-05-04-06:32:48
    ** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
    ** Copyright 2022-2023 Advanced Micro Devices, Inc. All Rights
Reserved.

INFO: [v++ 60-1306] Additional information associated with this v++ link
can be found at:
      Reports: /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/reports/link
      Log files: /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/logs/link
Running Dispatch Server on port: 43787
```

```
INFO: [v++ 60-1548] Creating build summary session with primary output
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/dpu.xclbin.link_summary, at Sat Dec
20 13:37:41 2025
INFO: [v++ 60-1315] Creating rulecheck session with output
'/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-
3/binary_container_1/reports/link/v++_link_dpu_guidance.html', at Sat Dec
20 13:37:41 2025
INFO: [v++ 60-895]   Target platform: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-3/platform.xsa
INFO: [v++ 60-1578]   This platform contains Xilinx Shell Archive
'/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/platform.xsa'
INFO: [v++ 60-629] Linking for hardware target
INFO: [v++ 60-423]   Target device: xilinx_vcs-
3_sundance_vcs3_platform_0_0
INFO: [v++ 60-1332] Run 'run_link' status: Not started
INFO: [v++ 60-1443] [13:37:41] Run run_link: Step system_link: Started
INFO: [v++ 60-1453] Command Line: system_link --xo
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/dpu.xo -keep --config
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/syslinkConfig.ini --xpfm
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/platform.xsa --target hw --output_dir
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int --temp_dir
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/sys_link
INFO: [v++ 60-1454] Run Directory: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/run_link
INFO: [SYSTEM_LINK 82-70] Extracting xo v3 file
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/dpu.xo
INFO: [SYSTEM_LINK 82-53] Creating IP database
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/sys_link/_sysl/.cdb/xd_ip_db.xml
INFO: [SYSTEM_LINK 82-38] [13:37:42] build_xd_ip_db started:
/tools/Xilinx/Vivado/2023.1/Vitis/2023.1/bin/build_xd_ip_db -ip_search 0
-sds-pf /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/sys_link/vcs3_dpu_platform.hpfm
-clkid 1 -ip /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/sys_link/iprepo/xilinx_com_RTLKernel_DPUCZDX8G_1
```

```
_0,DPUCZDX8G -o /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/sys_link/_sysl/.cdb/xd_ip_db.xml
INFO: [SYSTEM_LINK 82-37] [13:37:43] build_xd_ip_db finished successfully
Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak =
451.969 ; gain = 0.000 ; free physical = 17381 ; free virtual = 42665
INFO: [SYSTEM_LINK 82-51] Create system connectivity graph
INFO: [SYSTEM_LINK 82-102] Applying explicit connections to the system
connectivity graph: /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/sys_link/cfgraph/cfgen_cfgraph.xml
INFO: [SYSTEM_LINK 82-38] [13:37:43] cfgen started:
/tools/Xilinx/Vivado/2023.1/Vitis/2023.1/bin/cfgen  -nk DPUCZDX8G:1 -sp
DPUCZDX8G_1.M_AXI_GP0:HPC0 -sp DPUCZDX8G_1.M_AXI_HP0:HP0 -sp
DPUCZDX8G_1.M_AXI_HP2:HP1 -dpa_mem_offload false -dmclkid 1 -r
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/sys_link/_sysl/.cdb/xd_ip_db.xml
-o /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-
3/binary_container_1/link/sys_link/cfgraph/cfgen_cfgraph.xml
INFO: [CFGEN 83-0] Kernel Specs:
INFO: [CFGEN 83-0]   kernel: DPUCZDX8G, num: 1  {DPUCZDX8G_1}
INFO: [CFGEN 83-0] Port Specs:
INFO: [CFGEN 83-0]   kernel: DPUCZDX8G_1, k_port: M_AXI_GP0, sptag: HPC0
INFO: [CFGEN 83-0]   kernel: DPUCZDX8G_1, k_port: M_AXI_HP0, sptag: HP0
INFO: [CFGEN 83-0]   kernel: DPUCZDX8G_1, k_port: M_AXI_HP2, sptag: HP1
INFO: [SYSTEM_LINK 82-37] [13:37:44] cfgen finished successfully
Time (s): cpu = 00:00:00.48 ; elapsed = 00:00:00.49 . Memory (MB): peak =
451.969 ; gain = 0.000 ; free physical = 17387 ; free virtual = 42671
INFO: [SYSTEM_LINK 82-52] Create top-level block diagram
INFO: [SYSTEM_LINK 82-38] [13:37:44] cf2bd started:
/tools/Xilinx/Vivado/2023.1/Vitis/2023.1/bin/cf2bd  --linux --trace_buffer
1024 --input_file /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/sys_link/cfgraph/cfgen_cfgraph.xml --ip_db
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/sys_link/_sysl/.cdb/xd_ip_db.xml
--cf_name dr --working_dir /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/sys_link/_sysl/.xsd --temp_dir
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/sys_link --output_dir
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int
INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer 1024 -i
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
```

```
PYNQ/boards/vcs-
3/binary_container_1/link/sys_link/cfgraph/cfgen_cfgraph.xml -r
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/sys_link/_sysl/.cdb/xd_ip_db.xml
-o dr.xml
INFO: [CF2BD 82-28] cf2xd finished successfully
INFO: [CF2BD 82-31] Launching cf_xsd: cf_xsd -disable-address-gen -dn dr -
dp /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/sys_link/_sysl/.xsd
INFO: [CF2BD 82-28] cf_xsd finished successfully
INFO: [SYSTEM_LINK 82-37] [13:37:45] cf2bd finished successfully
Time (s): cpu = 00:00:00.72 ; elapsed = 00:00:00.84 . Memory (MB): peak =
451.969 ; gain = 0.000 ; free physical = 17392 ; free virtual = 42680
INFO: [v++ 60-1441] [13:37:45] Run run_link: Step system_link: Completed
Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak =
449.574 ; gain = 0.000 ; free physical = 17431 ; free virtual = 42719
INFO: [v++ 60-1443] [13:37:45] Run run_link: Step cf2sw: Started
INFO: [v++ 60-1453] Command Line: cf2sw -sdsl /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/int/sdsl.dat -rtd /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/int/cf2sw.rtd -nofilter
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/cf2sw_full.rtd -xclbin
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/xclbin_orig.xml -o
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/xclbin_orig.1.xml
INFO: [v++ 60-1454] Run Directory: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/run_link
INFO: [v++ 60-1441] [13:37:45] Run run_link: Step cf2sw: Completed
Time (s): cpu = 00:00:00.6 ; elapsed = 00:00:00.64 . Memory (MB): peak =
449.574 ; gain = 0.000 ; free physical = 17397 ; free virtual = 42686
INFO: [v++ 60-1443] [13:37:45] Run run_link: Step rtd2_system_diagram:
Started
INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram
INFO: [v++ 60-1454] Run Directory: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/run_link
INFO: [v++ 60-1441] [13:37:45] Run run_link: Step rtd2_system_diagram:
Completed
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.03 . Memory (MB): peak =
449.574 ; gain = 0.000 ; free physical = 17397 ; free virtual = 42686
INFO: [v++ 60-1443] [13:37:45] Run run_link: Step vpl: Started
INFO: [v++ 60-1453] Command Line: vpl -t hw -f
```

```
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/platform.xsa -s --remote_ip_cache
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/ip_cache --output_dir
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int --log_dir
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/logs/link --report_dir
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/reports/link --config
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/vplConfig.ini -k
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/kernel_info.dat --
webtalk_flag Vitis --temp_dir /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link --no-info --iprepo /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/int/xo/ip_repo/xilinx_com_RTLKernel_DPUCZDX8G_1_
0 --messageDb /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/link/run_link/vpl.pb
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/dr.bd.tcl
INFO: [v++ 60-1454] Run Directory: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/run_link

****** vpl v2023.1 (64-bit)
  **** SW Build 3860322 on 2023-05-04-06:32:48
    ** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
    ** Copyright 2022-2023 Advanced Micro Devices, Inc. All Rights
Reserved.

INFO: [VPL 60-839] Read in kernel information from file
'/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/kernel_info.dat'.
INFO: [VPL 60-423]   Target device: xilinx_vcs-
3_sundance_vcs3_platform_0_0
INFO: [VPL 60-1032] Extracting hardware platform to
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/vivado/vpl/.local/hw_platform
[13:37:48] Run vpl: Step create_project: Started
Creating Vivado project.
[13:37:51] Run vpl: Step create_project: Completed
[13:37:51] Run vpl: Step create_bd: Started
[13:37:53] Run vpl: Step create_bd: Completed
```

```
[13:37:53] Run vpl: Step update_bd: Started
[13:37:53] Run vpl: Step update_bd: Completed
[13:37:53] Run vpl: Step generate_target: Started
[13:38:04] Run vpl: Step generate_target: Completed
[13:38:04] Run vpl: Step config_hw_runs: Started
[13:38:04] Run vpl: Step config_hw_runs: Completed
[13:38:04] Run vpl: Step synth: Started
[13:38:34] Block-level synthesis in progress, 8 of 11 jobs complete, 3
jobs running.
[13:39:05] Block-level synthesis in progress, 10 of 11 jobs complete, 1
job running.
[13:39:35] Block-level synthesis in progress, 10 of 11 jobs complete, 1
job running.
[13:40:05] Block-level synthesis in progress, 10 of 11 jobs complete, 1
job running.
[13:40:35] Top-level synthesis in progress.
[13:40:41] Run vpl: Step synth: Completed
[13:40:41] Run vpl: Step impl: Started
[13:41:12] Finished 2nd of 6 tasks (FPGA linking synthesized kernels to
platform). Elapsed time: 00h 03m 25s

[13:41:12] Starting logic optimization..
[13:41:12] Phase 1 Retarget
[13:41:12] Phase 2 Constant propagation
[13:41:12] Phase 3 Sweep
[13:41:12] Phase 4 BUFG optimization
[13:41:42] Finished 3rd of 6 tasks (FPGA logic optimization). Elapsed
time: 00h 00m 30s

[13:41:42] Starting logic placement..
[13:41:42] Phase 1 Placer Initialization
[13:41:42] Phase 1.1 Placer Initialization Netlist Sorting
[13:41:42] Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
[13:41:42] Phase 1.3 Build Placer Netlist Model
[13:41:42] Phase 1.4 Constrain Clocks/Macros
[13:41:42] Phase 2 Global Placement
[13:41:42] Phase 2.1 Floorplanning
[13:41:42] Phase 2.1.1 Partition Driven Placement
[13:41:42] Phase 2.1.1.1 PBP: Partition Driven Placement
[13:41:42] Phase 2.1.1.2 PBP: Clock Region Placement
[13:41:42] Phase 2.1.1.3 PBP: Discrete Incremental
[13:41:42] Phase 2.1.1.4 PBP: Compute Congestion
[13:41:42] Phase 2.1.1.5 PBP: Macro Placement
[13:41:42] Phase 2.1.1.6 PBP: UpdateTiming
[13:41:42] Phase 5 Shift Register Optimization
[13:41:42] Phase 6 Post Processing Netlist
```

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[13:42:12] Phase 2.1.1.7 PBP: Add part constraints
[13:42:12] Phase 2.2 Update Timing before SLR Path Opt
[13:42:12] Phase 2.3 Post-Processing in Floorplanning
[13:42:12] Phase 2.4 Global Placement Core
[13:42:12] Phase 2.4.1 UpdateTiming Before Physical Synthesis
[13:42:12] Phase 2.4.2 Physical Synthesis In Placer
[13:42:12] Phase 3 Detail Placement
[13:42:12] Phase 3.1 Commit Multi Column Macros
[13:42:12] Phase 3.2 Commit Most Macros & LUTRAMs
[13:42:12] Phase 3.3 Small Shape DP
[13:42:12] Phase 3.3.1 Small Shape Clustering
[13:42:12] Phase 3.3.2 Flow Legalize Slice Clusters
[13:42:12] Phase 3.3.3 Slice Area Swap
[13:42:12] Phase 3.3.3.1 Slice Area Swap Initial
[13:42:42] Phase 3.4 Re-assign LUT pins
[13:42:42] Phase 3.5 Pipeline Register Optimization
[13:42:42] Phase 4 Post Placement Optimization and Clean-Up
[13:42:42] Phase 4.1 Post Commit Optimization
[13:42:42] Phase 4.1.1 Post Placement Optimization
[13:42:42] Phase 4.1.1.1 BUFG Insertion
[13:42:42] Phase 1 Physical Synthesis Initialization
[13:42:42] Phase 4.1.1.2 Post Placement Timing Optimization
[13:42:42] Phase 4.2 Post Placement Cleanup
[13:42:42] Phase 4.3 Placer Reporting
[13:42:42] Phase 4.3.1 Print Estimated Congestion
[13:42:42] Phase 4.4 Final Placement Cleanup
[13:42:42] Finished 4th of 6 tasks (FPGA logic placement). Elapsed time:
00h 01m 00s

[13:42:42] Starting logic routing..
[13:42:42] Phase 1 Build RT Design
[13:42:42] Phase 2 Router Initialization
[13:42:42] Phase 2.1 Fix Topology Constraints
[13:42:42] Phase 2.2 Pre Route Cleanup
[13:42:42] Phase 2.3 Global Clock Net Routing
[13:43:12] Phase 2.4 Update Timing
[13:43:12] Phase 3 Initial Routing
[13:43:12] Phase 3.1 Global Routing
[13:43:12] Phase 4 Rip-up And Reroute
[13:43:12] Phase 4.1 Global Iteration 0
[13:43:42] Phase 4.2 Global Iteration 1
[13:43:42] Phase 5 Delay and Skew Optimization
[13:43:42] Phase 5.1 Delay CleanUp
[13:43:42] Phase 5.1.1 Update Timing
[13:43:42] Phase 5.1.2 Update Timing
[13:44:12] Creating bitmap...
```

```
[13:44:12] Phase 5.2 Clock Skew Optimization
[13:44:12] Phase 6 Post Hold Fix
[13:44:12] Phase 6.1 Hold Fix Iter
[13:44:12] Phase 6.1.1 Update Timing
[13:44:12] Phase 7 Route finalize
[13:44:12] Phase 8 Verifying routed nets
[13:44:12] Phase 9 Depositing Routes
[13:44:12] Phase 10 Resolve XTalk
[13:44:12] Phase 11 Route finalize
[13:44:12] Phase 12 Post Router Timing
[13:44:12] Finished 5th of 6 tasks (FPGA routing). Elapsed time: 00h 01m
30s

[13:44:12] Starting bitstream generation..
[13:44:12] Phase 13 Post-Route Event Processing
Check VPL, containing 6 checks, has run: 0 errors
[13:44:15] Run vpl: Step impl: Completed
[13:44:15] Writing bitstream ./vcs3_dpu_wrapper.bit...
[13:44:15] Finished 6th of 6 tasks (FPGA bitstream generation). Elapsed
time: 00h 00m 02s
[13:44:15] Run vpl: FINISHED. Run Status: impl Complete!
INFO: [v++ 60-1441] [13:44:15] Run run_link: Step vpl: Completed
Time (s): cpu = 00:00:02 ; elapsed = 00:06:29 . Memory (MB): peak =
449.574 ; gain = 0.000 ; free physical = 20090 ; free virtual = 43164
INFO: [v++ 60-1443] [13:44:15] Run run_link: Step rtdgen: Started
INFO: [v++ 60-1453] Command Line: rtdgen
INFO: [v++ 60-1454] Run Directory: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/run_link
INFO: [v++ 60-1453] Command Line: cf2sw -a /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/int/address_map.xml -sdsl
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/sdsl.dat -xclbin
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/xclbin_orig.xml -rtd
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/dpu.rtd -o
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/dpu.xml
INFO: [v++ 60-1652] Cf2sw returned exit code: 0
INFO: [v++ 60-1441] [13:44:15] Run run_link: Step rtdgen: Completed
Time (s): cpu = 00:00:00.6 ; elapsed = 00:00:00.64 . Memory (MB): peak =
449.574 ; gain = 0.000 ; free physical = 20079 ; free virtual = 43153
INFO: [v++ 60-1443] [13:44:15] Run run_link: Step xclbinutil: Started
INFO: [v++ 60-1453] Command Line: xclbinutil --add-section
```

```
BITSTREAM:RAW:/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/link/int/system.bit --
force --target hw --key-value SYS:dfx_enable:false --add-section
:JSON:/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/link/int/dpu.rtd --add-section
CLOCK_FREQ_TOPOLOGY:JSON:/home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/int/dpu_xml.rtd --add-section
BUILD_METADATA:JSON:/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/link/int/dpu_build.rtd -
-add-section EMBEDDED_METADATA:RAW:/home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/int/dpu.xml --add-section
SYSTEM_METADATA:RAW:/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/int/systemDiagramModelSlrBaseAddress.json --key-
value SYS:PlatformVBNV:xilinx_vcs-3_sundance_vcs3_platform_0_0 --output
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/dpu.xclbin
INFO: [v++ 60-1454] Run Directory: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/run_link
XRT Build Version: 2.14.354 (2022.2)
       Build Date: 2022-10-08 09:49:53
          Hash ID: 43926231f7183688add2dccfd391b36a1f000bea
Creating a default 'in-memory' xclbin image.

Section: 'BITSTREAM'(0) was successfully added.
Size   : 5568789 bytes
Format : RAW
File   : '/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/link/int/system.bit'

Section: 'MEM_TOPOLOGY'(6) was successfully added.
Format : JSON
File   : 'mem_topology'

Section: 'IP_LAYOUT'(8) was successfully added.
Format : JSON
File   : 'ip_layout'

Section: 'CONNECTIVITY'(7) was successfully added.
Format : JSON
File   : 'connectivity'
WARNING: Skipping CLOCK_FREQ_TOPOLOGY section for count size is zero.
WARNING: Section 'CLOCK_FREQ_TOPOLOGY' content is empty.  No data in the
```

```
given JSON file.

Section: 'CLOCK_FREQ_TOPOLOGY'(11) was empty.  No action taken.
Format : JSON
File   : '/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/link/int/dpu_xml.rtd'

Section: 'BUILD_METADATA'(14) was successfully added.
Size   : 4594 bytes
Format : JSON
File   : '/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/link/int/dpu_build.rtd'

Section: 'EMBEDDED_METADATA'(2) was successfully added.
Size   : 4540 bytes
Format : RAW
File   : '/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/link/int/dpu.xml'

Section: 'SYSTEM_METADATA'(22) was successfully added.
Size   : 18512 bytes
Format : RAW
File   : '/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/int/systemDiagramModelSlrBaseAddress.json'
Successfully wrote (5607918 bytes) to the output file:
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/dpu.xclbin
Leaving xclbinutil.
INFO: [v++ 60-1441] [13:44:15] Run run_link: Step xclbinutil: Completed
Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.05 . Memory (MB): peak =
449.574 ; gain = 0.000 ; free physical = 20065 ; free virtual = 43144
INFO: [v++ 60-1443] [13:44:15] Run run_link: Step xclbinutilinfo: Started
INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/dpu.xclbin.info --input
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/dpu.xclbin
INFO: [v++ 60-1454] Run Directory: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/run_link
INFO: [v++ 60-1441] [13:44:16] Run run_link: Step xclbinutilinfo:
Completed
Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.07 . Memory (MB): peak =
449.574 ; gain = 0.000 ; free physical = 20054 ; free virtual = 43134
INFO: [v++ 60-1443] [13:44:16] Run run_link: Step generate_sc_driver:
```

```
Started
INFO: [v++ 60-1453] Command Line:
INFO: [v++ 60-1454] Run Directory: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/link/run_link
INFO: [v++ 60-2442] Software platform is not available, OS name is set
from advanced.param 'software.os': linux
INFO: [v++ 60-2442] Software platform is not available, CPU type is set
internally based on part name and design intent from hardware platform:
cortex-a53
INFO: [v++ 60-1441] [13:44:16] Run run_link: Step generate_sc_driver:
Completed
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak =
449.574 ; gain = 0.000 ; free physical = 20054 ; free virtual = 43134
Check POST-VPL, containing 1 checks, has run: 0 errors
INFO: [v++ 60-244] Generating system estimate report...
INFO: [v++ 60-1092] Generated system estimate report:
/home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/reports/link/system_estimate_dpu.xtxt
INFO: [v++ 60-2397] Platform default or user specified output type sd_card
detected but is not a supported output for v++ --link. Use the v++ --
package option instead to create SD card output.
INFO: [v++ 60-586] Created /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/dpu.xclbin
INFO: [v++ 60-1307] Run completed. Additional information can be found in:
      Guidance: /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/reports/link/v++_link_dpu_guidance.html
      Timing Report: /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/reports/link/imp/impl_1_vcs3_dpu_wrapper_timing_summa
ry_routed.rpt
      Vivado Log: /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/logs/link/vivado.log
      Steps Log File: /home/sundance/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards/vcs-
3/binary_container_1/logs/link/link.steps.log

INFO: [v++ 60-2343] Use the vitis_analyzer tool to visualize and navigate
the relevant reports. Run the following command.
    vitis_analyzer /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-
PYNQv3.5/DPU-PYNQ/boards/vcs-3/binary_container_1/dpu.xclbin.link_summary
INFO: [v++ 60-791] Total elapsed time: 0h 6m 44s
INFO: [v++ 60-1653] Closing dispatch client.
cp -f /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
```

```
PYNQ/boards/vcs-
3/binary_container_1/link/vivado/vpl/prj/prj.gen/sources_1/bd/*/hw_handoff
/*.hwh \
      /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/dpu.hwh
cp -f /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-
3/binary_container_1/link/vivado/vpl/prj/prj.runs/impl_1/*.bit \
      /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/dpu.bit
cp -f /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/binary_container_1/dpu.xclbin \
      /home/sundance/sundance/VCS-3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-
PYNQ/boards/vcs-3/dpu.xclbin
sundance@sundance-Amd-Am5-Workstation:~/sundance/VCS-
3/vcs_base/VCS_3_DPU/DPU-PYNQv3.5/DPU-PYNQ/boards$
```