Hyperspectral Processing Using FPGAs and DSPs

As focal-plane technology advances, it becomes increasingly practical to reduce the size and increase the portability of remote-sensing instruments. To achieve smaller and more portable instruments, supporting electronics hardware and computing elements must similarly decrease in scale and power consumption, while also increasing in computing ability to meet new real-time processing (RTP) needs. To meet the packaging, power, and processing (P3) requirements, RTP systems will need to be assembled using combinations of field-programmable gate arrays (FPGAs) and digital signal processing (DSP) processors rather than bulky, expensive, and less efficient general purpose computing devices.

Project Goals

Our FY2005 goals include the following:

1. evaluate processing requirements to perform covariance estimation, eigenfactorization, and matched filtering (L3 processing) hyperspectral data processing;
2. build a controller to archive data and operate the A/D and DSP components using a single board computer;
3. build a prototype to digitize at least four channels of analog information clocked off a hyperspectral focal-plane array, and process the data prior to L3 by performing bad-pixel correction and spectral calibration (L1 processing);
4. build a prototype that performs real-time hyperspectral data processing from a complete data cube through one or more algorithms selected from the L1 and L3 processing chains.

Relevance to LLNL Mission

This project will provide engineering experience in small scale, low-power, low-cost, RTP systems for hyperspectral imagery, which can be extended to any complex

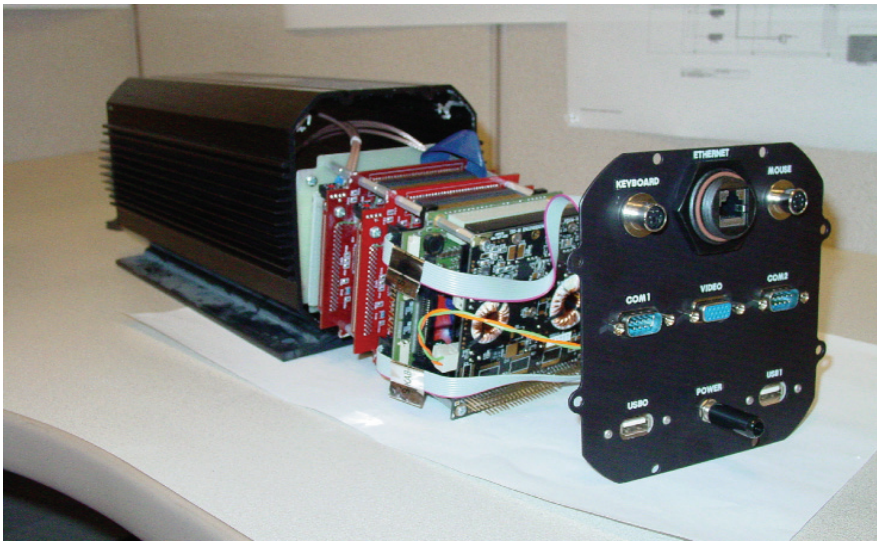

Figure 1. Hardware for hyperspectral embedded processing system.

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mathematical problem where P3 requirements are key. This project will also result in a package that can be used for any application that digitizes analog input and can benefit from processing the resulting data in real-time. An added benefit is that this technology will be used to increase the efficiency of automated, non-real-time ground data processing of hyperspectral data.

FY2005 Accomplishments and Results

Figures 1 and 2 show some of the hardware for the hyperspectral embedded processing system. We achieved four major milestones this year. First, using EDMA and compiler optimization techniques, we increased the performance of the covariance matrix calculation 300%. The speed and performance is comparable to a generalized CPU with I/O bandwidth still the limiting factor. Second, we refined a covariance matrix algorithm and segmented the calculation into two parts, to divide the workload between the two DSP processors. By exploiting the linearity of the calculation and distributing the workload, performance was improved another 30%. Third, we achieved a reduction of FPGA fabric use by moving memory storage from flip-flops and combinatorial logic to on-board block RAM available on Xilinx Virtex II FPGAs. Fourth, we simplified the VHDL coding by using Mentor Graphics FPGA Advantage tools.

Covariance matrix generation is required for background estimation prior to performing matched filtering and identification in L3 processing of hyperspectral data. This computation requires a significant number of memory accesses and this has been the largest bottleneck in using conventional DSP chips. While performance improved some 330% over FY2004 performance, the DSP is still too slow to perform full-frame processing in real-time. A parallel project using graphics processors to perform L3 processing demonstrated performance that would meet RTP requirements.

The pervasiveness of high-definition television and streaming video has created a large demand for fixed-point processing. Until DSP manufacturers improve input/output performance of floating-point chips, it appears the graphics processor market is more suitable for this type of RTP.

Related References

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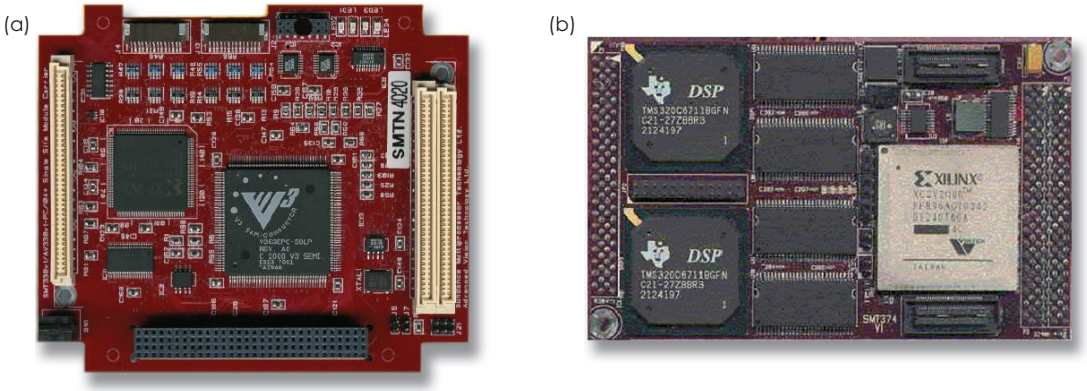

Figure 2. (a) Sundance PC-104+ carrier board, and (b) Sundance dual TI 6713 DSP module.