



FC203A - Power Spectrum Extraction/Exchange FPGA Core

User's Guide

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DOCUMENT HISTORY

Date	Initials	Revision	Description of Change
19-Feb-07	FH	0.0	Initial Release for Internal Review
2-Apr-07	FH	0.1	SPAN is now size of burst on each output stream
3-Apr-07	FH	0.2	Input is always ready, output must be too
5-Apr-07	FH	0.3	Fixed table 3
8-Apr-07	FH	0.5	Added resource Info



Table of Contents

1. GENERAL DESCRIPTION	4
2. I/O DESCRIPTION.....	5
3. PRESENTATION	8
4. USAGE.....	8
5. VERIFICATION.....	10
6. DELIVERABLES	11
7. LICENSING AND PROPERTY RIGHTS	11
8. ORDERING INFORMATION	11

Table of Figures

Figure 1 – FC203A Component Diagram.....	4
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1. GENERAL DESCRIPTION

The FC203A - Power Spectrum Extraction/Exchange FPGA module is an efficient implementation of a general table “chop/swap” operation, specifically designed for use in front of the FC203B Power Spectrum Interleave module. A control word defines how many input samples are to be passed through to the output, and the low-order half of those samples are passed to one output while the high-order samples are passed to the second output. The high/low division may optionally be exchanged by asserting a bit in the control word.

In order for it to be used within a Diamond/FPGA system, the I/O interfaces are ‘standardized’ to the model described by Diamond¹.

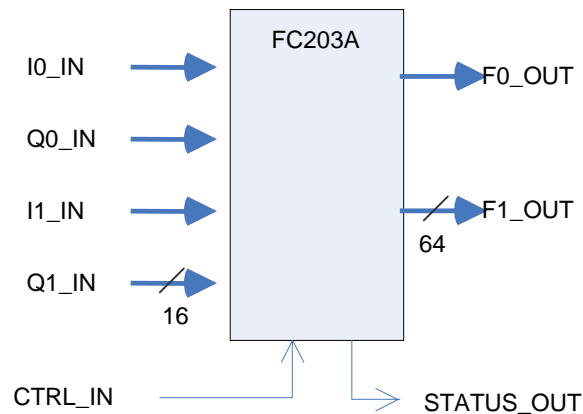


Figure 1 – FC203A Component Diagram

¹ See: <http://www.3l.com/Diamond/Documentation/Diamond.pdf> (Chapter 28, “FPGA Tasks”)



2. I/O DESCRIPTION

The FC203A component presents as a pure-FPGA ‘task’, and implements the following interface:

Port Name	Channel	Valid Width	Direction	Description
I0_IN, I1_IN	0, 2	16	Input	In-Phase Component, frequency-domain data (2 channels)
Q0_IN, Q1_IN	1, 3	16	Input	Quadrature Component, frequency-domain data (2 channels)
CTRL_IN	4	32	Input	Control Word
F0_OUT, F1_OUT	0, 1	64	Output	In-phase/Quadrature components, 2-channels each
STATUS_OUT	2	32	Output	Pass-through control/status

Table 1 –FC203A Interfaces

Additional port descriptions are provided below:

I0 IN.. I1 IN

There are two input ports for in-phase frequency domain streams. Data values are pairs of 16-bit extended twos-complement as described in the FC108 User Manual, although the extended sign value in bits 16-31 is ignored. These ports are suitable for connecting to the FC108-D’s I_OUT ports.

Q0 IN.. Q1 IN

There are two input ports for the quadrature frequency streams. Data values are pairs of 16-bit extended twos-complement as described in the FC108 User Manual. These ports are suitable for connecting to the FC108-D’s Q_OUT ports.

NOTE: In agreement with the implementation of FC108, the input ports xn_IN are always “ready” when any enable bit is set. To avoid the need for buffering in this module the downstream data sinks must also be ready whenever this module has data to write. A FIFO may be required at the output of this module to insure this.

NOTE: For simplicity, it is assumed that all four input channels (or the active subset) will “write” at the same time. If this does not occur then the FC203A’s bin count will be in error on some channels. There is currently no way to detect or report this condition.

CTRL IN

Control miscellaneous parameters and features of the FC203A subcomponent. The port accepts data one 32-bit word at a time.

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Signal	Bits	Mode	Description
m	3..lsb	R/W	Configure m for input streams
LOW_FREQ	15..4	R/W	Select lowest frequency bin
SPAN	25..16	R/W	Select number of active frequency bins
EXCHANGE	26	R/W	Enable high/low exchange
RESERVED	27	R/W	Pass-through (reserved)
ENABLE	msb..28	R/W	Output/function enable

Table 2 - FC203A Control Word

The FC203A sub-component ignores some of the bits in the control word; they exist to enable the configuration of multiple modules (including FC203B) in a daisy-chain manner.

‘m’ determines the number of raw frequency component samples that are accepted at the Ix_IN and Qx_IN ports to make up one frame. The relation between the frame size M and the control word value ‘m’ is $M=2^m$. After M samples are received on each input the internal count of bin number is reset to zero. The maximum value of m is 12, corresponding to 4096 samples per frame.

LOW_FREQ determines the frequency bin offset (from 0) which determines the start of the spectral sampling on each of the input samples. All bins up to but not including LOW_FREQ are discarded. If LOW_FREQ is zero, then no samples are discarded initially.

SPAN determines the number of frequency bins that will be passed along to each of the FC203A outputs. Both F0_OUT and F1_OUT will receive SPAN samples on each frame. $LOW_FREQ + 2 * SPAN$ must be less than M or the results will be undefined. SPAN is ten bits in size, a value of zero indicates the maximum 1024 samples will be passed.

EXCHANGE determines if a spectral exchange of the low vs. high frequencies will be performed on the streams. Low frequency bins are in the range $[LOW_FREQ, LOW_FREQ + SPAN - 1]$. High frequency bins are in the range $[LOW_FREQ + SPAN, LOW_FREQ + 2 * SPAN - 1]$. If EXCHANGE is zero, the low-frequency bins are passed to F0_OUT. If EXCHANGE is one, the low-frequency bins are passed to F1_OUT.

ENABLE will cause the module to generate data on its output (F0_OUT, F1_OUT) ports if any of the four bits are non-zero.

NOTE: To simplify the FPGA logic, the control word is assumed to be static while the module is enabled. Changes to m, LOW_FREQ, SPAN, or EXCHANGE while any ENABLE bit is set may result in unpredictable output.

F0 OUT, F1 OUT

These are dual-channel partitioned frequency data ports. Data values are groups of 64-bit values in bursts of SPAN qwords. The 64-bit values consist of the in-phase and quadrature components (16-bit two’s complement as described in the FC108 User Manual) of two channels. This port is suitable for connecting to the Fx_IN ports of the FC203B subcomponent.

Bit 15..0	I0(0)	I0(1)	...	I0(SPAN - 1)
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Bit 31..16	Q0(0)	Q0(1)	...	Q0(SPAN - 1)
Bit 47..32	I1(0)	I1(1)	...	I1(SPAN - 1)
Bit 63..48	Q1(0)	Q1(1)	...	Q1(SPAN - 1)

Table 3 – Stream Format of Fx_OUT Port, low-frequency channel, LOW_FREQ = 0

STATUS_OUT

The module control/status word is driven on this channel; in this case all bits are passed unchanged. This register may be read at any time, not just when a new control value has been written. This port is suitable for connecting to a HOST port for the purpose of system state feedback or to another FC203A or FC203B sub-component for daisy-chained configuration.



3. PRESENTATION

The firmware module is instantiated in a Diamond/FPGA configuration file as follows:

```
FC203A\  
+---analysis\           Implementation Analysis  
+---fc203a\             Task Source Code  
+---specifications\  
  \---test\             Verification Test Benches
```

Users of the FC203A firmware module will reference the Diamond .fcd file (top level) from the fc203a\ above.

4. USAGE

The firmware module is instantiated in a Diamond/FPGA configuration file as follows:

```
! declare tasks  
!  
task chop0      ins=5 outs=3  file="..\fc203a\fc203a.fcd"  
!  
! place tasks on FPGA  
!  
place chop0    <fpga>  
!  
! connect dataflow  
!  
connect ? <user_1>[w]    chop0[0]  
connect ? <user_1>[x]    chop0[1]  
connect ? <user_1>[y]    chop0[2]  
connect ? <user_1>[z]    chop0[3]  
connect ? <user_cfg>[n]  chop0[4]  
connect ? chop0[0]      <user_2>[a]  
connect ? chop0[1]      <user_3>[b]  
connect ? chop0[2]      <user_stat>[c]
```

Where <user_1> is a four-channel data source, <user_2> and <user_3> are data-sink tasks, and <user_stat> is a status-sink task. <user_cfg> is a connection which supplies the 32-bit configuration control word.



In some cases, it is useful to provide some amount of elastic buffering before or after the FC203A task in order to help close timing in the FPGA design. This can be accomplished as follows:

```
! declare tasks
!
task fifo1      ins=1 outs=1   file="..\fifo\fifo8.fcd"
task chop0     ins=5 outs=3   file="..\fc203a\fc203a.fcd"
task fifo2     ins=1 outs=1   file="..\fifo\fifo8.fcd"
!
! place tasks on FPGA
!
place fifo1    <fpga>
place chop0   <fpga>
place fifo2   <fpga>
!
! connect dataflow
!
connect C1     <user_1>[x]     fifo1[0]
connect ?     fifo1[0]       chop0[0]
! ...repeat for other inputs...
connect C2     <user_cfg>[y]   chop0[4]
connect ?     chop0[0]       fifo2[0]
connect C3     fifo2[0]       <user_2>[z]
! ...repeat for other outputs...
```

Note: *When implementing on some FPGA devices, a slower clock may be needed.*

In order to close timing on some (slow) FPGA device/speed grades, the task may need to run under a slower clock. To do this, use Diamond's facility to generate a custom clock, and provide this clock to each FC203A instance.

See the 3L/Diamond User Guide v3.1.3 pg. 306 for additional details.

For example:

```
! Use a slower clock for the UUT
!
clock slow processor=<fpga> source=DEFAULT output=50MHz
!
! place tasks on FPGA
!
place chop0    <fpga>      clock=slow
```



5. VERIFICATION

The firmware module will be supported by two types of test benches. In all cases, compilation is performed using `gmake` (distributed with CCS3.0 or greater)².

Unit Test Benches

A C- Reference Model is implemented as a Diamond/DSP Task. This model is not yet implemented as of this revision.

Resource and Performance Analysis Benches

A mechanism to obtain the resource utilization of the FC203A core is provided. The basic principle is to generate a “baseline” implementation of the target FPGA that contains a ‘stub’. The ‘stub’ has all the same inputs and outputs, but is a trivial implementation of the FPGA task. This “baseline” is compared to a real instantiation of the FC203A module. The stub FPGA task is provided as ‘FC203A\FC203A_base.fcd’.

Comparing the two MAP report files and subtracting the Slices, BRAM and MPY in use provides an accurate real-world estimate of the resources used by the FC203A module.

Finally, Diamond application configuration files are provided which enable the FC203A module to be instantiated into a supported single (stand-alone) FPGA board. By connecting the dataflow inputs of the FC203A to SDB resources, and the CTRL_IN to the default Comport (CP3, typically) resource, a hardware reference is created which can be added to any system and operated at line rate.

The configuration files and makefile for accomplishing these are provided in the `analysis\` folder.

MODULE	FPGA	Slices	BRAM	MPY	F _{MAX} (MHz)	Notes
SMT348-10	XC4VSX55-10	110	0	0	262	
SMT365-8-1	XC2V1000-4	108	0	0	172	
SMT368-10	XC4VSX35-10	110	0	0	262	
SMT368-12	XC4VSX35-12	110	0	0	331	
SMT398-8000	XC2V8000-4	108	0	0	172	
SMT398-VP70	XC2VP70-6	100	0	0	227	
SMT417	XC2VP50-5	99	0	0	202	

Table 4 –FC203A Performance Estimates and Resource Utilization

The results in table 4 are estimates only, based on very lightly-loaded FPGA configurations. Some trade-off between slice usage and speed is possible depending on synthesis and fitting options. Exceeding F_{MAX} may cause logic errors and unexpected results, which can be exceedingly hard to debug. It is the system designer’s responsibility to avoid this condition.

² Only `gmake` has the necessary syntax to effectively implement the build system. Contact Sundance DSP for assistance if your installation lacks CCS.



6. DELIVERABLES

FC203A is a complete Diamond/FPGA firmware module that includes:

- Firmware source (.vhd) files
- Diamond/FPGA integration support (.fcd, _pkg.vhd) and example implementations
- VHDL Module-level testbench (included with FC203B)
- C Simulation harness [*NOTE: Not available in Release 0.1*]
- Matlab analysis tools [*NOTE: Not available in Release 0.1*]
- User Guide

7. LICENSING AND PROPERTY RIGHTS

Sundance DSP retains copyright and licensing rights, and distributes the FC203A firmware module under non-disclosure agreement only. Special arrangements are made on a case-by-case basis.

All customers need to purchase support contracts from Sundance DSP in order to be able to obtain updates and technical support for the FC203A firmware module.

For support, please register on <http://support.sundancedsp.com> and post all questions on the forum. You can also contact any of Sundance offices, around the world, by telephone or email. For details, please see the Sundance web site at <http://www.sundancedsp.com>

8. ORDERING INFORMATION

The FC203A component may be ordered separately, or bundled with any other package containing multiple products. Contact Sundance DSP for specific details.