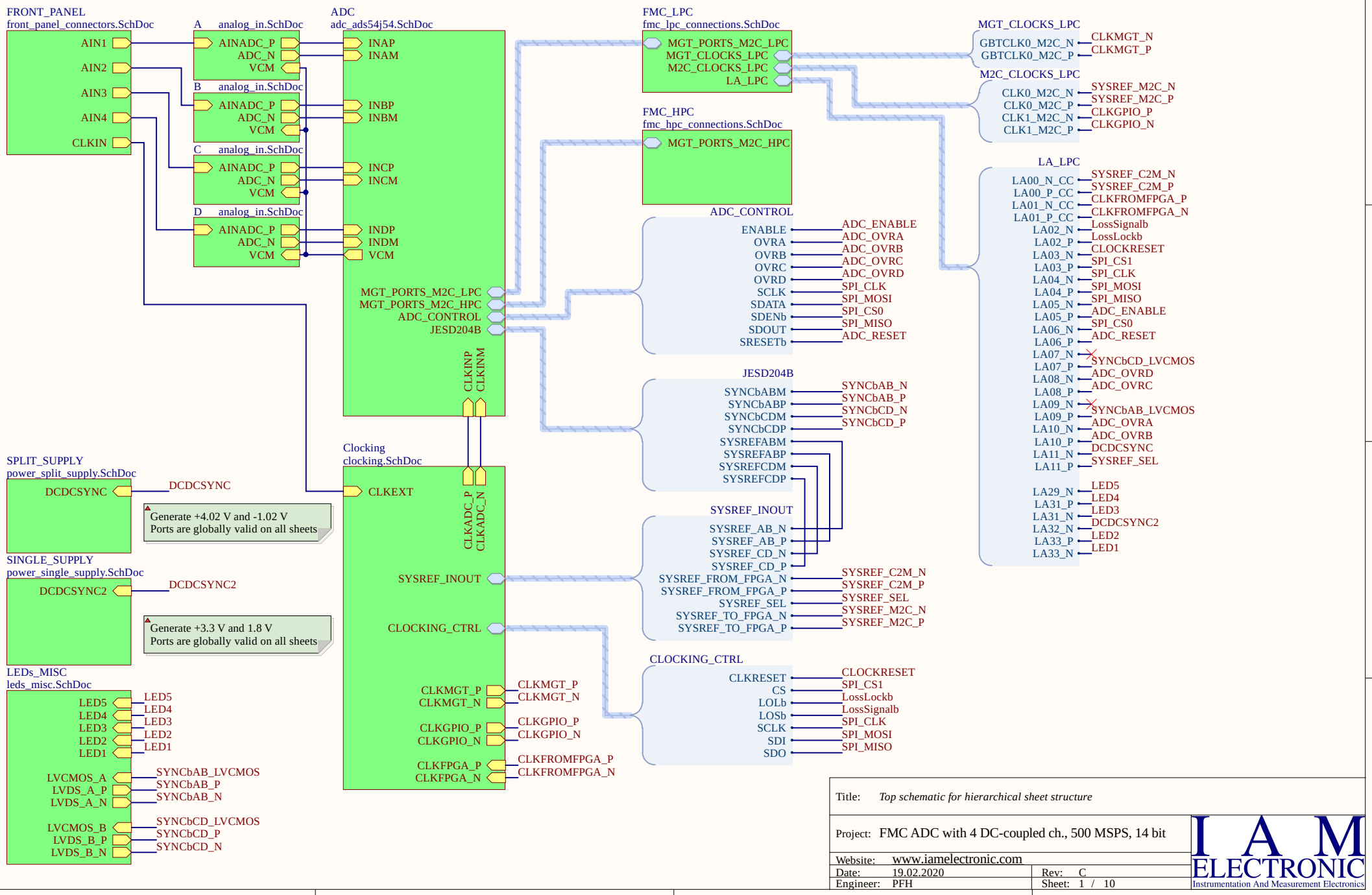
FRONT_PANEL
front_panel_connectors.SchDoc
AIN1
AIN2
AIN3
AIN4
CLKIN
A analog_in.SchDoc
AINADC_P
ADC_N
VCM
B analog_in.SchDoc
C analog_in.SchDoc
D analog_in.SchDoc
ADC
adc_ads54j54.SchDoc
INAP
INAM
INBP
INBM
INCP
INCM
INDP
INDM
VCM
MGT_PORTS_M2C_LPC
MGT_PORTS_M2C_HPC
ADC_CONTROL
JESD204B
CLKINP
CLKINM
FMC_LPC
fmc_lpc_connections.SchDoc
MGT_CLOCKS_LPC
M2C_CLOCKS_LPC
LA_LPC
FMC_HPC
fmc_hpc_connections.SchDoc
MGT_PORTS_M2C_HPC
MGT_CLOCKS_LPC
GBTCLK0_M2C_N
GBTCLK0_M2C_P
CLKMGT_N
CLKMGT_P
M2C_CLOCKS_LPC
CLK0_M2C_N
CLK0_M2C_P
CLK1_M2C_N
CLK1_M2C_P
SYSREF_M2C_N
SYSREF_M2C_P
CLKGPIO_P
CLKGPIO_N
LA_LPC
LA00_N_CC
LA00_P_CC
LA01_N_CC
LA01_P_CC
LA02_N
LA02_P
LA03_N
LA03_P
LA04_N
LA04_P
LA05_N
LA05_P
LA06_N
LA06_P
LA07_N
LA07_P
LA08_N
LA08_P
LA09_N
LA09_P
LA10_N
LA10_P
LA11_N
LA11_P
LA29_N
LA31_P
LA31_N
LA32_N
LA33_P
LA33_N
SYSREF_C2M_N
SYSREF_C2M_P
CLKFROMFPGA_P
CLKFROMFPGA_N
LossSignalb
LossLockb
CLOCKRESET
SPI_CS1
SPI_CLK
SPI_MOSI
SPI_MISO
ADC_ENABLE
SPI_CS0
ADC_RESET
SYNCbCD_LVCMOS
ADC_OVRD
ADC_OVRC
SYNCbAB_LVCMOS
ADC_OVRA
ADC_OVRB
DCDCSYNC
SYSREF_SEL
LED5
LED4
LED3
DCDCSYNC2
LED2
LED1
ADC_CONTROL
ENABLE
OVRA
OVRB
OVRC
OVRD
SCLK
SDATA
SDENb
SDOUT
SRESETb
JESD204B
SYNCbABM
SYNCbABP
SYNCbCDM
SYNCbCDP
SYSREFABM
SYSREFABP
SYSREFCDM
SYSREFCDP
SYNCbAB_N
SYNCbAB_P
SYNCbCD_N
SYNCbCD_P
SYSREF_INOUT
SYSREF_AB_N
SYSREF_AB_P
SYSREF_CD_N
SYSREF_CD_P
SYSREF_FROM_FPGA_N
SYSREF_FROM_FPGA_P
SYSREF_TO_FPGA_N
SYSREF_TO_FPGA_P
SYSREF_C2M_N
SYSREF_C2M_P
SYSREF_SEL
SYSREF_M2C_N
SYSREF_M2C_P
CLOCKING_CTRL
CLKRESET
CS
LOLb
LOSb
SCLK
SDI
SDO
CLOCKRESET
SPI_CS1
LossLockb
LossSignalb
SPI_CLK
SPI_MOSI
SPI_MISO
Clocking
clocking.SchDoc
CLKEXT
CLKADC_P
CLKADC_N
SYSREF_INOUT
CLOCKING_CTRL
CLKMGT_P
CLKMGT_N
CLKGPIO_P
CLKGPIO_N
CLKFPGA_P
CLKFPGA_N
SPLIT_SUPPLY
power_split_supply.SchDoc
DCDCSYNC
Generate +4.02 V and -1.02 V
Ports are globally valid on all sheets
SINGLE_SUPPLY
power_single_supply.SchDoc
DCDCSYNC2
Generate +3.3 V and 1.8 V
Ports are globally valid on all sheets
LEDs_MISC
leds_misc.SchDoc
LED5
LED4
LED3
LED2
LED1
LVCMOS_A
LVDS_A_P
LVDS_A_N
SYNCbAB_LVCMOS
SYNCbAB_P
SYNCbAB_N
LVCMOS_B
LVDS_B_P
LVDS_B_N
SYNCbCD_LVCMOS
SYNCbCD_P
SYNCbCD_N
Title: Top schematic for hierarchical sheet structure
Project: FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website: www.iamelectronic.com
Date: 19.02.2020
Engineer: PFH
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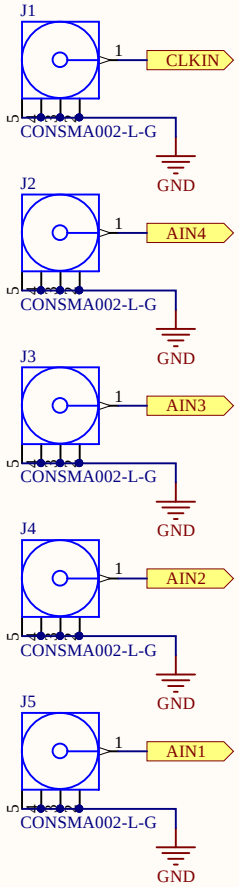
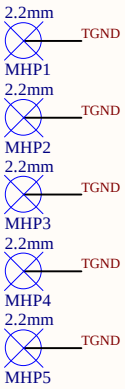
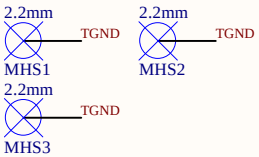
SMA front panel inputs



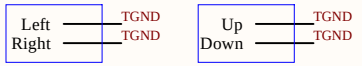
Mounting holes (ruggedized, primary)



Mounting holes (ruggedized, secondary)

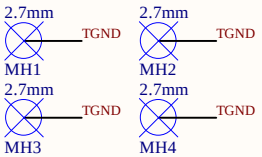


Thermal interfaces (primary and secondary)



Place RT for shorting TGND and GND.
TGND WILL BE NO CURRENT RETURN PATH!

Mounting holes (commercial grade)



Logos on Silkscreen

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Fiducials on Top

Fiducials on Bottom

Title:	*Front panel connectors (5x SMA, mounting holes, thermal interfaces and logos)*
Project:	FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website:	www.iamelectronic.com
Date:	19.02.2020
Rev:	C
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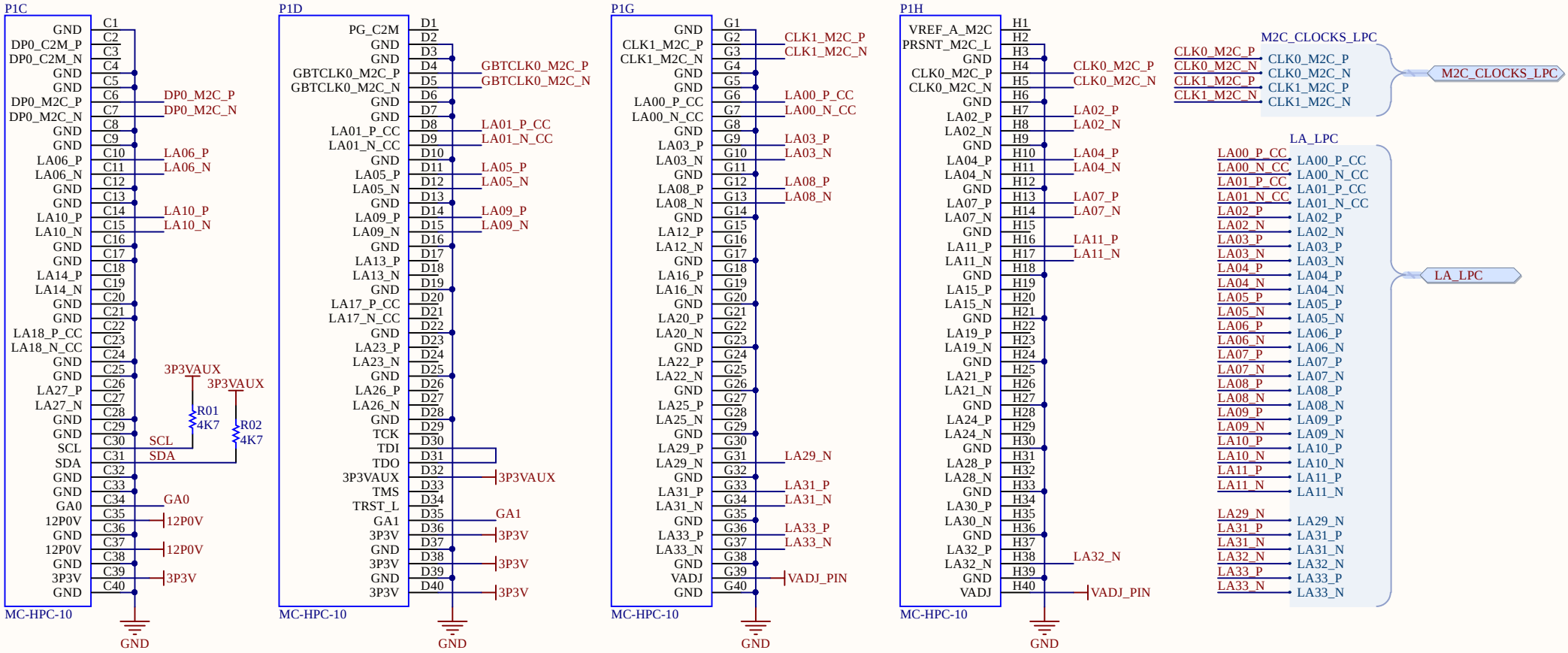
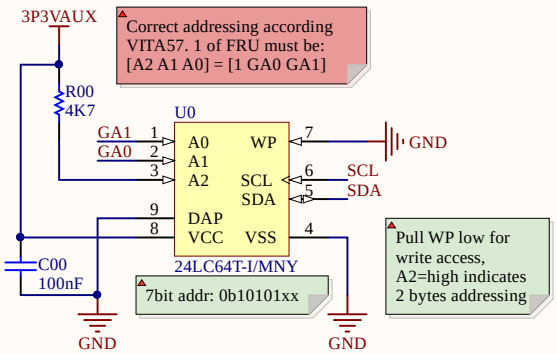
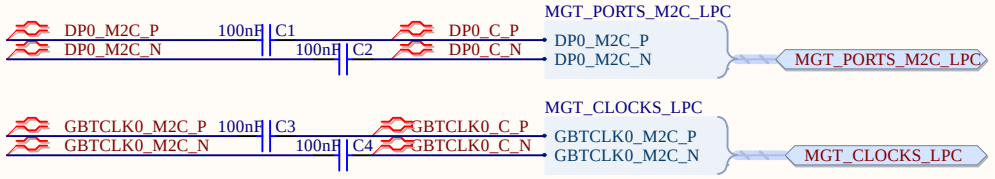
High-pin count (HPC) connector, low-pin count (LPC) only banks



EEPROM for FRU data





Title:	*FMC Connector (LPC pins of HPC connector), EEPROM (FRU) and LEDs*
Project:	FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website:	www.iamelectronic.com
Date:	19.02.2020
Rev:	C
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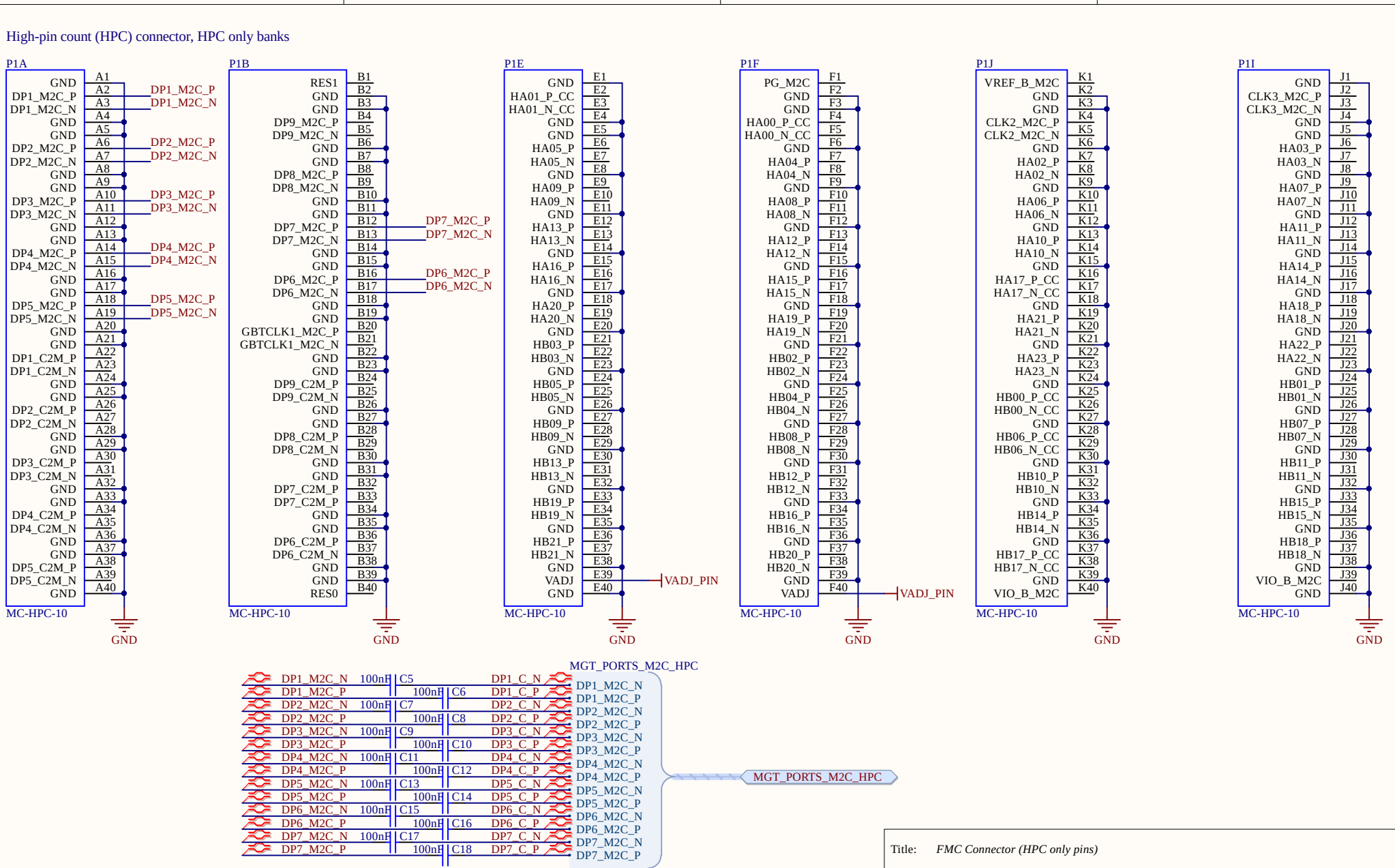
High-pin count (HPC) connector, HPC only banks
P1A
GND A1
DP1_M2C_P A2 DP1_M2C_P
DP1_M2C_N A3 DP1_M2C_N
GND A4
GND A5
GND A6 DP2_M2C_P
DP2_M2C_P A7 DP2_M2C_N
DP2_M2C_N A8
GND A9
GND A10 DP3_M2C_P
DP3_M2C_P A11 DP3_M2C_N
DP3_M2C_N A12
GND A13
GND A14 DP4_M2C_P
DP4_M2C_P A15 DP4_M2C_N
DP4_M2C_N A16
GND A17
GND A18 DP5_M2C_P
DP5_M2C_P A19 DP5_M2C_N
DP5_M2C_N A20
GND A21
GND A22
DP1_C2M_P A23
DP1_C2M_N A24
GND A25
GND A26
DP2_C2M_P A27
DP2_C2M_N A28
GND A29
GND A30
DP3_C2M_P A31
DP3_C2M_N A32
GND A33
GND A34
DP4_C2M_P A35
DP4_C2M_N A36
GND A37
GND A38
DP5_C2M_P A39
DP5_C2M_N A40
GND
MC-HPC-10
GND
P1B
RES1 B1
GND B2
GND B3
DP9_M2C_P B4
DP9_M2C_N B5
GND B6
GND B7
DP8_M2C_P B8
DP8_M2C_N B9
GND B10
GND B11
DP7_M2C_P B12 DP7_M2C_P
DP7_M2C_N B13 DP7_M2C_N
GND B14
GND B15
DP6_M2C_P B16 DP6_M2C_P
DP6_M2C_N B17 DP6_M2C_N
GND B18
GND B19
GBTCLK1_M2C_P B20
GBTCLK1_M2C_N B21
GND B22
GND B23
DP9_C2M_P B24
DP9_C2M_N B25
GND B26
GND B27
DP8_C2M_P B28
DP8_C2M_N B29
GND B30
GND B31
DP7_C2M_P B32
DP7_C2M_P B33
GND B34
GND B35
DP6_C2M_P B36
DP6_C2M_N B37
GND B38
GND B39
RES0 B40
MC-HPC-10
GND
P1E
GND E1
HA01_P_CC E2
HA01_N_CC E3
GND E4
GND E5
HA05_P E6
HA05_N E7
GND E8
HA09_P E9
HA09_N E10
GND E11
HA13_P E12
HA13_N E13
GND E14
HA16_P E15
HA16_N E16
GND E17
HA20_P E18
HA20_N E19
GND E20
HB03_P E21
HB03_N E22
GND E23
HB05_P E24
HB05_N E25
GND E26
HB09_P E27
HB09_N E28
GND E29
HB13_P E30
HB13_N E31
GND E32
HB19_P E33
HB19_N E34
GND E35
HB21_P E36
HB21_N E37
GND E38
VADJ E39 VADJ_PIN
GND E40
MC-HPC-10
GND
P1F
PG_M2C F1
GND F2
GND F3
HA00_P_CC F4
HA00_N_CC F5
GND F6
HA04_P F7
HA04_N F8
GND F9
HA08_P F10
HA08_N F11
GND F12
HA12_P F13
HA12_N F14
GND F15
HA15_P F16
HA15_N F17
GND F18
HA19_P F19
HA19_N F20
GND F21
HB02_P F22
HB02_N F23
GND F24
HB04_P F25
HB04_N F26
GND F27
HB08_P F28
HB08_N F29
GND F30
HB12_P F31
HB12_N F32
GND F33
HB16_P F34
HB16_N F35
GND F36
HB20_P F37
HB20_N F38
GND F39
VADJ F40 VADJ_PIN
MC-HPC-10
GND
P1J
VREF_B_M2C K1
GND K2
GND K3
CLK2_M2C_P K4
CLK2_M2C_N K5
GND K6
HA02_P K7
HA02_N K8
GND K9
HA06_P K10
HA06_N K11
GND K12
HA10_P K13
HA10_N K14
GND K15
HA17_P_CC K16
HA17_N_CC K17
GND K18
HA21_P K19
HA21_N K20
GND K21
HA23_P K22
HA23_N K23
GND K24
HB00_P_CC K25
HB00_N_CC K26
GND K27
HB06_P_CC K28
HB06_N_CC K29
GND K30
HB10_P K31
HB10_N K32
GND K33
HB14_P K34
HB14_N K35
GND K36
HB17_P_CC K37
HB17_N_CC K38
GND K39
VIO_B_M2C K40
MC-HPC-10
GND
P1I
GND J1
CLK3_M2C_P J2
CLK3_M2C_N J3
GND J4
GND J5
HA03_P J6
HA03_N J7
GND J8
HA07_P J9
HA07_N J10
GND J11
HA11_P J12
HA11_N J13
GND J14
HA14_P J15
HA14_N J16
GND J17
HA18_P J18
HA18_N J19
GND J20
HA22_P J21
HA22_N J22
GND J23
HB01_P J24
HB01_N J25
GND J26
HB07_P J27
HB07_N J28
GND J29
HB11_P J30
HB11_N J31
GND J32
HB15_P J33
HB15_N J34
GND J35
HB18_P J36
HB18_N J37
GND J38
VIO_B_M2C J39
GND J40
MC-HPC-10
GND
DP1_M2C_N 100nF C5 DP1_C_N
DP1_M2C_P 100nF C6 DP1_C_P
DP2_M2C_N 100nF C7 DP2_C_N
DP2_M2C_P 100nF C8 DP2_C_P
DP3_M2C_N 100nF C9 DP3_C_N
DP3_M2C_P 100nF C10 DP3_C_P
DP4_M2C_N 100nF C11 DP4_C_N
DP4_M2C_P 100nF C12 DP4_C_P
DP5_M2C_N 100nF C13 DP5_C_N
DP5_M2C_P 100nF C14 DP5_C_P
DP6_M2C_N 100nF C15 DP6_C_N
DP6_M2C_P 100nF C16 DP6_C_P
DP7_M2C_N 100nF C17 DP7_C_N
DP7_M2C_P 100nF C18 DP7_C_P
MGT_PORTS_M2C_HPC
DP1_M2C_N
DP1_M2C_P
DP2_M2C_N
DP2_M2C_P
DP3_M2C_N
DP3_M2C_P
DP4_M2C_N
DP4_M2C_P
DP5_M2C_N
DP5_M2C_P
DP6_M2C_N
DP6_M2C_P
DP7_M2C_N
DP7_M2C_P
MGT_PORTS_M2C_HPC
Title: FMC Connector (HPC only pins)
Project: FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website: www.iamelectronic.com
Date: 19.02.2020
Rev: C
Engineer: PFH
Sheet: 4 / 10
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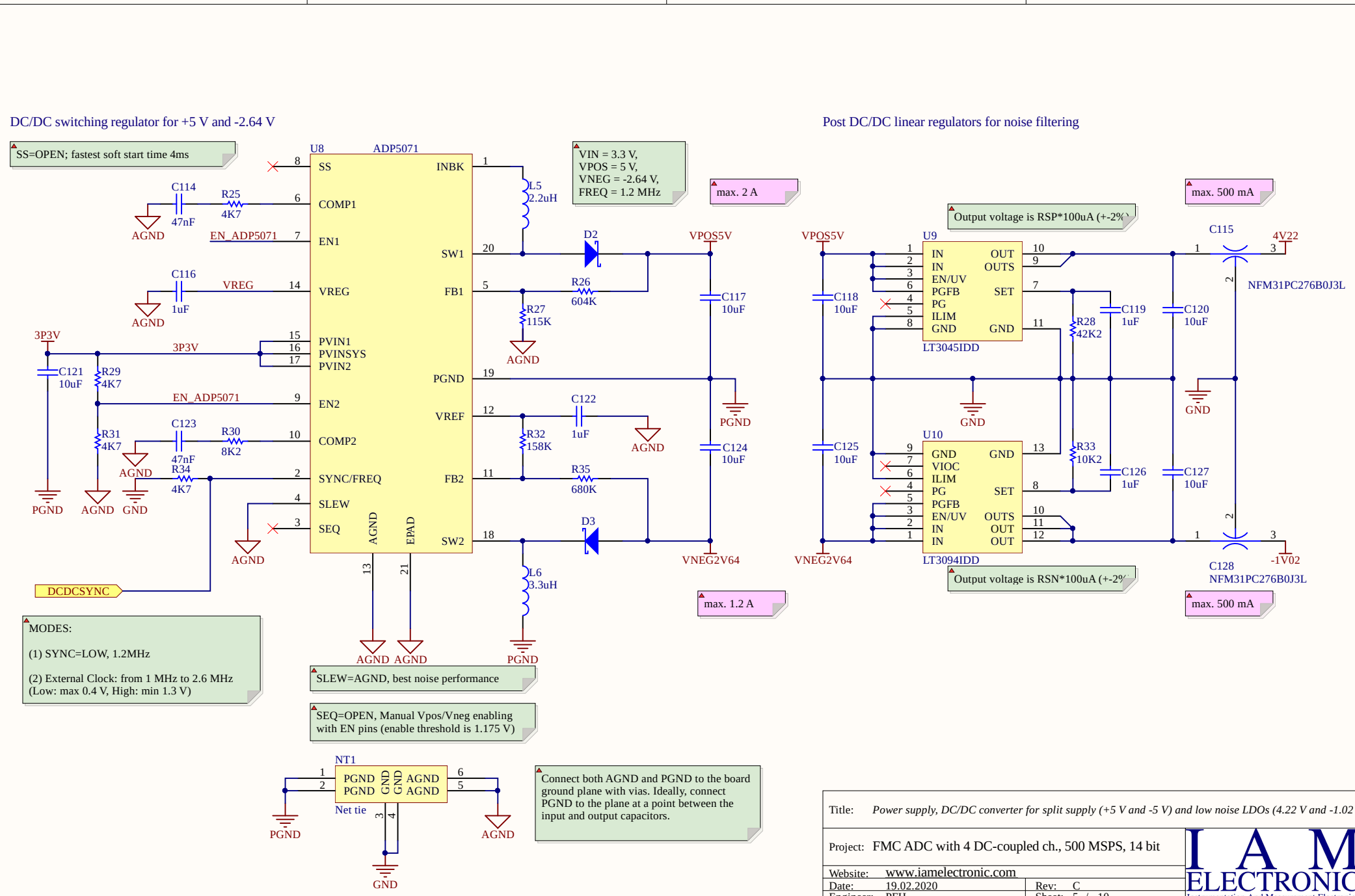
DC/DC switching regulator for +5 V and -2.64 V
Post DC/DC linear regulators for noise filtering
SS=OPEN; fastest soft start time 4ms
U8
ADP5071
SS
COMP1
EN1
VREG
PVIN1
PVINSYS
PVIN2
EN2
COMP2
SYNC/FREQ
SLEW
SEQ
AGND
EPAD
INBK
SW1
FB1
PGND
VREF
FB2
SW2
C114
47nF
R25
4K7
AGND
EN_ADP5071
C116
1uF
VREG
3P3V
C121
10uF
R29
4K7
R31
4K7
C123
47nF
R30
8K2
R34
4K7
GND
DCDCSYNC
VIN = 3.3 V,
VPOS = 5 V,
VNEG = -2.64 V,
FREQ = 1.2 MHz
L5
2.2uH
max. 2 A
D2
VPOS5V
R26
604K
R27
115K
C117
10uF
C122
1uF
R32
158K
C124
10uF
D3
R35
680K
VNEG2V64
L6
3.3uH
max. 1.2 A
MODES:
(1) SYNC=LOW, 1.2MHz
(2) External Clock: from 1 MHz to 2.6 MHz
(Low: max 0.4 V, High: min 1.3 V)
SLEW=AGND, best noise performance
SEQ=OPEN, Manual Vpos/Vneg enabling with EN pins (enable threshold is 1.175 V)
NT1
PGND
AGND
Net tie
Connect both AGND and PGND to the board ground plane with vias. Ideally, connect PGND to the plane at a point between the input and output capacitors.
Output voltage is RSP*100uA (+-2%)
max. 500 mA
U9
LT3045IDD
IN
OUT
EN/UV
PGFB
SET
PG
ILIM
GND
C118
10uF
C119
1uF
C120
10uF
R28
42K2
C115
NFM31PC276B0J3L
4V22
U10
LT3094IDD
VIOC
OUTS
C125
10uF
C126
1uF
C127
10uF
R33
10K2
C128
NFM31PC276B0J3L
-1V02
Output voltage is RSN*100uA (+-2%)
max. 500 mA
Title: Power supply, DC/DC converter for split supply (+5 V and -5 V) and low noise LDOs (4.22 V and -1.02 V)
Project: FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website: www.iamelectronic.com
Date: 19.02.2020
Engineer: PFH
Rev: C
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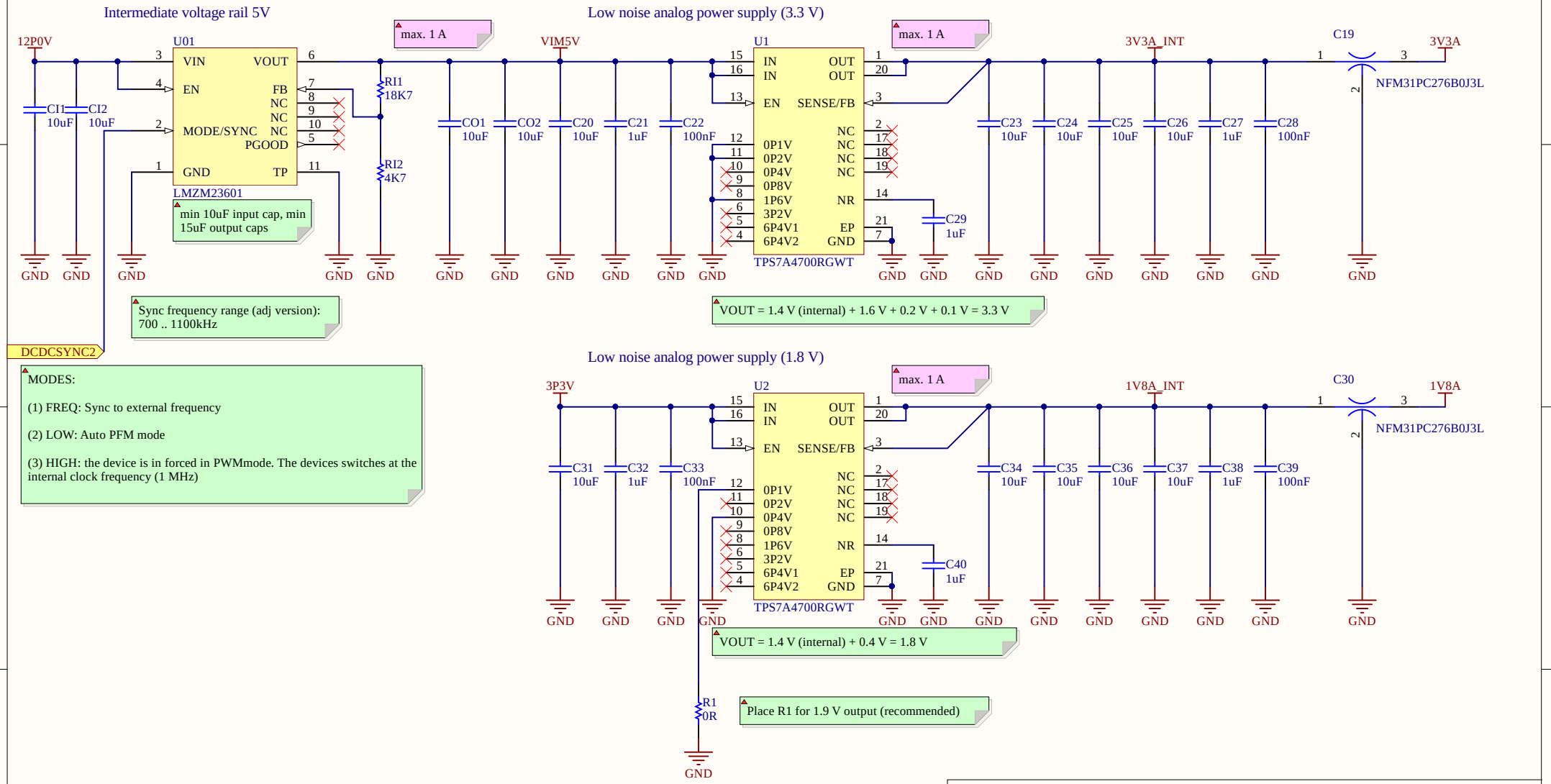

Title:	*Linear voltage regulators for analog supply voltages (3.3 V and 1.8 V)*
Project:	FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website:	www.iamelectronic.com
Date:	19.02.2020
Rev:	C
Engineer:	PFH
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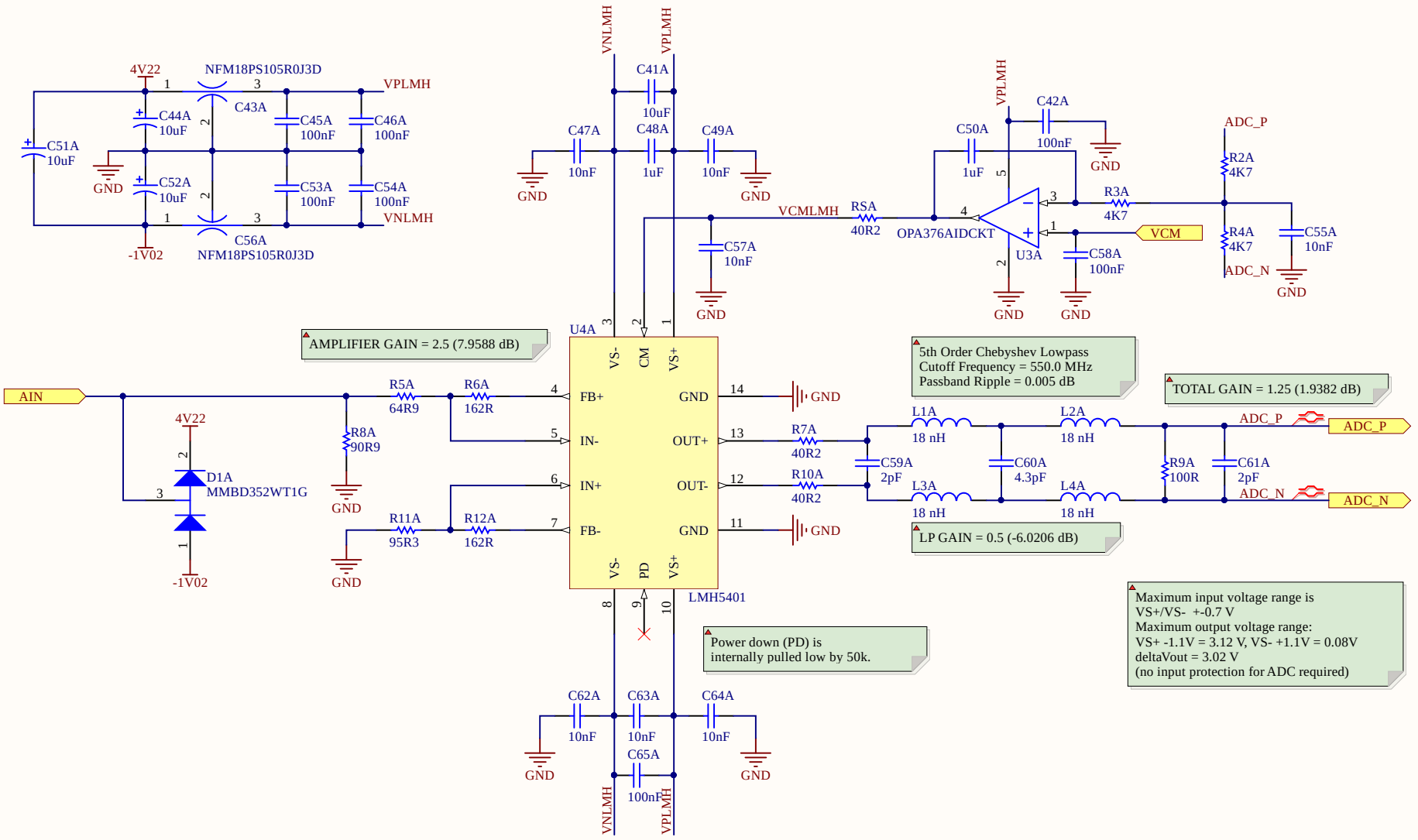
Power supply filtering

Amplifier stage with passive low-pass filter

Common mode control



Title:	*Analog input channel with passive low-pass filter*
Project:	FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website:	www.iamelectronic.com
Date:	19.02.2020
Rev:	C
Engineer:	PFH
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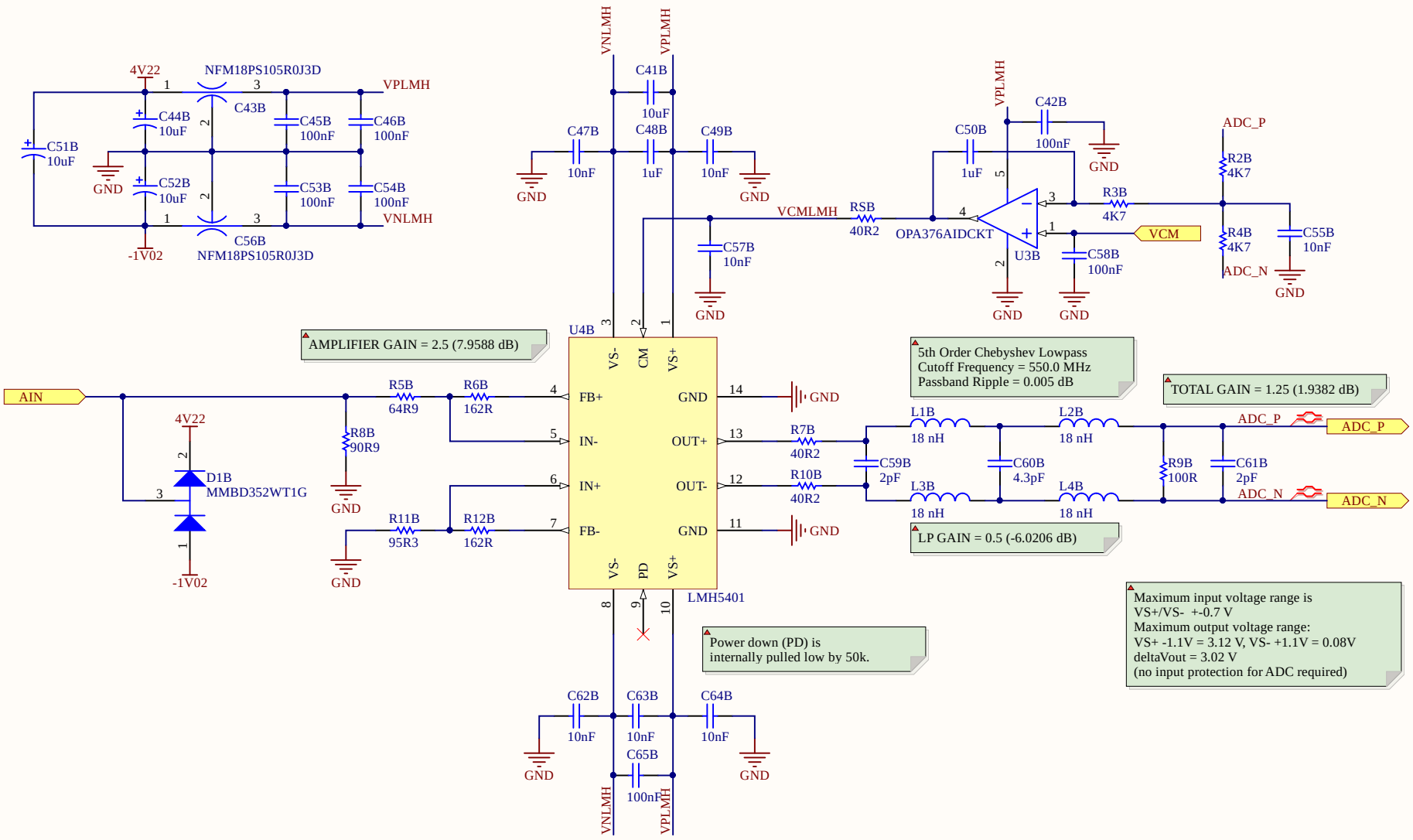

Title:	*Analog input channel with passive low-pass filter*
Project:	FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website:	www.iamelectronic.com
Date:	19.02.2020
Engineer:	PFH
Rev:	C
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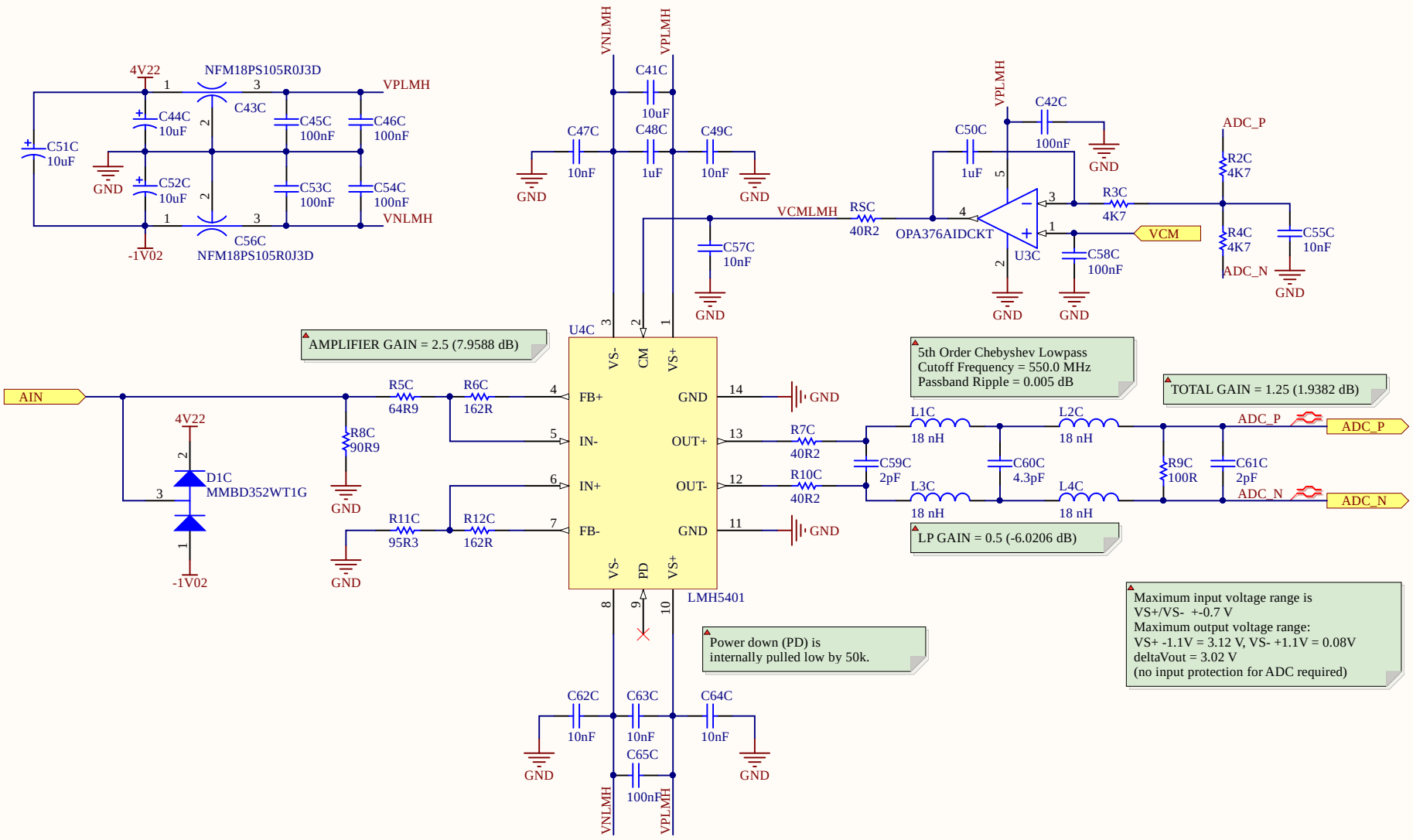

Title:	*Analog input channel with passive low-pass filter*
Project:	FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website:	www.iamelectronic.com
Date:	19.02.2020
Engineer:	PFH
Rev:	C
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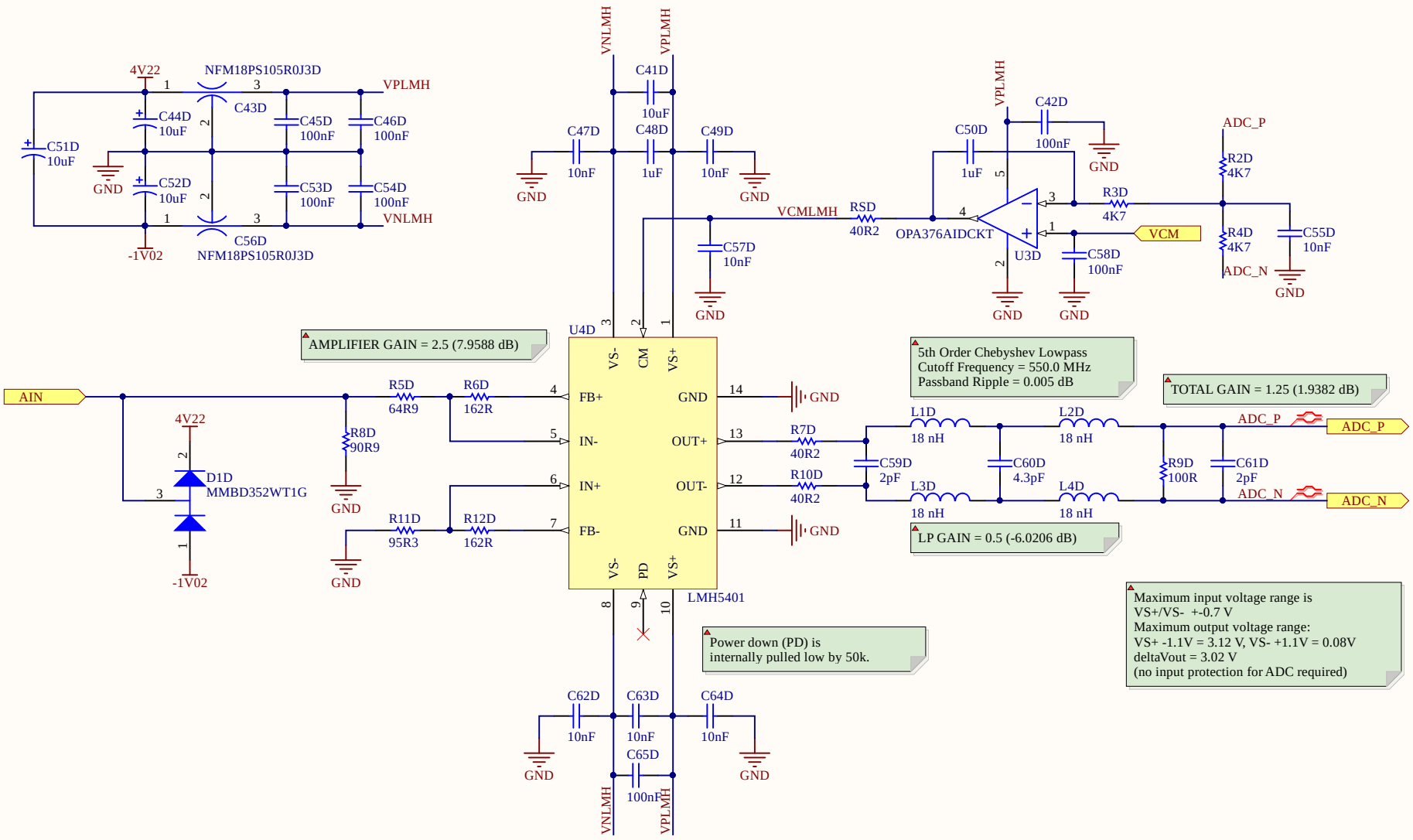

Title:	*Analog input channel with passive low-pass filter*
Project:	FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website:	www.iamelectronic.com
Date:	19.02.2020
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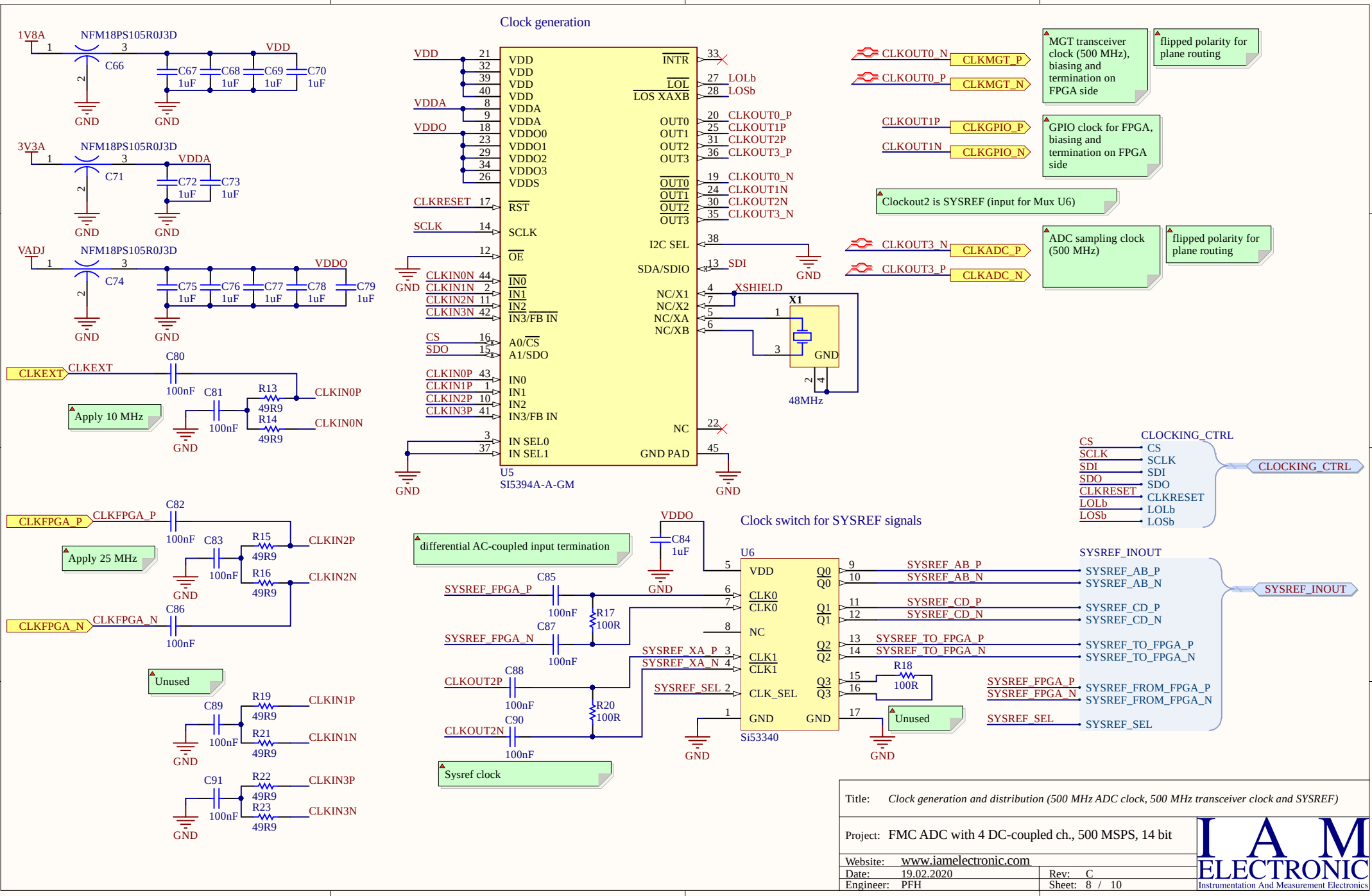

Title:	*Clock generation and distribution (500 MHz ADC clock, 500 MHz transceiver clock and SYSREF)*
Project:	FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
Website:	www.iamelectronic.com
Date:	19.02.2020
Engineer:	PFH
Rev:	C
Sheet:	8 / 10

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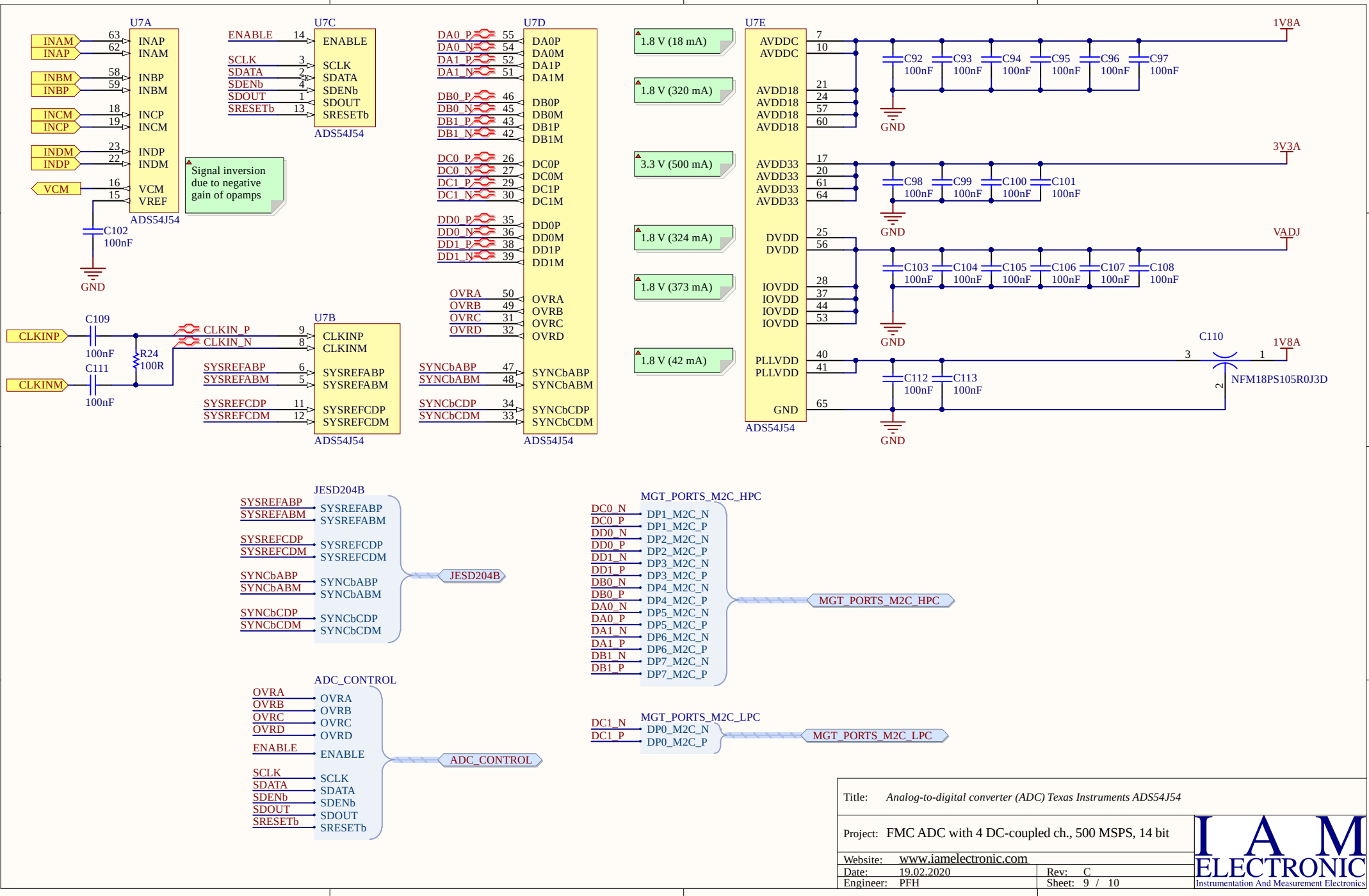
U7A
INAM
INAP
INBM
INBP
INCM
INCP
INDM
INDP
VCM
INAP
INAM
INBP
INBM
INCP
INCM
INDP
INDM
VCM
VREF
ADS54J54
Signal inversion due to negative gain of opamps
C102
100nF
GND
U7C
ENABLE
SCLK
SDATA
SDENb
SDOUT
SRESETb
ADS54J54
U7D
DA0_P
DA0_N
DA1_P
DA1_N
DB0_P
DB0_N
DB1_P
DB1_N
DC0_P
DC0_N
DC1_P
DC1_N
DD0_P
DD0_N
DD1_P
DD1_N
OVRA
OVRB
OVRC
OVRD
SYNCbABP
SYNCbABM
SYNCbCDP
SYNCbCDM
ADS54J54
1.8 V (18 mA)
1.8 V (320 mA)
3.3 V (500 mA)
1.8 V (324 mA)
1.8 V (373 mA)
1.8 V (42 mA)
U7E
AVDDC
AVDD18
AVDD33
DVDD
IOVDD
PLLVDD
GND
ADS54J54
C92 100nF
C93 100nF
C94 100nF
C95 100nF
C96 100nF
C97 100nF
C98 100nF
C99 100nF
C100 100nF
C101 100nF
C103 100nF
C104 100nF
C105 100nF
C106 100nF
C107 100nF
C108 100nF
C112 100nF
C113 100nF
1V8A
3V3A
VADJ
C110
NFM18PS105R0J3D
C109
100nF
C111
100nF
R24
100R
CLKINP
CLKINM
CLKIN_P
CLKIN_N
U7B
SYSREFABP
SYSREFABM
SYSREFCDP
SYSREFCDM
ADS54J54
JESD204B
MGT_PORTS_M2C_HPC
DP1_M2C_N
DP1_M2C_P
DP2_M2C_N
DP2_M2C_P
DP3_M2C_N
DP3_M2C_P
DP4_M2C_N
DP4_M2C_P
DP5_M2C_N
DP5_M2C_P
DP6_M2C_N
DP6_M2C_P
DP7_M2C_N
DP7_M2C_P
MGT_PORTS_M2C_LPC
DP0_M2C_N
DP0_M2C_P
ADC_CONTROL
Title: Analog-to-digital converter (ADC) Texas Instruments ADS54J54
Project: FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
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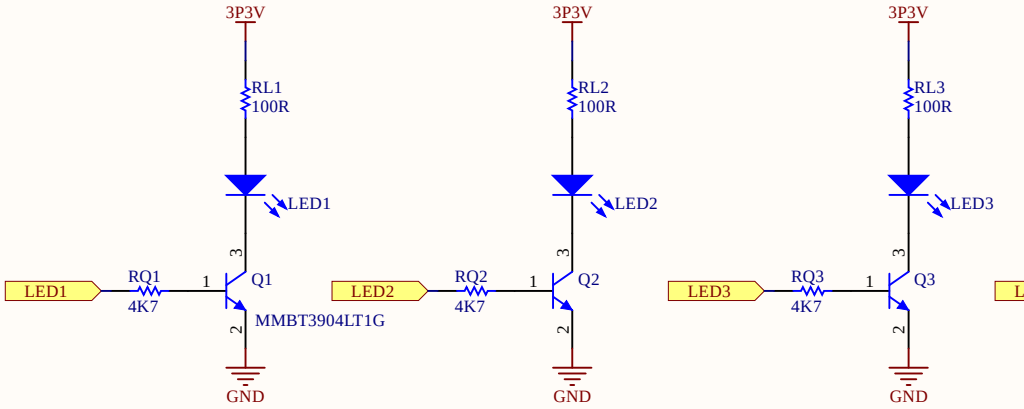
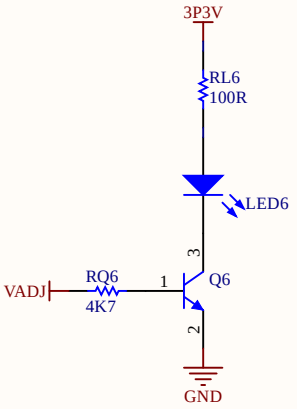
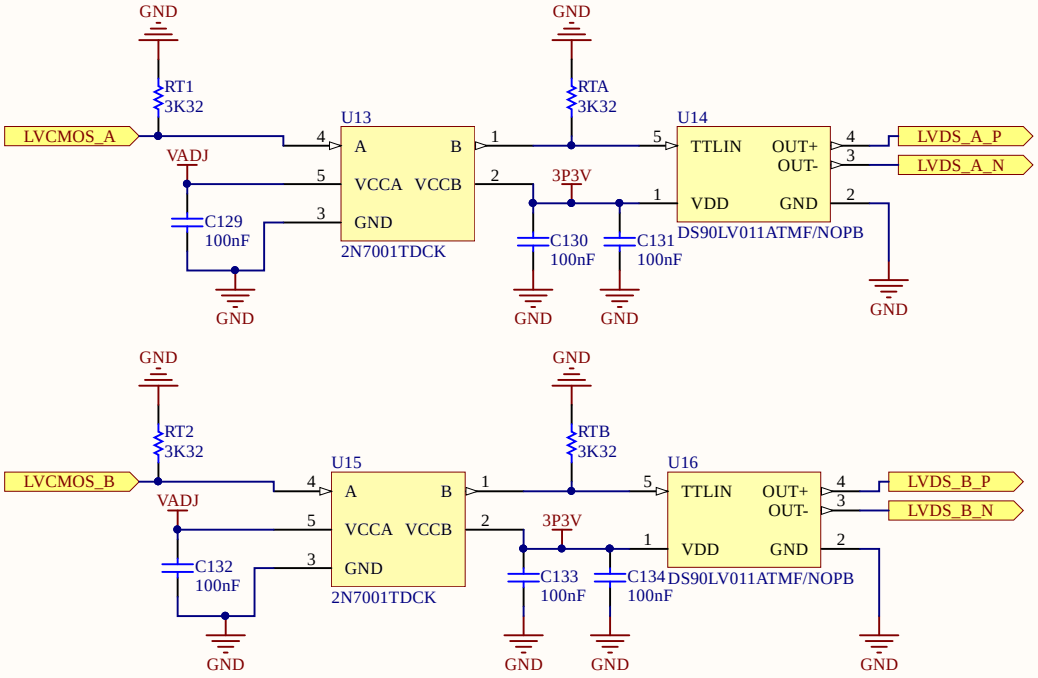
GPIO Leds (green)



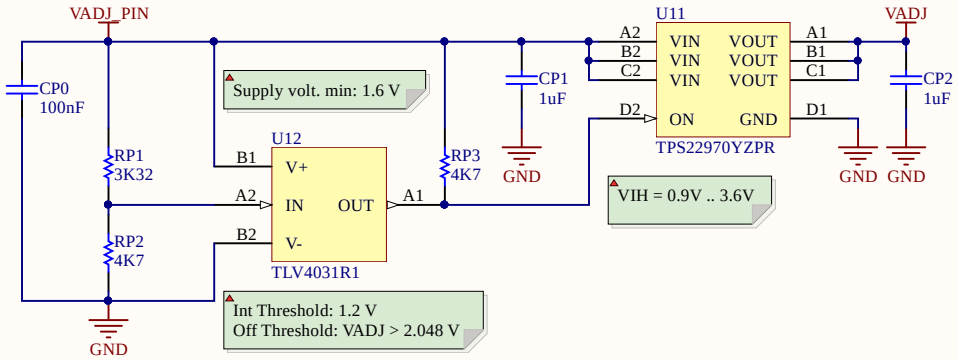
Power on LED



Single-ended LVCMOS 1.8V to LVDS translatation (1.2V offset, ±350mV differential signaling)



Protection circuit for VADJ (circuit is on with VADJ at 1.8V, off at >2.1V)



Title:	*LEDs, VADJ protection, and level shifting for LVCMOS18 signals*
Project:	FMC ADC with 4 DC-coupled ch., 500 MSPS, 14 bit
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