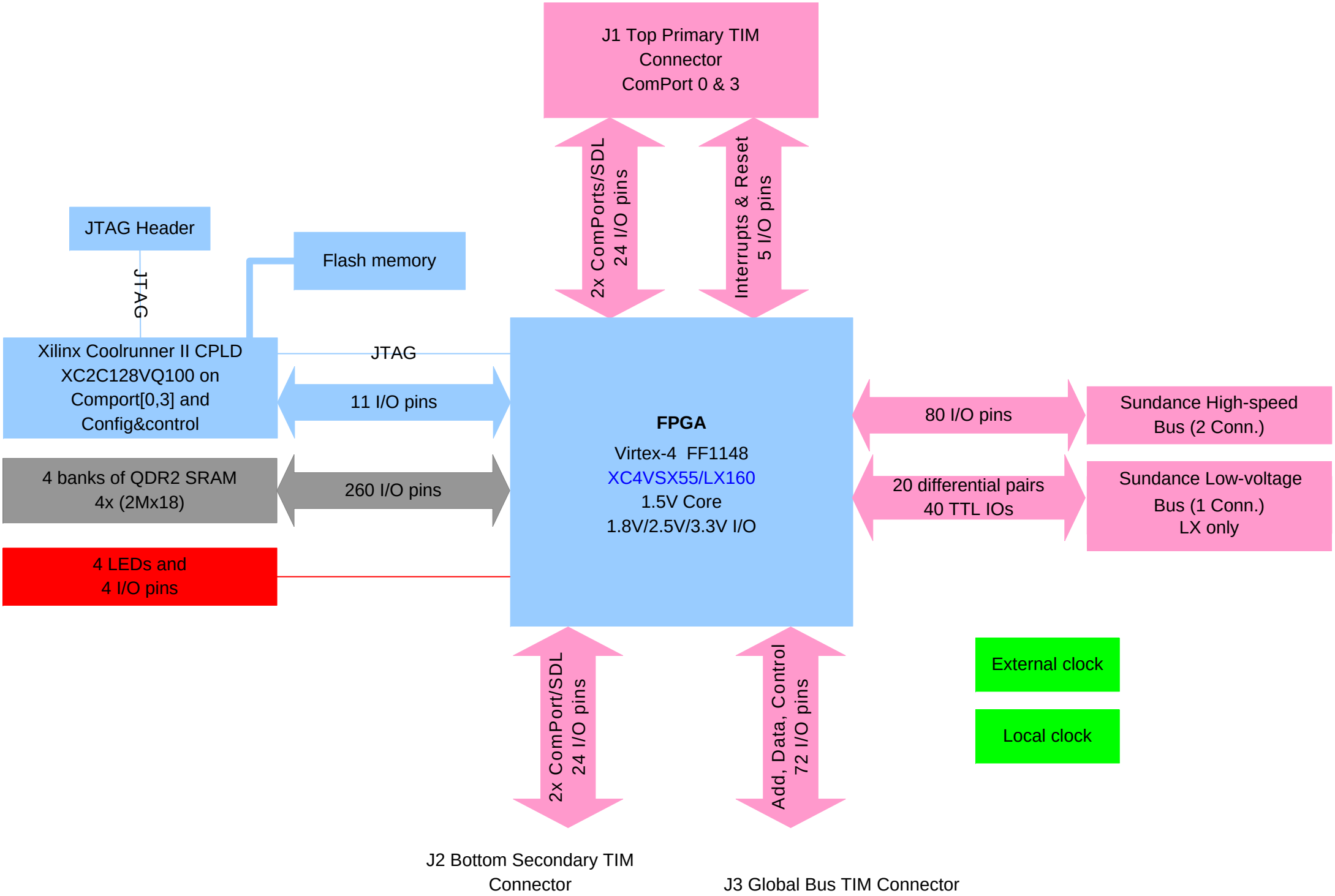
J1 Top Primary TIM Connector ComPort 0 & 3
2x ComPorts/SDL 24 I/O pins
Interrupts & Reset 5 I/O pins
JTAG Header
JTAG
Flash memory
Xilinx Coolrunner II CPLD XC2C128VQ100 on Comport[0,3] and Config&control
JTAG
11 I/O pins
4 banks of QDR2 SRAM 4x (2Mx18)
260 I/O pins
4 LEDs and 4 I/O pins
FPGA
Virtex-4 FF1148
XC4VSX55/LX160
1.5V Core
1.8V/2.5V/3.3V I/O
80 I/O pins
Sundance High-speed Bus (2 Conn.)
20 differential pairs 40 TTL IOs
Sundance Low-voltage Bus (1 Conn.) LX only
2x ComPort/SDL 24 I/O pins
Add, Data, Control 72 I/O pins
External clock
Local clock
J2 Bottom Secondary TIM Connector
J3 Global Bus TIM Connector