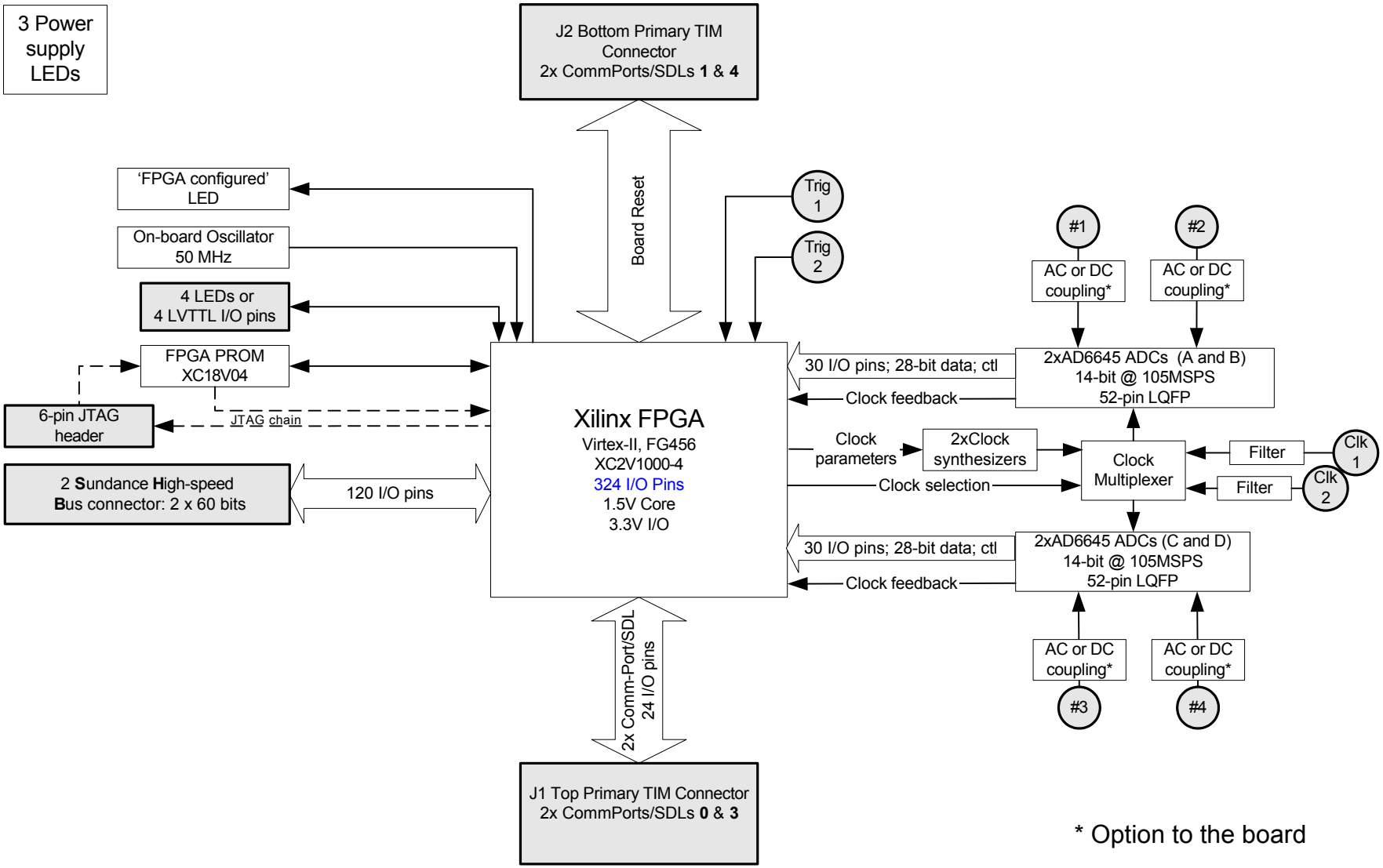
3 Power supply LEDs
J2 Bottom Primary TIM Connector
2x CommPorts/SDLs **1** & **4**
Board Reset
'FPGA configured' LED
On-board Oscillator 50 MHz
4 LEDs or 4 LVTTL I/O pins
FPGA PROM XC18V04
6-pin JTAG header
JTAG chain
2 **S**undance **H**igh-speed **B**us connector: 2 x 60 bits
120 I/O pins
Trig 1
Trig 2
Xilinx FPGA
Virtex-II, FG456
XC2V1000-4
324 I/O Pins
1.5V Core
3.3V I/O
2x Comm-Port/SDL
24 I/O pins
J1 Top Primary TIM Connector
2x CommPorts/SDLs **0** & **3**
#1
#2
#3
#4
AC or DC coupling*
30 I/O pins; 28-bit data; ctl
Clock feedback
2xAD6645 ADCs (A and B)
14-bit @ 105MSPS
52-pin LQFP
Clock parameters
2xClock synthesizers
Clock selection
Clock Multiplexer
Filter
Clk 1
Clk 2
2xAD6645 ADCs (C and D)
14-bit @ 105MSPS
52-pin LQFP
* Option to the board