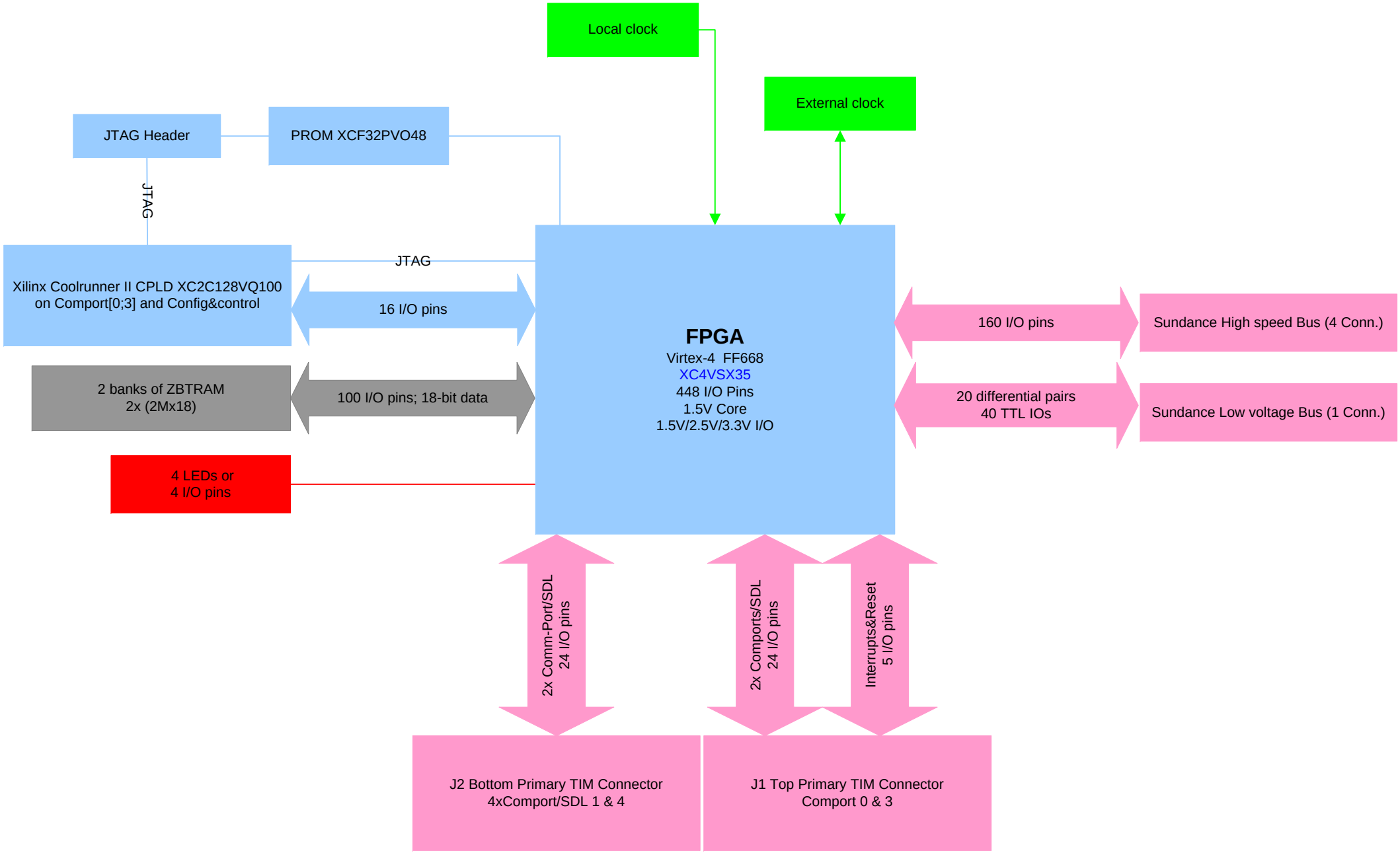
Local clock
External clock
JTAG Header
PROM XCF32PVO48
JTAG
JTAG
Xilinx Coolrunner II CPLD XC2C128VQ100
on Comport[0;3] and Config&control
16 I/O pins
FPGA
Virtex-4 FF668
XC4VSX35
448 I/O Pins
1.5V Core
1.5V/2.5V/3.3V I/O
160 I/O pins
Sundance High speed Bus (4 Conn.)
2 banks of ZBTRAM
2x (2Mx18)
100 I/O pins; 18-bit data
20 differential pairs
40 TTL IOs
Sundance Low voltage Bus (1 Conn.)
4 LEDs or
4 I/O pins
2x Comm-Port/SDL
24 I/O pins
2x Comports/SDL
24 I/O pins
Interrupts&Reset
5 I/O pins
J2 Bottom Primary TIM Connector
4xComport/SDL 1 & 4
J1 Top Primary TIM Connector
Comport 0 & 3