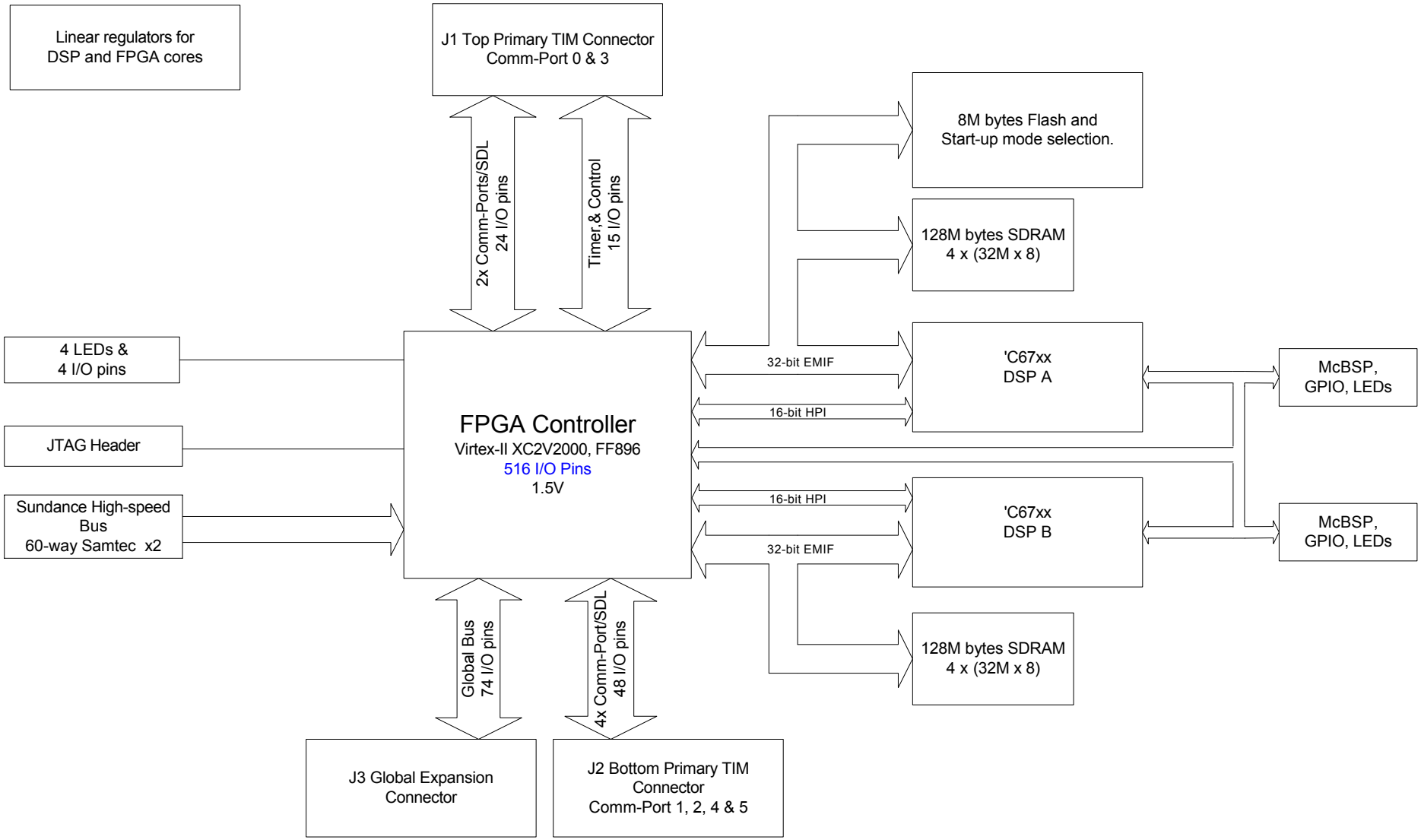
Linear regulators for
DSP and FPGA cores
J1 Top Primary TIM Connector
Comm-Port 0 & 3
2x Comm-Ports/SDL
24 I/O pins
Timer,& Control
15 I/O pins
8M bytes Flash and
Start-up mode selection.
128M bytes SDRAM
4 x (32M x 8)
4 LEDs &
4 I/O pins
JTAG Header
Sundance High-speed
Bus
60-way Samtec x2
FPGA Controller
Virtex-II XC2V2000, FF896
516 I/O Pins
1.5V
32-bit EMIF
16-bit HPI
'C67xx
DSP A
McBSP,
GPIO, LEDs
16-bit HPI
32-bit EMIF
'C67xx
DSP B
McBSP,
GPIO, LEDs
128M bytes SDRAM
4 x (32M x 8)
Global Bus
74 I/O pins
4x Comm-Port/SDL
48 I/O pins
J3 Global Expansion
Connector
J2 Bottom Primary TIM
Connector
Comm-Port 1, 2, 4 & 5