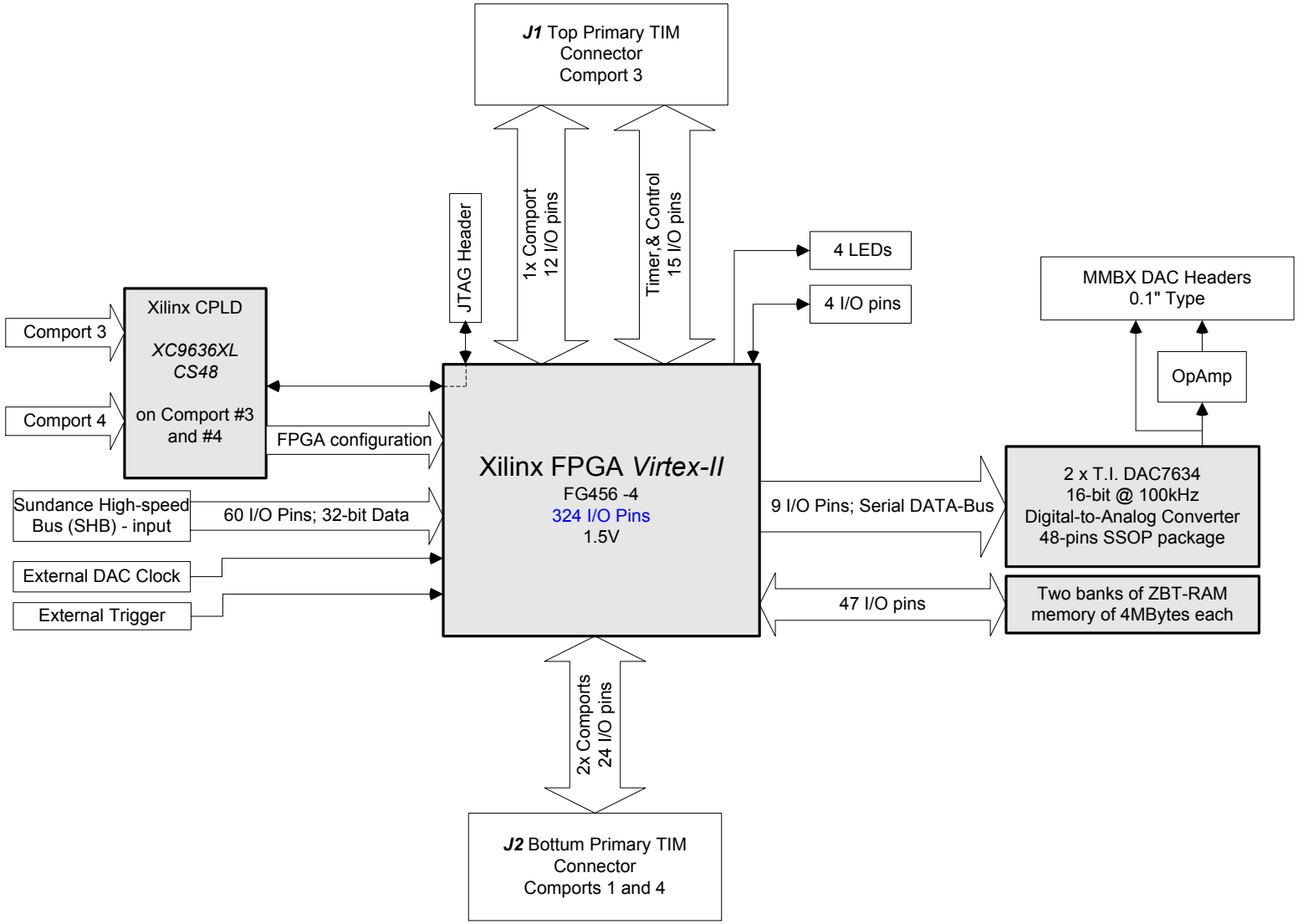
J1 Top Primary TIM Connector Comport 3
1x Comport 12 I/O pins
Timer & Control 15 I/O pins
JTAG Header
4 LEDs
4 I/O pins
MMBX DAC Headers 0.1" Type
OpAmp
Comport 3
Comport 4
Xilinx CPLD
XC9636XL CS48
on Comport #3 and #4
FPGA configuration
Xilinx FPGA Virtex-II
FG456 -4
324 I/O Pins
1.5V
Sundance High-speed Bus (SHB) - input
60 I/O Pins; 32-bit Data
External DAC Clock
External Trigger
9 I/O Pins; Serial DATA-Bus
2 x T.I. DAC7634 16-bit @ 100kHz Digital-to-Analog Converter 48-pins SSOP package
47 I/O pins
Two banks of ZBT-RAM memory of 4MBytes each
2x Comports 24 I/O pins
J2 Bottum Primary TIM Connector Comports 1 and 4