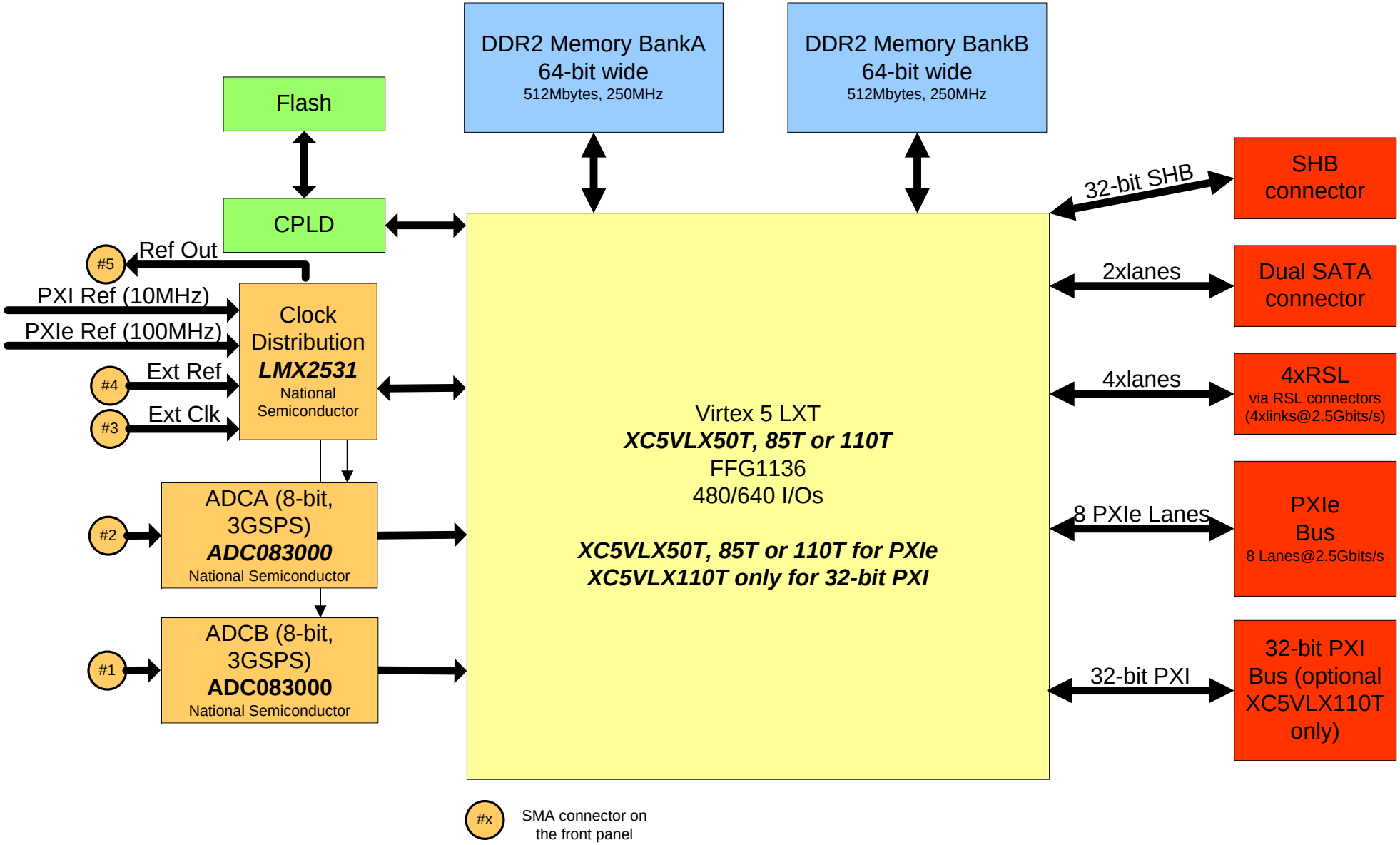
DDR2 Memory BankA
64-bit wide
512Mbytes, 250MHz
DDR2 Memory BankB
64-bit wide
512Mbytes, 250MHz
Flash
CPLD
Ref Out
#5
PXI Ref (10MHz)
PXIe Ref (100MHz)
Clock Distribution
LMX2531
National Semiconductor
#4
Ext Ref
#3
Ext Clk
ADCA (8-bit, 3GSPS)
ADC083000
National Semiconductor
#2
ADCB (8-bit, 3GSPS)
ADC083000
National Semiconductor
#1
Virtex 5 LXT
XC5VLX50T, 85T or 110T
FFG1136
480/640 I/Os
XC5VLX50T, 85T or 110T for PXIe
XC5VLX110T only for 32-bit PXI
32-bit SHB
SHB connector
2xlanes
Dual SATA connector
4xlanes
4xRSL
via RSL connectors
(4xlinks@2.5Gbits/s)
8 PXIe Lanes
PXIe Bus
8 Lanes@2.5Gbits/s
32-bit PXI
32-bit PXI Bus (optional XC5VLX110T only)
#x
SMA connector on the front panel