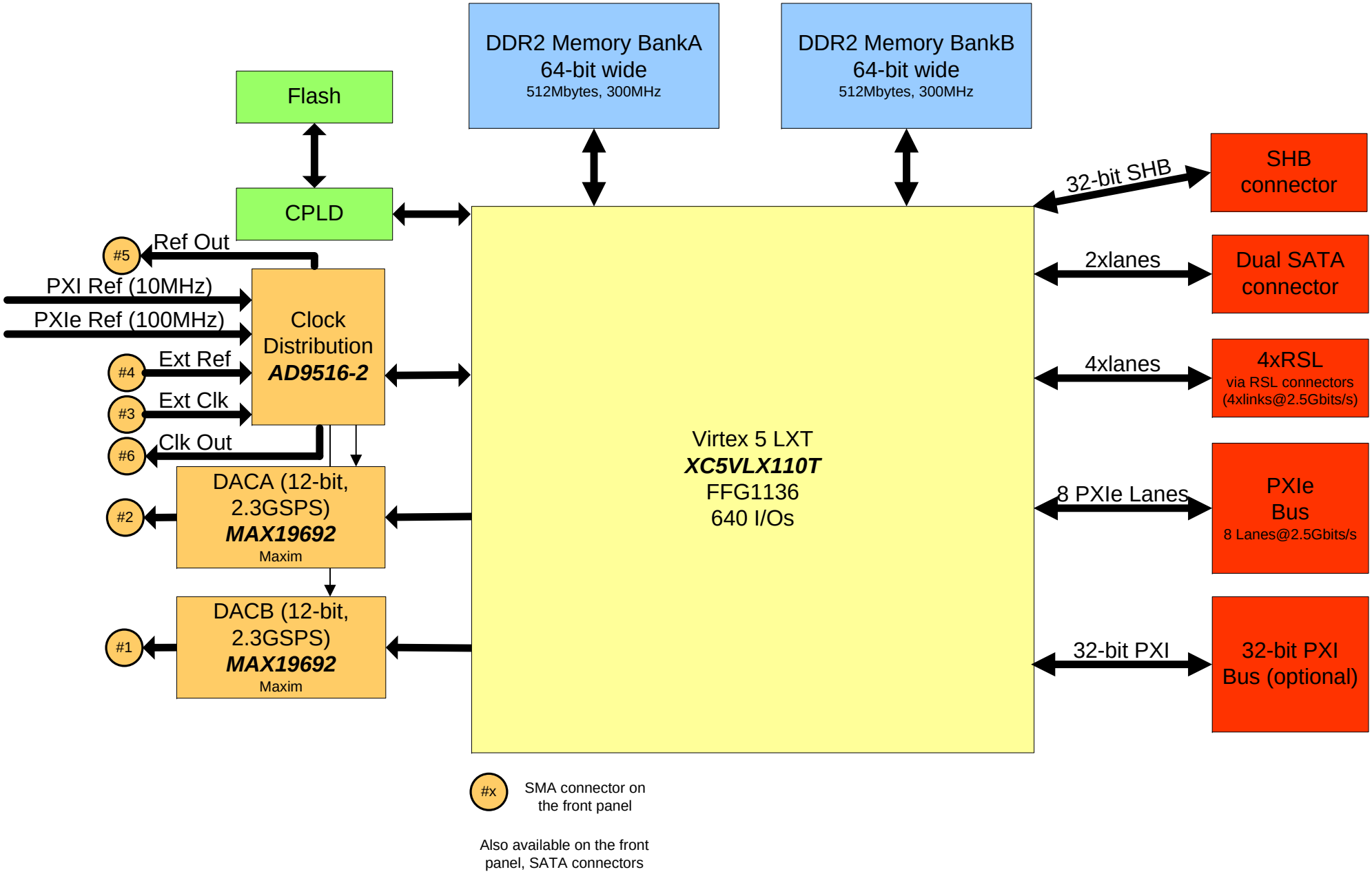
DDR2 Memory BankA
64-bit wide
512Mbytes, 300MHz
DDR2 Memory BankB
64-bit wide
512Mbytes, 300MHz
Flash
CPLD
Ref Out
#5
PXI Ref (10MHz)
PXIe Ref (100MHz)
Clock
Distribution
AD9516-2
#4
Ext Ref
#3
Ext Clk
#6
Clk Out
DACA (12-bit,
2.3GSPS)
MAX19692
Maxim
#2
DACB (12-bit,
2.3GSPS)
MAX19692
Maxim
#1
Virtex 5 LXT
XC5VLX110T
FFG1136
640 I/Os
32-bit SHB
SHB
connector
2xlanes
Dual SATA
connector
4xlanes
4xRSL
via RSL connectors
(4xlinks@2.5Gbits/s)
8 PXIe Lanes
PXIe
Bus
8 Lanes@2.5Gbits/s
32-bit PXI
32-bit PXI
Bus (optional)
#x
SMA connector on
the front panel
Also available on the front
panel, SATA connectors