MORFAN-1
Dual Radio MIMO Transceiver Card
User Manual

Date: Dec 15, 2008
Version: 1.2

Revision History

Date	Version	Revisions	Initials
Dec 05, 2007	1.1	Initial release	
Dec 15, 2008	1.2	Firmware Design, implementation on SMT351 FPGA Module using Diamond FPGA IDE with firmware version 4.2	MF

Table of Contents

List of Figures

List of Tables

Precautions

In order to guarantee that the MORFAN card functions correctly and to protect the module from damage, the following precautions should be taken:

- Protect the board against electrostatic discharge.
  Always place the module in a static protective bag during storage and transition.
- If the card is operated in a closed environment (cabinet) proper cooling (e.g. by use of a fan) must be assured.

1 Introduction

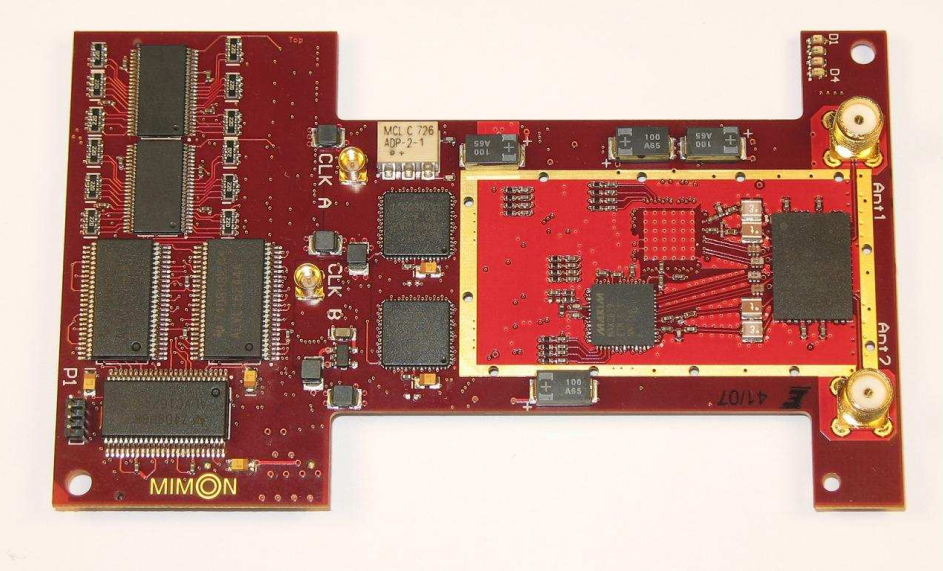


Figure 1 : MORFAN-1 MIMO Transceiver card

1.1 General Description

MORFAN-1 is an advanced, high-quality MIMO transceiver card, designed to cover all features of future high-speed MIMO TDD radio systems. MORFAN-1 comprises two complete, fully configurable transceiver chains between two 2 x 10-bit digital I/Q interfaces and two dual-band 50 Ohm antenna ports. Each transceiver chain comprises RF-frontend (band switch / RX-TX switch and power amplifier), up-/down converters with on chip PLLs and high-performance analog-to-digital and digital-to-analog converters for the I/Q signals and auxiliary analog-to-digital converters for RSSI and TX power detection signals.

With a single externally supplied common reference clock for the transceiver PLLs multiple MORFAN-1 cards are easily combined to build an arbitrary size 2*m* x 2*n* MIMO system with coherent LO phase.

All control signals and the SPI bus are routed through a 120-pin QSH data connector providing highest freedom for flexible, application specific configuration and control during operation. MORFAN-1 is designed to fit on and connect directly to an FPGA base module like the Sundance SMT368.

The optional MORFAN-1 Firmware Control Module permits simple and unrestricted access to all control registers from a user friendly C-Language API.

1.2 Features

- Dual radio MIMO transceiver card for 2.4 – 2.5 GHz & 5.15 – 5.875 GHz bands
- Bandwidth configurable up to 40 MHz
- Direct conversion architecture
- 2 x 10-bit digital I/Q baseband interface
- 200 MSPS Digital-to-Analog converters
- 80 MSPS Analog-to-Digital converters
- Auxiliary ADCs for RSSI and TX power detection signals
- Transceiver and RF front-end comply to IEEE 802.11a/b/g/n specifications with 64 QAM modulation
- Pout up to 18 dBm in 2.4 – 2.5 GHz
- Pout up to 15 dBm in 5.15 – 5.875 GHz
- 4-pin header for custom I/O (4 LVTTL)
- Stackable to build arbitrary order 2*m* x 2*n* MIMO systems
- Fully configurable
- All I/O signals completely buffered for highest noise immunity
- Complete separation of digital and analog supply circuits using low-noise LDOs

1.3 Interfaces

- 2 SMA connectors (50 Ohm) for two dual-band antennas
- 2 MMCX connectors (50 Ohm) for transceiver PLL clock reference and sampling clock reference of the ADDAC chips respectively
- Samtec BKT connector for 5 V and 3.3 V power supply
- 120-pin Samtec QSH connector for all digital I/O signals
- Plugs directly into a Sundance SMT368 module

1.4 Related Documents

- Datasheet: “SE2545A23 RangeCharger™ Dual Band 802.11n Wireless LAN Front End”, SiGe
- Datasheet: “MAX2828/2829 World-Class Transceiver-IC”, Maxim
- Datasheet: “AD9861”, Analog Devices
  http://www.analog.com/en/prod/0%2C2877%2CAD9861%2C00.html
- Sundance High-speed Bus (SHB) specifications – Sundance.
  ftp://ftp2.sundance.com/Pub/documentation/pdf-files/SHB_Technical_Specification.pdf
- Sundance LVDS Bus (SLB) specifications – Sundance
  http://www.sundance.com/docs/SLB%20-%20Sundance%20Local%20Bus%20Specification.pdf
- TIM Specifications.
  ftp://ftp2.sundance.com/Pub/documentation/pdf-files/tim_spec_v1.01.pdf
- Xilinx Virtex-4 FPGA
  http://direct.xilinx.com/bvdocs/publications/ds031.pdf
- Sundance SMT368 User Manual – Sundance
  http://www.sundance.com/docs/SMT368%20User%20Manual.pdf

2 Functional Description

MORFAN-1 is an advanced, high-quality MIMO transceiver card, designed to cover all features of future high-speed MIMO TDD radio systems. It is used in combination with the base module such as SMT368. Figure 2 shows us the block diagram of MORFAN-1 transceiver card, the base module SMT368 and the connection between them. The base module provides MORFAN-1 with QSH connector for data connection and BKS connector for power connection.

On the MORFAN-1 transceiver card, a single-chip MIMO RF front-end (SE2545A23) is applied, which contains basically all circuitry between the transceiver and the antenna. Two transceiver chips of type Maxim MAX2829 are used to up- and down-convert signals between the ISM bands and the base band. The MAX2829 is specially designed for MIMO/Smart Antenna application and the IEEE 802.11n standard.

In order to fulfill the requirements of more simple and clever MIMO solutions the MORFAN-1 transceiver card is equipped with two built-in ADDAC chips – AD9861. Each of transceiver chips is served by one AD9861. The AD9861 integrates dual 10-bit ADCs and dual 10-bit DACs as well as three auxiliary converters. The dual ADCs convert the digital base band I/Q signals to analog signals when the MORFAN-1 card acts as transmitter. When the MORFAN-1 card acts as receiver, the dual DACs convert the analog base band I/Q signals to digital format. The auxiliary converters are used for conversion of the Receive Signal Strength Information (RSSI) and Power Detection Signals as needed for implementation of digital Automatic Gain Control (AGC) and Power Control (PwC) algorithms. The conversion values are accessible via the firmware registers.

All control pins of the mentioned ICs above are routed through to the base module via the QSH connector. The firmware on the base module offers the user flexibility to specify control signals and control register settings. More details about the firmware are explained in Firmware implementation section.

The MORFAN-1 card has two external reference clock inputs – **CLK A** and **CLK B**. CLK A is the reference clock for the two transceiver PLLs. CLK B is the reference clock for generating the sampling clock in two ADDAC chips.

The 4-pin header – **P1** provides the 4 LVTTL I/O pins for custom usage. These 4 pins are directly connected to the FPGA on the base module via the QSH connector.

The MORFAN-1 card is equipped with four LEDs – **D1:D4**. They are connected with the FPGA on the base module through the QSH connector. All LEDs are controlled by the firmware for use as indicators. Two of them act as Lock Detect Indicators of the transceivers. They are turned on when the frequency synthesizers are locked.

2.1 Block Diagrams

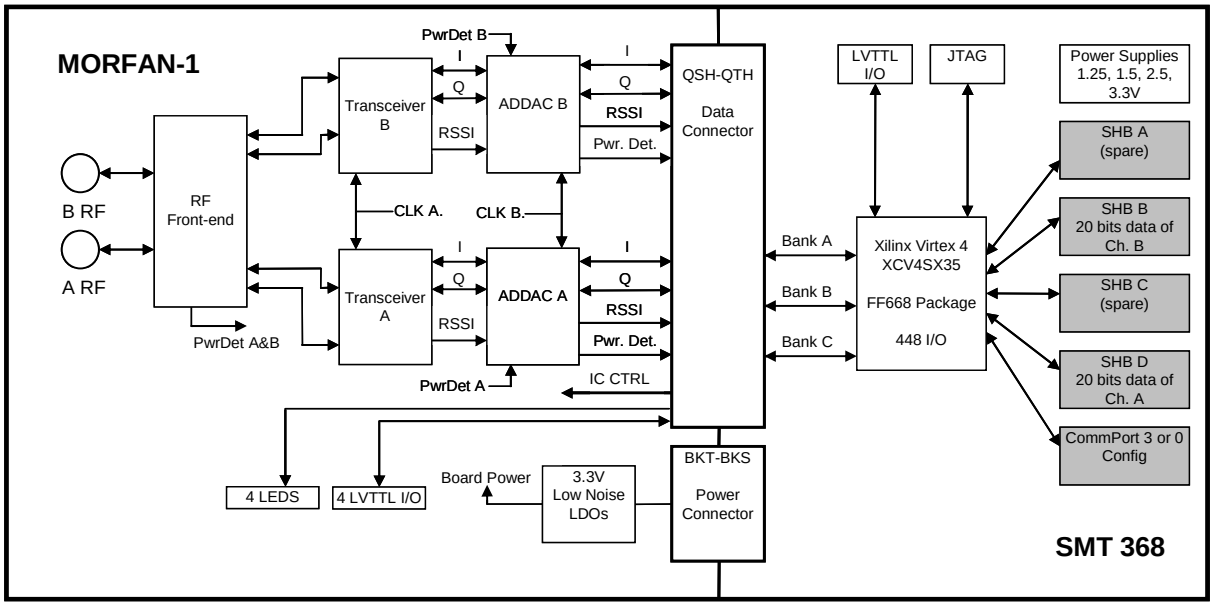


Figure 2 : Block diagram of MORFAN-1 MIMO transceiver card and SMT368

2.2 Power Supply

The base module is to supply the MORFAN-1 transceiver card with +5 V and +3.3 V DC power via the power connector from Samtec Inc.

The male power connector is located on the MORFAN-1 transceiver card. The Samtec Part Number for this connector is BKT-133-03-F-V-A (Fig. 3). The corresponding female power connector BKS-133-03-F-V-A is located on the base module.

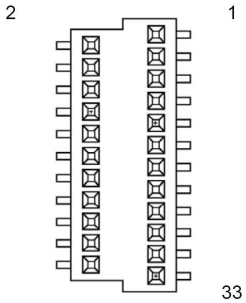


Figure 3 : BKT power connector

Table 1 : MORFAN-1 transceiver card pin usage on the power connector

Pin Number	Pin Name	Description of Signal
1	D+3V3	Not connected
2	DGND	Digital Ground
3	D+3V3	Not connected
4	DGND	Digital Ground
5	D+3V3	Digital 3.3 Volts
6	DGND	Digital Ground
7	D+3V3	Digital 3.3 Volts

8	DGND	Digital Ground
9	D+5V0	Digital 5.0 Volts
10	DGND	Digital Ground
11	D+5V0	Digital 5.0 Volts
12	DGND	Digital Ground
13	D+5V0	Digital 5.0 Volts
14	DGND	Digital Ground
15	D+5V0	Digital 5.0 Volts
16	DGND	Digital Ground
17	D+12V0	Not connected
18	DGND	Digital Ground
19	D+12V0	Not connected
20	DGND	Digital Ground
21	D-12V0	Not connected
22	DGND	Digital Ground
23	D-12V0	Not connected
24	DGND	Digital Ground
25	DGND	Digital Ground
26	EMU0	Not connected
27	EMU1	Not connected
28	TMS	Not connected
29	nTRST	Not connected
30	TCK	Not connected
31	TDI	Not connected
32	TDO	Not connected
33	DGND	Digital Ground

2.3 Data Connection

All communication between the MORFAN-1 transceiver card and the base module is carried through the data connector. The MORFAN-1 transceiver card is equipped with the 120-pin male connector with the Samtec Part Number QSH-060-01-F-D-DP-A shown in Figure 4. The corresponding female connector QTH-060-01-F-D-DP-A is located on the base module.

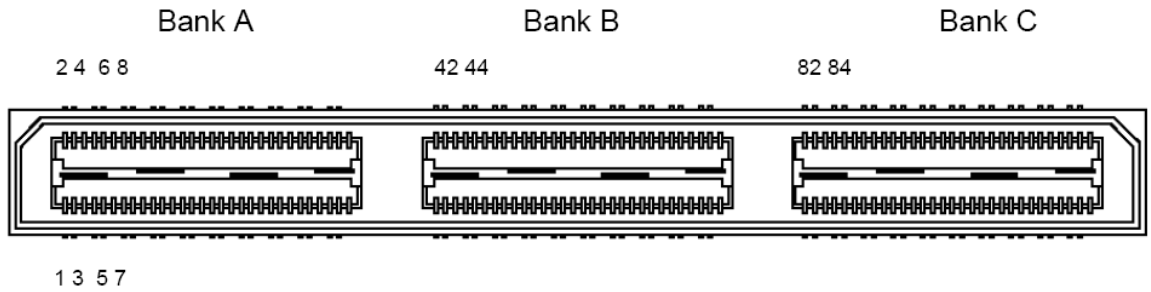


Figure 4 : 120pin-QSH data connector

Note that all signals from and to the MORFAN-1 card are single ended.

The pins are grouped as follows:

- 8 pins for control and switching of the RF Front-end Chip
- 30 pins for control and switching of the 2 Transceiver Chips
- 63 pins for control and data transfer from and to the 2 ADDAC Chips
- 4 pins LVTTL I/O header

- 4 pins for LEDs
- 11 pins not connected

The detailed pin assignment is given in Table 2, Table 3 and Table 4. For more detailed functional descriptions of the pins of the different chips please refer to the relevant documents.

Table 2 : Pin configuration of QSH connector Bank A

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
1	AdAL7	AD9861 A data pin L7	2	AdAL9	AD9861 A data pin L9
3	AdAL6	AD9861 A data pin L6	4	AdAL8	AD9861 A data pin L8
5	AdAL5	AD9861 A data pin L5	6	AdAL2	AD9861 A data pin L2
7	AdAL4	AD9861 A data pin L4	8	AdAL3	AD9861 A data pin L3
9	AdAL1	AD9861 A data pin L1	10	AdAL0	AD9861 A data pin L0
11	AdAU8	AD9861 A data pin U8	12	AdAU9	AD9861 A data pin U9
13	AdAU5	AD9861 A data pin U5	14	AdAU7	AD9861 A data pin U7
15	AdAU4	AD9861 A data pin U4	16	AdAU6	AD9861 A data pin U6
17	AdAU3	AD9861 A data pin U3	18	AdAU1	AD9861 A data pin U1
19	AdAU2	AD9861 A data pin U2	20	AdAU0	AD9861 A data pin U0
21	AdBL9	AD9861 B data pin L9	22	AdBL0	AD9861 B data pin L0
23	AdBL8	AD9861 B data pin L8	24	AdBL1	AD9861 B data pin L1
25	AdBL7	AD9861 B data pin L7	26	AdBL2	AD9861 B data pin L2
27	AdBL6	AD9861 B data pin L6	28	AdBL4	AD9861 B data pin L4
29	AdBL5	AD9861 B data pin L5	30	AdBL3	AD9861 B data pin L3
31	AdBU9	AD9861 B data pin U9	32	AdBU8	AD9861 B data pin U8
33	AdBU4	AD9861 B data pin U4	34	AdBU3	AD9861 B data pin U3
35	AdBU5	AD9861 B data pin U5	36	AdBU2	AD9861 B data pin U2
37	AdBU6	AD9861 B data pin U6	38	AdBU1	AD9861 B data pin U1
39	AdBU7	AD9861 B data pin U7	40	AdBU0	AD9861 B data pin U0

Table 3 : Pin configuration of QSH connector Bank B

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
41	AdAIFace1	IFace1 AD A	42	AdAAuCs	Aux. Ser. Chip Sel. Ad A
43	AdARxDwn	Rx PwrDwn AD A	44	AdASerDa	Ser Data AD A
45	AdASerEn	Ser Enable AD A	46	AdATxDwn	Tx PwrDwn AD A
47	AdASerClk	Ser Clock AD A	48	AdAAuClk	Aux. Ser. Clock AD A
49	AdBIFace1	IFace1 AD B	50	AdBAuCs	Aux. Ser. Chip Sel. Ad B
51	AdBSerClk	Ser Clock AD B	52	AdBSerDa	Ser Data AD B
53	AdBSerEn	Ser Enable AD B	54	AdBTxDwn	Tx PwrDwn AD B
55	AdBRxDwn	Rx PwrDwn AD B	56	AdBAuClk	Aux. Ser. Clock AD B
57	TRAB6	Gain Transceiver A (B6)	58	TRAB7	Gain Transceiver A (B7)
59	TRAB4	Gain Transceiver A (B4)	60	TRAB5	Gain Transceiver A (B5)
61	TRAB2	Gain Transceiver A (B2)	62	TRAB3	Gain Transceiver A (B3)
63	TRARxhp	RXHP Transceiver A	64	TRAB1	Gain Transceiver A (B1)
65	TRAShdn	SHDN Transceiver A	66	TRARxEna	Transceiver A Receive Ena
67	TRASerClk	Transceiver A Serial Clock	68	TRASerEn	Transceiver A Serial Enable
69	TRATxEna	Transceiver A Tx Ena	70		Not connected

71		Not connected	72		Not connected
73		Not connected	74		Not connected
75		Not connected	76		Not connected
77		Not connected	78		Not connected
79		Not connected	80		Not connected

Table 4 : Pin configuration of QSH connector Bank C

Pin No	Pin Name	Signal Description	Pin No	Pin Name	Signal Description
81	TRBB6	Gain Transceiver B (B6)	82	TRBB7	Gain Transceiver B (B7)
83	TRBB2	Gain Transceiver B (B2)	84	TRBB5	Gain Transceiver B (B5)
85	TRBB4	Gain Transceiver B (B4)	86	TRBB3	Gain Transceiver B (B3)
87	TRBB1	Gain Transceiver B (B1)	88	AdABRst	Reset AD A and B
89	Led2	LED 2	90	AdASerOut	Aux. Ser. Data AD A
91	TRALd	LD Transceiver A	92	Lvttl3	LVTTL I/O 3
93	TRBSerEn	Transceiver B Serial Ena	94	AdBSerOut	Aux. Ser. Data AD B
95	TRBLd	LD Transceiver B	96	Led4	LED 4
97	AntATx	Tx Switch Select, Ch.A	98	SPuAg	PU0g SiGe (PA Switch)
99	AntARx	Rx Switch Select, Ch.B	100	AntBTx	Tx Switch Select, Ch.B
101	SPuAa	PU0a SiGe (PA Switch)	102	SPUBa	PU1a SiGe (PA Switch)
103	AntBRx	Rx Switch Select, Ch.B	104	SPuBg	PU1g SiGe (PA Switch)
105	Led3	LED 3	106	AdBIFace3	IFace3 AD B
107	Lvttl2	LVTTL I/O 2	108	AdBIFace2	IFace2 AD B
109	Lvttl1	LVTTL I/O 1	110	Lvttl4	LVTTL I/O 4
111	TRASerData	Transceiver A Serial Data	112	Led1	LED 1
113	AdAIFace3	IFace3 AD A	114	TRBTxEna	Transceiver B Tx Ena
115	AdAIFace2	IFace2 AD A	116	TRBShdn	SHDN Transceiver B
117	TRBSerClk	Transceiver B Serial Clock	118	TRBRxEna	Transceiver B Receive Ena
119	TRBSerData	Transceiver B Serial Data	120	TRBRxhp	RXHP Transceiver B

2.4 Reference Clock Inputs

Number: Two
Connector Style: MMCX (Female), 50 Ohm, Single-Ended
Assumed Source: external clock resource

One reference clock, **CLK A,** is shared by the two transceiver chips on the MORFAN-1 card. This clock should be a high-quality 40 MHz sinusoid at a level of 2 dBm.

The other reference clock, **CLK B,** is used by the two AD9861 chips on the MORFAN-1 card to generate the sampling clocks. The maximum frequency of this reference clock is up to 80 MHz.

2.5 Antenna Connectors

Number: Two
Connector Style: SMA (Female), 50 Ohm, Single-Ended
Assumed Destination: Dual band antenna

2.6 LEDs

There are 4 LEDs **D1:D4** controlled by the firmware.

LED1 – Lock Detect by Transceiver B
LED2 – Lock Detect by Transceiver A
LED3 – FPGA heart beat
LED4 – Tx/Rx Active Indicator

2.7 Customer I/O Header

The 4-pin header **P1** offers 4 custom I/O pins, which are all directly connected with the FPGA on the base module through the QSH connector. Pin 1 and Pin 2 can be controlled by setting the registers in the firmware to provide the trigger signals.

Pin 1 – Custom usage (LVTTL), Trigger 0 output
Pin 2 – Custom usage (LVTTL), Trigger 1 output
Pin 3 – Custom usage (LVTTL)
Pin 4 – Custom usage (LVTTL)

Note: The LVTTL pins are directly connected to the FPGA pins. They are not 5 V tolerant.

3 Mechanical Specification and Electrical Characteristics

3.1 Mechanical Specification

The mechanical specification of the MORFAN-1 transceiver card follows the SLB design specification for daughter modules in order to make sure that the MORFAN-1 card fits to the Sundance base module.

The physical dimension, including the shape and the positions of MORFAN-1 card interface, is shown in Figure 5. This shape allows access to the SHB (Sundance High-speed Bus) or SRL (Serial Rocket Link or RocketIO connector) on the base module even when MORFAN-1 card is put on the top of base module (for example SMT368). Regarding the SLB standard, the MORFAN-1 card interface consists of the QSH connector for data connection and the BKT connector for power connection. The mated height between the base module and the MORFAN-1 card is 5 mm.

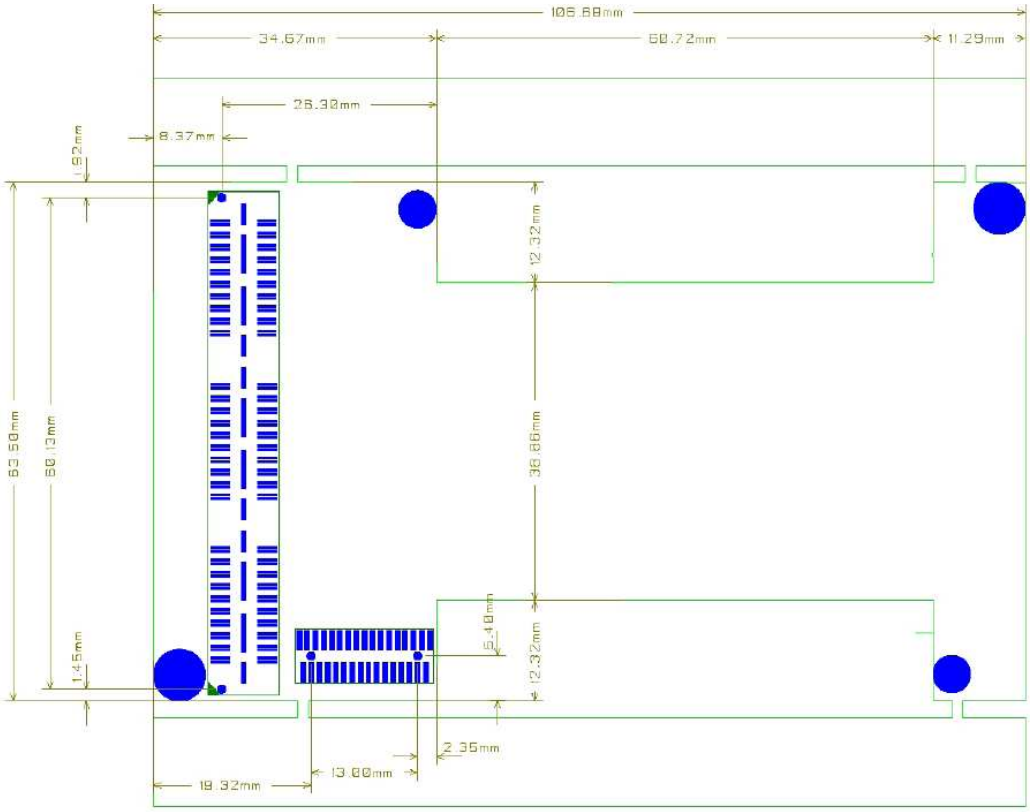


Figure 5 : Physical dimension of the MORFAN-1 transceiver card
(transparent top-view, blue compents are on backside)

3.2 Electrical Characteristics

Each pin on the BKT power connector (33 pins in total) can carry 1.5 A. Digital 5V (D+5V0), digital 3V3 (D+3V3) and digital ground (DGND) are provided over this connector. D+3V3 and D+5V0 are assigned four pins each. The daughter card can thus draw a total of 6A of each of these two supplies. The integral ground plane on the differential connector provides additional grounding.

4 Firmware Implementation

The block diagram of the default firmware is shown in Figure 6. The firmware supports system configuration, controlling and data transfer.

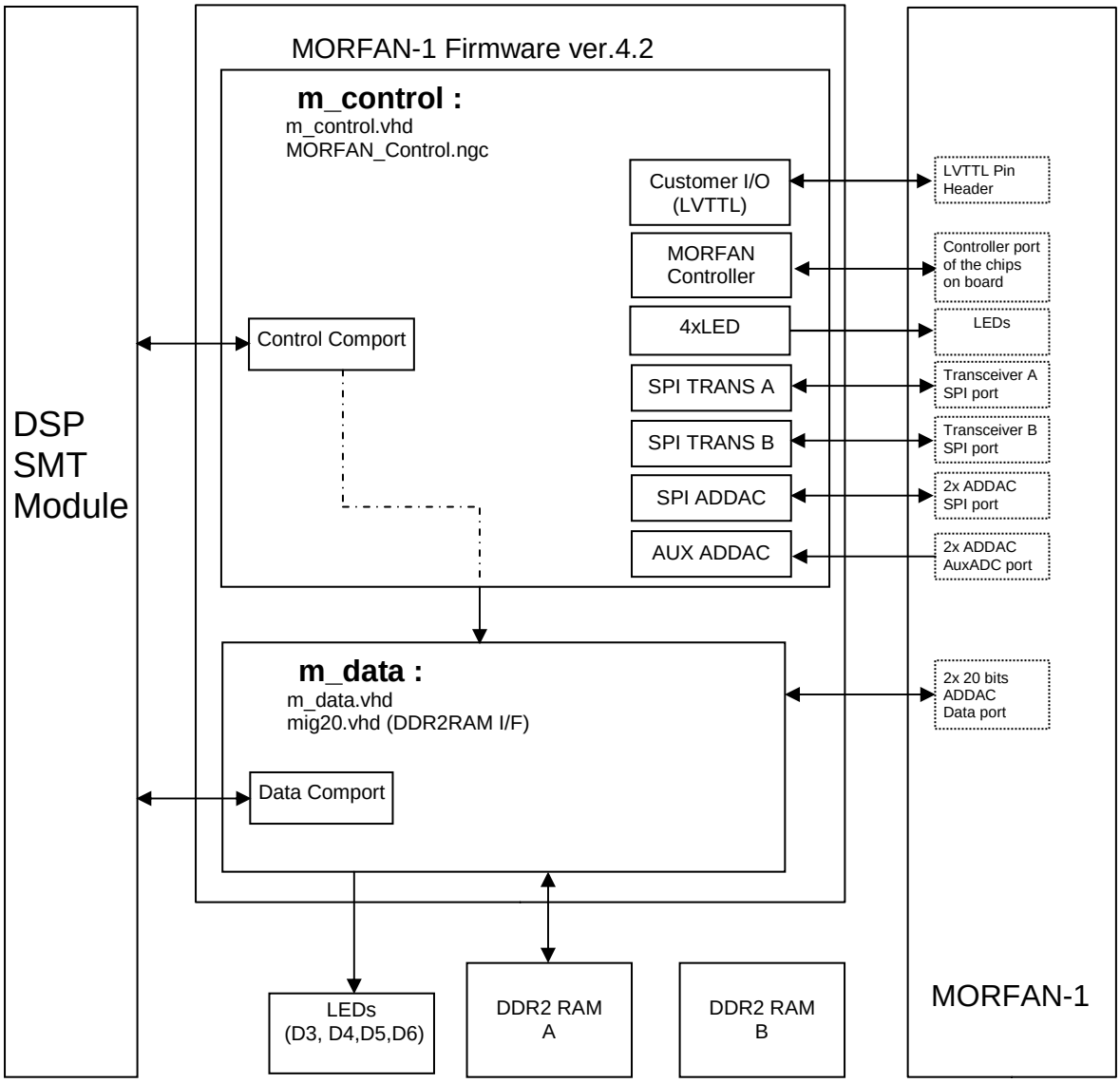


Figure 6 : Block diagram of the default firmware

Functional Overview:

- "m_control" is a block for receiving instructions from DSP module, and controlling MORFAN board. Modules which are integrated in this block are :
  - Control Comport: receive instruction words, and send back read-register to DSP.
  - MORFAN Controller: run switching of MORFAN board.
  - SPI: send SPI signals to every corresponding chip on MORFAN board.
  - AUX ADC: convert the RSSI and Power Detection information into register words.

- “m_data” is a block for data transfer between ADC data ports and DSP Module through Data Comport interface. It is also retrieve a direct control words from DSP module, by getting the forwarded control worlds from Control Comport on “m_control” module. This block supported by DDR2 SRAM interface which available on SMT351 board. DDR2 SRAM is used as data source for continuous transmission (Tx) mode and data buffer for receiving (Rx) mode.

5 Control Register Settings

The registers control the complete functionality of the MORFAN-1 transceiver card. They are set up via the Comport 3 of the base module.

Control Packet Structure

The data passed to the FPGA over the Comports must conform to a certain packet structure. Only valid packets will be accepted and only after acceptance of a packet, the specified settings will be applied. The packet structure is illustrated in Table 5. Byte 0 of a packet must be 0x10 (for writing register) or 0x20 (for reading register). This byte indicates the start of a packet, which is required for the synchronization of the communication. Byte 1 denotes the register address to be accessed. Byte 2 and Byte 3 contain the 16-bit data to be written into or to be read out from the register, where Byte 2 is the upper byte and Byte 3 is the lower byte.

Table 5 : Control Packet Structure for writing (Byte 0 = 0x10)

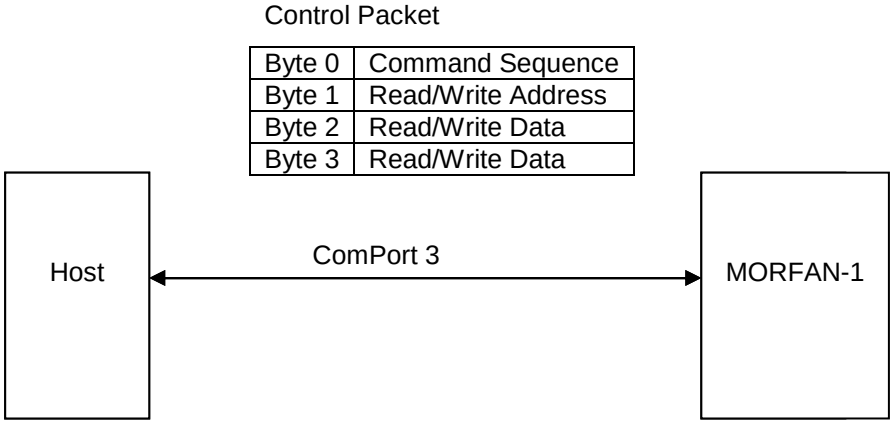
	Byte Content							
Byte	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0	“0”	“0”	“0”	“1”	“0”	“0”	“0”	“0”
1	Addres7	Address6	Address5	Address4	Address3	Address2	Address1	Address0
2	Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
3	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

Table 6 : Control Packet Structure for reading (Byte 0 = 0x20)

	Byte Content							
Byte	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0	“0”	“0”	“1”	“0”	“0”	“0”	“0”	“0”
1	Addres7	Address6	Address5	Address4	Address3	Address2	Address1	Address0
2	Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
3	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0

Reading and Writing Registers

Control packets are sent to the base module over the Comport 3. This is a bi-directional interface.



Register Map

The write packets must contain the address where the data shall be written to and the read packets must contain the address where the required data shall be read. The following figure shows the memory map for the writeable and readable control registers on the MORFAN-1 transceiver card.

Table 7 : Register Map

Address	Register Definitions	Read/Write	Address	Register Definitions	Read/Write
0x00	Reset Register	Write-only	**0x1D**	ADDAC A Register 3	R/W
0x01	Test Register	R/W	**0x1E**	ADDAC A Register 4	R/W
0x02	Function Register 0	R/W	**0x1F**	ADDAC A Register 5	R/W
0x03	Function Register 1	R/W	**0x20**	ADDAC A Register 6	R/W
0x04	Function Register 2	R/W	**0x21**	ADDAC A Register 7	R/W
0x05	Function Register 3	R/W	**0x22**	ADDAC A Register 8	R/W
0x06	Transceiver A Register 0	R/W	**0x23**	ADDAC A Register 9	R/W
0x07	Transceiver A Register 1	R/W	**0x24**	ADDAC A Register 10	R/W
0x08	Transceiver A Register 2	R/W	**0x25**	ADDAC A Register 11	R/W
0x09	Transceiver A Register 3	R/W	**0x26**	ADDAC A Register 12	R/W
0x0A	Transceiver A Register 4	R/W	**0x27**	ADDAC A Register 13	R/W
0x0B	Transceiver A Register 5	R/W	**0x28**	ADDAC B Register 0	R/W
0x0C	Transceiver A Register 6	R/W	**0x29**	ADDAC B Register 1	R/W
0x0D	Transceiver A Register 7	R/W	**0x2A**	ADDAC B Register 2	R/W
0x0E	Transceiver A Register 8	R/W	**0x2B**	ADDAC B Register 3	R/W
0x0F	Transceiver A Register 9	R/W	**0x2C**	ADDAC B Register 4	R/W
0x10	Transceiver B Register 0	R/W	**0x2D**	ADDAC B Register 5	R/W
0x11	Transceiver B Register 1	R/W	**0x2E**	ADDAC B Register 6	R/W
0x12	Transceiver B Register 2	R/W	**0x2F**	ADDAC B Register 7	R/W
0x13	Transceiver B Register 3	R/W	**0x30**	ADDAC B Register 8	R/W
0x14	Transceiver B Register 4	R/W	**0x31**	ADDAC B Register 9	R/W
0x15	Transceiver B Register 5	R/W	**0x32**	ADDAC B Register 10	R/W
0x16	Transceiver B Register 6	R/W	**0x33**	ADDAC B Register 11	R/W
0x17	Transceiver B Register 7	R/W	**0x34**	ADDAC B Register 12	R/W
0x18	Transceiver B Register 8	R/W	**0x35**	ADDAC B Register 13	R/W
0x19	Transceiver B Register 9	R/W	**0x36**	Update Register	R = Firmware Version; W = Update SPI.
0x1A	ADDAC A Register 0	R/W	**0x37**	Update RSSI/PWDT	Write-Only
0x1B	ADDAC A Register 1	R/W	**0x38**	RSSI/PWRDT CH A	Read-Only
0x1C	ADDAC A Register 2	R/W	**0x39**	RSSI/PWRDT CH B	Read-Only

5.1 Register Description

Reset Register – 0x00

This register is used to reset some components.

Reset Register – 0x00																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"00000000000000"														1	1

Note: The Reset bits do not get cleared automatically, so the device can remain in reset mode while not used, in order to reduce the global power dissipation.

Reconfigurable register:

Bit	Default	Description

1	1	ADQ A & B Reset, “1” = reset, “0” = normal operation
0	0	Transceiver A & B Reset ; “1”= reset, “0” = normal operation

Test Register – 0x01

Any 16-bit value written in this register can be read-back to check that the Comport used works properly.

Test Register – 0x01																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	1	1	1	1	0	0	0	0	1	0	1	0	1	0	1	0

Function Register 0 – 0x02 (MIMO activation)

This register allows the basic setup of MORFAN-1 transceiver card, which are activating MIMO system, choose the frequency band of operation, select memory, and define the transmitter or receiver function.

Function Register 0 – 0x02																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	“000000000000”												0	0	1	1

Reconfigurable bits of the register:

Bit	Default	Description
3	0	“0” =use memory (ZBT RAM) , “1” = no memory (direct transfer)
2	0	Working mode. “1” = Receiver, “0” = Transmitter
1	1	Frequency range. “0” = 2.4 GHz (802.11g), “1” = 5.2 GHz (802.11a)
0	1	**MIMO activation**. “0” = SISO mode (only path A available), **“1” = MIMO active**

Function Register 1 – 0x03 (Receiver & Transmitter Switching)

This register controls the switching of the MORFAN-1 transceiver card, either active (transmit or receive) or standby.

Function Register 1 – 0x03																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	Reserved “00000000”								0	0	0	0	0	0	0	0

Reconfigurable bits of the register:

Bit	Default	Description
7	0	“1” = Write to Memory, “0”= Stop write to memory
6	0	“1” = Read from memory, “0”= not read from memory
5	0	“000000” = standby “111111” = active (actual working mode depends on Reg. 0x02) Any other combinations doesn’t affect actual situation.
4	0	
3	0	
2	0	
1	0	
0	0	

Function Register 2 – 0x04 (External Trigger)

This register controls the state of trigger signals.

Function Register 2 – 0x04

Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	“00000000000000”														0	0

Reconfigurable bits of the register:

Bit	Default	Description
1	0	Trigger1. “0” = LOW state; “1” = HIGH state.
0	0	Trigger0. “0” = LOW state; “1” = HIGH state.

Function Register 3 – 0x05 (digital gain control of transceiver chips)

By default, the gain control is applied through the parallel digital inputs of the transceiver chips. This register is used to set these digital inputs.

Function Register 3 – 0x05																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	“00”		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reconfigurable bits of the register:

Bit	Default	Description
13	0	Bit13:Bit7, are digital gain control for Transceiver B. **As Receiver** B13:B12 are used for Rx LNA gain control. “00”&“01” = minimum, “10” = medium, “11” = maximum. B11:B7 are used for Rx VGA gain control. “00000” = 0 dB (minimum), “11111” = 62 dB (maximum). **As Transmitter** B13 is not used, B12:B7 is used for Tx VGA gain control. “000000” = 0 dB (minimum), “111111” = 30 dB (maximum)
12	0	
11	0	
10	0	
9	0	
8	0	
7	0	
6	0	Bit6:Bit0, are digital gain control for Transceiver A. **As Receiver** B6:B5 are used for Rx LNA gain control. “00”&“01” = minimum, “10” = medium, “11” = maximum. B4:B0 are used for Rx VGA gain control. “00000” = 0 dB (minimum), “11111” = 62 dB (maximum). **As Transmitter** B6 is not used, B5:B0 is used for Tx VGA gain control. “000000” = 0 dB (minimum), “111111” = 30 dB (maximum)
5	0	
4	0	
3	0	
2	0	
1	0	
0	0	

Transceiver A Register 0 – 0x06 (Standby)

Various internal blocks of the transceiver chip can be turned on or off by setting this standby register. Setting Bit 13 to 1 turns the block on, while setting it to 0 turns the block off.

Transceiver A Register 0 – 0x06																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	“00”		0	“1”	0	0	“0000000”							“111”		

Reconfigurable bits of the register:

Bit	Default	Description
13	1	**MIMO operation mode.** “0” = Normal operation; **“1” = MIMO applications**
11	0	Voltage Reference
10	0	PA Bias DAC, in Tx Mode

Transceiver A Register 1 – 0x07 (Integer-Divider Ratio)

This register contains the integer portion of the divider ratio of the synthesizer. This register in conjunction with the fractional-divider ratio register, permits selection of a precise frequency. Please refer to the appendix table 8 and 9.

Transceiver A Register 1 – 0x07																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"00"		1	1	"0000"				1	0	1	0	0	0	1	0

Reconfigurable bits of the register:

Bit	Default	Description
13	1	2 LSBs of the Fractional-Divider Ratio.
12	1	
7	1	Integer-Divider Ratio Word Programming Bits. Valid values are from 128(Bit7:Bit0 = "10000000") to 255 (Bit7:Bit0 = "11111111")
6	0	
5	1	
4	0	
3	0	
2	0	
1	1	
0	0	

Transceiver A Register 2 – 0x08 (Fractional-Divider Ratio)

This register (along with bit 13 and bit 12 of the integer divider ratio register) controls the fractional-divider ratio with 16-bit resolution. Bit 13 to bit 0 of this register combined with bit 13 and bit 12 of the integer-divider ratio register form the whole fractional-divider ratio. To retain the complete frequency plan please refer to the appendix table 8 and 9.

Transceiver A Register 2 – 0x08																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"00"		0	1	1	1	0	1	1	1	0	1	1	1	0	1

Reconfigurable bits of the register:

Bit	Default	Description
13	0	Bit0:Bit13 = refer to Appendix : Frequency Plan and Divider Ratio Programming Words
12	1	
11	1	
10	1	
9	0	
8	1	
7	1	
6	1	
5	0	
4	1	
3	1	
2	1	
1	0	
0	1	

Transceiver A Register 3 – 0x09 (Band Select and PLL)

This register configures the programmable-reference frequency dividers for the synthesizer, and sets the DC current for the charge pump. The programmable

reference frequency divider provides the reference frequency to the phase detector by dividing the signal of the crystal oscillator.

Transceiver A Register 3 – 0x09																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"00"		1	"11"		0	0	0	0	0	1	"0"	0	1	0	0

Reconfigurable bits of the register:

Bit	Default	Description
13	1	"0" = Normal operation; **"1" = MIMO applications**
10	0	These Bits set the VCO Sub-Band when programmed by using SPI (Bit8=1). "00" = lowest frequency band; "11" = highest frequency band.
9	0	
8	0	VCO SPI Bandswitch Enable. "0" = disable SPI control, bandswitch is done by FSM; "1" = bandswitch is done by SPI programming.
7	0	VCO Bandswitch Enable. "0" = disable; "1" = start automatic bandswitch.
6	0	RF Frequency Band Select in 802.11a Mode (Bit0=1). "0" = 4.9GHz to 5.35GHz Band; "1" = 5.47GHz to 5.875GHz Band.
5	1	PLL Charge-Pump-Current Select. "0" = 2mA, "1" = 4mA.
3	0	These Bits Set the Reference-Divider Ratio. "001" corresponds to R = 1 and "111" corresponds to R = 7.
2	1	
1	0	
0	0	RF Frequency Band Select. "0" = 2.4GHz Band; "1" = 5GHz band.

Transceiver A Register 4 – 0x0A (Calibration)

This register configures the RX/TX calibration modes.

Transceiver A Register 4 – 0x0A																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"000"			1	1	"1"	"00000000"								0	0

Reconfigurable bits of the register:

Bit	Default	Description
12	1	Transmitter I/Q Calibration LO Leakage and Sideband-Detector Gain-Control Bits. "00" = 8 dB; "01" = 18 dB; "10" = 24 dB; "11" = 34 dB
11	1	
1	0	"0" = TX Calibration Mode Disabled; "1" = TX Calibration Mode Enabled
0	0	"0" = RX Calibration Mode Disabled; "1" = RX Calibration Mode Enabled

Transceiver A Register 5 – 0x0B (Low-pass Filter)

This register allows the adjustment of the RX and TX low-pass filter corner frequencies.

Transceiver A Register 5 – 0x0B																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"0000"				0	"0000"				0	1	0	1	0	1	0

Reconfigurable bits of the register

Bit	Default	Description
11	0	RSSI High Bandwidth Enable. "0" = 2 MHz; "1" = 6MHz
6	0	TX LPF Corner Frequency Coarse Adjustment. "00" = undefined; "01" = 12MHz (nominal mode); "10" = 18MHz (turbo mode 1); "11" = 24MHz (turbo mode 2).
5	1	
4	0	RX LPF Corner Frequency Coarse Adjustment. "00" = 7.5MHz; "01" = 9.5MHz (nominal mode); "10" = 14 MHz (turbo mode 1); "11" = 18MHz (turbo mode 2).
3	1	
2	0	RX LPF Corner Frequency Fine Adjustment (Relative to the Course Setting). "000" = 90%; "001" = 95%; "010" = 100%; "011" = 105%; "100" =110%.
1	1	

0	0	

Transceiver A Register 6 – 0x0C (RX Control/RSSI)

This register is used to adjust the RX section and the RSSI output.

Transceiver A Register 6 – 0x0C																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"000"			0	0	0	"0"	0	"00"		'1'	"00"		1	"01"	

Reconfigurable bits of the register:

Bit	Default	Description
12	0	Enable Rx VGA Gain Programming Serially. "0" = Rx VGA gain programmed with external digital inputs (B7:B1); "1" = Rx VGA gain programmed with serial data bits in the Rx gain register (D6:D0).
11	0	RSSI Output Range. "0" = low range (0.5V to 2V); "1" = high range (0.5V to 2.5V).
10	0	RSSI Operating Mode. "0" = RSSI disabled if RXHP = 0, and enabled if RXHP = 1; "1" = RSSI enabled independent of RXHP
8	0	RSSI Pin Function. "0" = outputs RSSI signal in Rx mode; "1" = outputs temperature sensor voltage in Rx, Tx and standby modes.
2	1	Rx high-pass -3dB Corner Frequency when RXHP = 0. "0" = 100Hz; "1" = 30kHz

Transceiver A Register 7 – 0x0D (Tx Linearity/Base-band Gain)

This register allows the adjustment of the Tx gain and linearity.

Transceiver A Register 7 – 0x0D																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"00000"					0	1	0	0	0	"00"		0	0	0	0

Reconfigurable bits of the register:

Bit	Default	Description
10	0	Enable Tx VGA Gain Programming Serially. "0" = Tx VGA gain programmed with external digital inputs (B6:B1); "1" = Tx VGA gain programmed with data bits in the Tx gain register (D5:D0).
9	1	PA Driver linearity. "00" = 50% current (minimum linearity); "01" = 63% current; "10" = 78% current; "11" = 100% current (maximum linearity)
8	0	
7	0	Tx VGA linearity. "00" = 50% current (minimum linearity); "01" = 63% current; "10" = 78% current; "11" = 100% current (maximum linearity)
6	0	
3	0	Tx Upconverter Linearity. "00" = 50% current (minimum linearity); "01" = 63% current; "10" = 78% current; "11" = 100% current (maximum linearity).
2	0	
1	0	Tx Base-band Gain. "00" = max base-band gain -5dB; "01" = max base-band gain -3dB; "10" = max base-band gain -1.5dB; "11" = max base-band gain.
0	0	

Transceiver A Register 8 – 0x0E (Rx Gain)

This register (Rx Gain Register) sets the Rx base-band and RF gain when Transceiver A register 6 (Rx Control/RSSI register), Bit12 = "1".

Transceiver A Register 8 – 0x0E																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"000000000"									1	1	1	1	1	1	1

Reconfigurable bits of the register:

Bit	Default	Description	
6	1	Rx LNA Gain Control	Rx base-band and RF gain-control bits. Bit6 maps to digital input pin B1. Bit6:BitD0 =
5	1		

4	1	Rx VGA Gain Control	“0000000” corresponds to minimum gain.
3	1		
2	1		
1	1		
0	1		

Transceiver A Register 9 – 0x0F (Tx VGA Gain)

This register sets the Tx VGA gain when Transceiver Register 7 (Linearity/Base-band Gain Register), Bit10 = “1”.

Transceiver A Register 9 – 0x0F																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	“0000000000”										0	0	0	0	0	0

Reconfigurable bits of the register:

Bit	Default	Description
5	0	For faster Tx VGA gain setting, only Bit5:Bit0 need to be programmed. Tx VGA Gain Control. Bit5 maps to digital input pin B6 and Bit0 maps to digital input pin B1. Bit5:Bit0 = “000000” corresponds to minimum gain.
4	0	
3	0	
2	0	
1	0	
0	0	

Transceiver B Register 0 – 0x10 (Standby)
Refer to Transceiver A Register 0

Transceiver B Register 1 – 0x11 (Integer-Divider Ratio)
Refer to Transceiver A Register 1

Transceiver B Register 2 – 0x12 (Fractional-Divider Ratio)
Refer to Transceiver A Register 2

Transceiver B Register 3 – 0x13 (Band Select and PLL)
Refer to Transceiver A Register 3

Transceiver B Register 4 - 0x14 (Calibration)
Refer to Transceiver A Register 4

Transceiver B Register 5 - 0x15 (Low-pass Filter)
Refer to Transceiver A Register 5

Transceiver B Register 6 – 0x16 (Rx Control/RSSI)
Refer to Transceiver A Register 6

Transceiver B Register 7 – 0x17 (Tx Linearity/Base-band Gain)
Refer to Transceiver A Register 7

Transceiver B Register 8 – 0x18 (Rx Gain)
Refer to Transceiver A Register 8

Transceiver B Register 9 – 0x19 (Tx VGA Gain)
Refer to Transceiver A Register 9

ADDAC A Register 0 – 0x1A

This register is used for general setting and clock mode of ADDAC A.

ADDAC A Register 0 – 0x1A																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	"00"		0	0	"0"	1	0	0	"00000"				

Reconfigurable bits of the register:

Bit	Default	Description
15	0	Clock Mode setting. "000" standard FD, HD10, HD20 (modes 1,4,7); "001" Optional FD timing (mode 2) ; "010" not used; "011" Optional HD20 timing (mode 5); "100" not used; "101" Optional HD10 timing (mode 8); "110" not used; "111" Clone Mode (mode 10)
14	0	
13	0	
10	0	Enable the IFACE2 port to be an output clock
9	0	Inv the output clock on IFACE3
7	1	SDIO pin. "0" = uni-directional ; "1" = bidirectional
6	0	SPI Mode. "0" = MSB; "1" = LSB
5	0	Soft Reset. "0" = not reset; "1" = reset register to default value

ADDAC A Register 1 – 0x1B

This register is used to set Power-Down mode of ADDAC A.

ADDAC A Register 1 – 0x1B																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	"000000"						0	0	0	0	0	0	0	"0"

Reconfigurable bits of the register:

Bit	Default	Description
15	0	Rx_A Analog Power-Down. "0" = active; "1" = Power-down
14	0	Rx_A DC Bias Analog Power-Down. "0" = active; "1" = Power-down
7	0	Power Down Tx Analog. "000" = default; "100 = Power down Tx A; "010" = Power-Down Tx B; "111 = Power-Down Tx A and Tx B
6	0	
5	0	
4	0	Tx Digital Power-Down. "0" = active; "1" = Power-down
3	0	Rx Digital Power-Down. "0" = active; "1" = Power-down
2	0	PLL Power-Down. "0" = active; "1" = Power-down
1	0	PLL Output Disconnect. "0" = connect; "1" = disconnect

ADDAC A Register 2 – 0x1C

This register is used to set Power-Down of ADDAC A.

ADDAC A Register 2 – 0x1C																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	"0000"				0	0	"000000"					

Reconfigurable bits of the register:

Bit	Default	Description
15	0	Rx Analog Bias Power-Down. "0" = active; "1" = Power-Down
14	0	RxRef Power-Down. "0" = active; "1" = Power-Down
13	0	DiffRef Power-Down. "0" = active; "1" = Power-Down
12	0	VREF Power-Down. "0" = active; "1" = Power-Down
7	0	Rx_B Analog Power-Down. "0" = active; "1" = Power-down

6	0	Rx_B DC Bias Power-Down. “0” = active; “1” = Power-down

ADDAC A Register 3 – 0x1D

This register is used to set Rx Path of ADDAC A.

ADDAC A Register 3 – 0x1D																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	“00”		0	0	“000000”						0	0	“0000”			

Reconfigurable bits of the register:

Bit	Default	Description
13	0	Rx_B 2’s complement. “0” = straight binary; “1” = 2’s complement
12	0	Rx_B Clk Duty. “0” = disable; “1” = enable
5	0	Rx_A 2’s complement. “0” = straight binary; “1” = 2’s complement
4	0	Rx_A Clk Duty. “0” = disable; “1” = enable

ADDAC A Register 4 – 0x1E

This register is used to set Ultra low power control of Rx path of ADDAC A, in combination with asserting the ADC_LO_PWR pin to reduce power consumption.

ADDAC A Register 4 – 0x1E																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	“0”	0	0	0	“00000000”								0	0	“00”	

Reconfigurable bits of the register:

Bit	Default	Description
14	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
13	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
12	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
3	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
2	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow

ADDAC A Register 5 – 0x1F

This register is used to set Ultra low power control of Rx path and DAC A Offset of ADDAC A.

ADDAC A Register 5 – 0x1F																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	“0”	0	0	0	“0000”			

Reconfigurable bits of the register:

Bit	Default	Description
15	0	DAC A Offset [9:2]
14	0	
13	0	
12	0	
11	0	
10	0	
9	0	
8	0	
6	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow
5	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow

4	0	Rx Ultralow PowerControl. “0” = normal; “1” = set to Ultralow

ADDAC A Register 6 – 0x20

This register is used for DAC A offset and DAC A gain control of ADDAC A.

ADDAC A Register 6 – 0x20																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	0	0	“00000”					0

Reconfigurable bits of the register:

Bit	Default	Description
15	0	DAC A Coarse Gain Control. “00” = output current scaling by 1/11; “01” = output current scaling by ½; “10” and “11” = no output current scaling
14	0	
13	0	DAC A Fine Gain [5:0] := “100000” Maximum positive gain adjustment; “111111” Minimum positive gain adjustment; “000000” default of no adjustment; “000001” Minimum negative gain adjustment; “011111” Maximum negative gain adjustment
12	0	
11	0	
10	0	
9	0	
8	0	
7	0	DAC A Offset [1:0]
6	0	
0	0	DAC A Offset Direction. “0” = to negative diff. pin; “1” = to positive diff. pin

ADDAC A Register 7 – 0x21

This register is used for DAC B offset and its direction of ADDAC A.

ADDAC A Register 7 – 0x21																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	‘00000’					0	0	0	0	0	0	0	0	0

Reconfigurable bits of the register:

Bit	Default	Description
15	0	DAC B Offset [1:0]
14	0	
8	0	DAC B Offset Direction. “0” = to negative diff. pin; “1” = to positive diff. pin
7	0	DAC B Offset [9:2]
6	0	
5	0	
4	0	
3	0	
2	0	
1	0	
0	0	

ADDAC A Register 8 – 0x22

This register is used for DAC B offset gain control, fine gain, and TxPGA gain of ADDAC A.

ADDAC A Register 8 – 0x22																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Reconfigurable bits of the register:

Bit	Default	Description
15	1	TxPGA Gain [7:0], is register control for the Tx programmable gain amplifier (TxPGA). The TxPGA provides a 20 dB continuous gain range with 0.1 dB steps (linear in dB) simultaneously to both Tx channels. Default is 0xFF. “0000 0000” = Minimum gain scaling -20 dB “1111 1111” = Maximum gain scaling 0dB
14	1	
13	1	
12	1	
11	1	
10	1	
9	1	
8	1	
7	0	DAC B Coarse Gain Control. “00” = output current scaling by 1/11; “01” = output current scaling by ½; “10” and “11” no output current scaling
6	0	
5	0	DAC B Fine Gain [5:0] := “100000” Maximum positive gain adjustment; “111111” Minimum positive gain adjustment; “000000” default of no adjustment; “000001” Minimum negative gain adjustment; “011111” Maximum negative gain adjustment
4	0	
3	0	
2	0	
1	0	
0	0	

ADDAC A Register 9 – 0x23

This register is used for other settings of Tx Path and I/O configuration of ADDAC A.

ADDAC A Register 9 – 0x23																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	“000”			0	0	“0”	0	“0”	0	“0000”			

Reconfigurable bits of the register:

Bit	Default	Description
15	0	Tx Twos Complement. “0” = straight binary; “1” = twos complement
14	0	Rx Twos Complement. “0” = straight binary; “1” = twos complement
13	0	Tx Inverse Sample. “0” = sampled on rising edge; “1” = sampled on falling edge clock
9	0	Interpolation control. “00” = filters bypassed; “01” = interpolation rate 2x; “10” = interpolation rate 4x.
8	0	
6	0	TxPGA Slave Enable. “0” = immediately after register updated; “1” = synchronized with falling edge of a signal applied to the TxPwrDwn
4	0	TxPGA Fast Update. “0” = normal mode; “1” = fast mode

ADDAC A Register 10 – 0x24

This register is used for I/O configuration and clock configuration of ADDAC A.

ADDAC A Register 10 – 0x24																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	“0”	0	0	0	0	0	0	“00”		0	0	0	0	0	0

Reconfigurable bits of the register:

Bit	Default	Description
15	0	PLL Bypass. “0” = PLL remains active; “1” = PLL bypassed
13	0	ADC Clock Div. “0” = no division; “1” = divides the clock by 2
12	0	Alt timing mode. “0” = normal timing operation; “1” = alternative operation mode
11	0	PLL Div5. “0” = no division; “1” = output of PLL divided by 5
10	0	PLL multiplication factor. “000” = 1x; “001” = 2x; “010” = 4x; “011” = 8x; “100” = 16x; “101” ~ “111”: not used.
9	0	
8	0	

5	0	Dig Loop On. “0” = off; “1” = on (on only in full duplex mode)
4	0	SpiFDnHD. “0” = HD mode; “1” = FD mode
3	0	SpiTxnRx for toggling Tx & Rx in HD mode. “0” = Rx; “1” = Tx
2	0	SpiB10n20, option for 10 or 20 bit. “0” = 20-bit; “1” = 10-bit
1	0	SPI IO Control, in conjunction with Bit3 to override external TxnRx pin operation
0	0	SpiClone. “1” = for clone mode; “0” = other

ADDAC A Register 11 – 0x25

This register is used for configuring clock and Auxiliary converters of ADDAC A.

ADDAC A Register 11 – 0x25																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	1	1	“00”		0	“00”		0	“00”	

Reconfigurable bits of the the register:

Bit	Default	Description
15	0	AuxDAC A FS [1:0]. “00” = 3.0 V; “01” = 3.3 V; “10” = 2.5 V; “11” = 2.7 V
14	0	
13	0	AuxDAC B FS [1:0]. “00” = 3.0 V; “01” = 3.3 V; “10” = 2.5 V; “11” = 2.7 V
12	0	
11	0	AuxDAC C FS [1:0]. “00” = 3.0 V; “01” = 3.3 V; “10” = 2.5 V; “11” = 2.7 V
10	0	
9	1	AuxADC Ref Enabe, “0” = use PLLAVDD as FS, “1” = enable user to select FS
8	1	If Bit 9 set high, allow user to select Ref FS; “0” = 3.0V, “1” = 2.5V
5	0	PLL to IFACE2. “0” = IFACE2 normal; “1” = IFACE2 switched to PLL output clock (FD)
2	0	PLL Slow. “0” = standard; “1” = changes phase noise generated from the PLL clock

ADDAC A Register 12 – 0x26

This register is used to start the averaging of Auxiliary ADC and define the sample numbers of ADDAC A.

ADDAC A Register 12 – 0x26																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	“0000”				0	0	0	0	“0000”				0	0	0

Reconfigurable bits of the the register:

Bit	Default	Description
15	0	Start Average AuxADC B when set to 1
10	0	Number of AuxADC B. “000” = 1 ; “001” = 2; “010” = 4; “011” = 8; “100” = 16; “101” = 32; “110” = 64; “111”: Not used
9	0	
8	0	
7	0	Start Average AuxADC A when set to 1
2	0	Number of AuxADC A. “000” = 1 ; “001” = 2; “010” = 4; “011” = 8; “100” = 16; “101” = 32; “110” = 64; “111”: Not used
1	0	
0	0	

ADDAC A Register 13 – 0x27

This register contains some settings for AuxADC of ADDAC A.

ADDAC A Register 13 – 0x27																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	“000000”						0	0	1	0	1	“0”	0	1	0	0

Reconfigurable bits of the the register:

Bit	Default	Description
9	0	AuxADC Clock Divider. “00” = Rx ADC Clock/4; “01” = Rx ADC Clock/2; “10” = Rx ADC Clock; “11” = SPI_CLK drives AuxADC
8	0	
7	1	Enable the AuxSPI. “0” = disable; “1” = enable
6	0	Select which AuxADC is activated. “0” = (port A1&A2=RSSI); “1” = (port B=PD)
5	1	Reference select B (full-scale voltage). “0” = use AUX_REF pin; “1” = use internal
3	0	Setting this bit high to initiate a conversion of AuxADC B
2	1	Reference select A (full-scale voltage). “0” = use AUX_REF pin; “1” = use internal
1	0	Select inputs connected to AuxADC. “0” = Aux_ADC_A2; “1” = Aux_ADC_A1
0	0	Setting this bit high to initiate a conversion of AuxADC A

ADDAC B Register 0 – 0x28
Refer to ADDAC A Register 0.

ADDAC B Register 1 – 0x29
Refer to ADDAC A Register 1.

ADDAC B Register 2 – 0x2A
Refer to ADDAC A Register 2.

ADDAC B Register 3 – 0x2B
Refer to ADDAC A Register 3.

ADDAC B Register 4 – 0x2C
Refer to ADDAC A Register 4.

ADDAC B Register 5 – 0x2D
Refer to ADDAC A Register 5.

ADDAC B Register 6 – 0x2E
Refer to ADDAC A Register 6.

ADDAC B Register 7 – 0x2F
Refer to ADDAC A Register 7.

ADDAC B Register 8 – 0x30
Refer to ADDAC A Register 8.

ADDAC B Register 9 – 0x31
Refer to ADDAC A Register 9.

ADDAC B Register 10 – 0x32
Refer to ADDAC A Register 10.
.

ADDAC B Register 11 – 0x33
Refer to ADDAC A Register 11.

ADDAC B Register 12 – 0x34
Refer to ADDAC A Register 12.

ADDAC B Register 13 – 0x35

Refer to ADDAC A Register 13.

Update Register – 0x36

The Update bit activates the Serial Interface to pass registers previously written in the FPGA into the corresponding device (Transceiver A and B, and ADDAC A&B).

Update Register – 0x36																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"000000000000"												1	1	1	1

Reading-back this register returns the Firmware version.

Update Register – 0x36																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0	Firmware version "10101010"							

Reconfigurable bits of the register:

Bit	Default	Description
3	1	ADDAC B Update. "0" = not updated; "1" = updated
2	1	ADDAC A Update. "0" = not updated; "1" = updated
1	1	Transceiver B Update. "0" = not updated; "1" = updated
0	1	Transceiver A Update. "0" = not updated; "1" = updated

Update RSSI/PWDT Register – 0x37

This register is to update the RSSI/PWDT values.

Update RSSI/PWDT Register – 0x37																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"00000000000000"														0	0

Reconfigurable bits of the register:

Bit	Default	Description
1	0	"0" = not updated, "1" = update RSSI / Power Detect of Channel B
0	0	"0" = not updated, "1" = update RSSI / Power Detect of Channel A

RSSI/PWDT CH.A Storage Register – 0x38

This register is a read-only register, to retrieve RSSI/PWDT of Channel A.

RSSI/PWDT CH.A Storage Register – 0x38																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"000000"						A[9:0]									

RSSI/PWDT CH.B Storage Register – 0x39

This register is a read-only register, to retrieve RSSI/PWDT of Channel B.

RSSI/PWDT CH.B Storage Register – 0x39																
Byte 1-0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	"000000"						B[9:0]									

6 Operating Procedures

The operations of the MORFAN-1 card are controlled via the firmware registers. Figure 8 illustrates the operating. At first, some registers of the firmware shall be initialized. They are relative with the settings of MIMO activation, frequency range, digital gain control, transmitter/receiver function, ZBT RAM implementation, and RSSI or Power-detect selection. Any other registers which are not described in this diagram must follow the default settings in the previous section, and before changing any default value please refer to data sheets of the relevant chips.

The second step is to reset the chips (ADDACs and Transceivers) on the MORFAN-1 card in order to guarantee the default setting of each chip. Note that the reset registers will not be automatically cleaned. Hence, the reset value should be cleaned later.

The third step is to update the chip registers. The register values in the firmware are sent to the corresponding chips.

The next step can follow two different branches. If the MORFAN-1 transceiver card acts as transmitter, the process should follow the steps listed in the block for transmitter. If ZBT RAMs are used for the data resource, the prepared data will be firstly written into the ZBT RAMs and later the data resource is realized by reading the ZBT RAMs continuously and cyclically. On the other hand, data can be sent directly from SHB to ADDAC if bypass mode is chosen. During transmission, the value of Power Detection can be retrieved from the certain registers, as shown in the figure. To stop the transmission zero value can be sent to *Function Register 1 – 0x03*.

If MORFAN-1 card is configured as receiver, the process should follow the steps listed in the block for receiver. ZBT RAMs can be chosen here to buffer the received data and later the data will be forwarded to SHB. During receiving, the RSSI value can be retrieved from the registers. Similar to transmitter function, the receiver function is ended by sending zero values to *Function Register 1 – 0x03*.

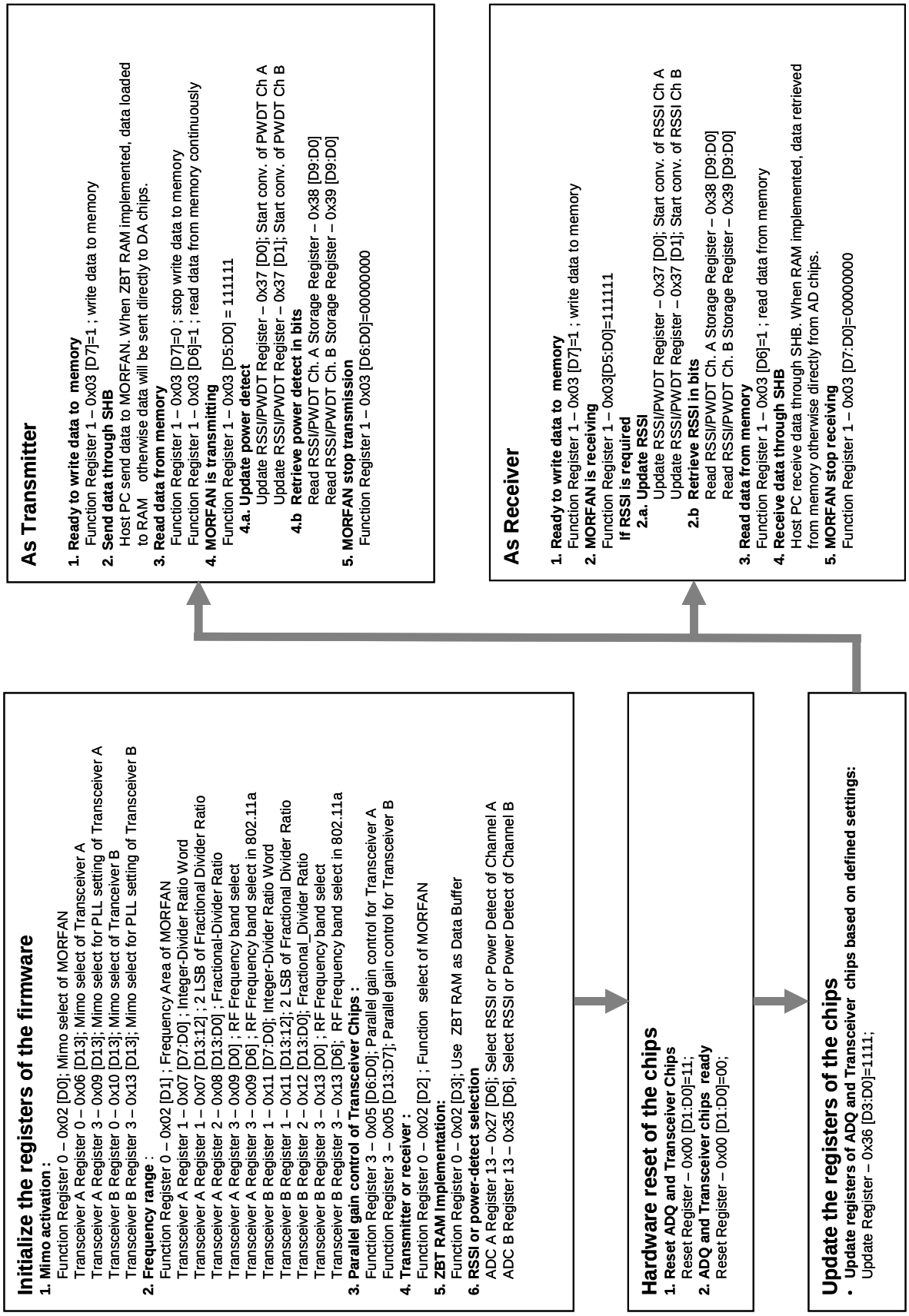


Figure 7 : Operating Procedures

7 Appendix

Table 8 : 2.4 GHz Frequency Plan and Divider Ratio Programming Words

fRF (MHz)	(fRF x 4/3) / 20MHz (DIVIDER RATIO)	INTEGER-DIVIDER RATIO	FRACTIONAL-DIVIDER RATIO	
		Reg 0x09, Bit7:Bit0	Reg 0x0A, Bit13:Bit0(hex)	Reg 0x09, Bit13:Bit12
2412	160.8000	1010 0000	3333	00
2417	161.1333	1010 0001	0888	10
2422	161.4667	1010 0001	1DDD	11
2427	161.8000	1010 0001	3333	00
2432	162.1333	1010 0010	0888	10
2437	162.4667	1010 0010	1DDD	11
2442	162.8000	1010 0010	3333	00
2447	163.1333	1010 0011	0888	10
2452	163.4667	1010 0011	1DDD	11
2457	163.8000	1010 0011	3333	00
2462	164.1333	1010 0100	0888	10
2467	164.4667	1010 0100	1DDD	11
2472	164.8000	1010 0100	3333	00
2484	165.6000	1010 0101	2666	01

Table 9 : 5 GHz Frequency Plan and Divider Ratio Programming Words

fRF (MHz)	(fRF x 4/5) / 20MHz (DIVIDER RATIO)	INTEGER-DIVIDER RATIO	FRACTIONAL-DIVIDER RATIO	
		Reg 0x09, Bit7:Bit0	Reg 0x0A, Bit13:Bit0(hex)	Reg 0x09, Bit13:Bit12
5180	207.2	1100 1111	0CCC	11
5200	208.0	1101 0000	0000	00
5220	208.8	1101 0000	3333	00
5240	209.6	1101 0001	2666	01
5260	210.4	1101 0010	1999	10
5280	211.2	1101 0011	0CCC	11
5300	212.0	1101 0100	0000	00
5320	212.8	1101 0100	3333	00
5500	220.0	1101 1100	0000	00
5520	220.8	1101 1100	3333	00
5540	221.6	1101 1101	2666	01
5560	222.4	1101 1110	1999	10
5580	223.2	1101 1111	0CCC	11
5600	224.0	1110 0000	0000	00
5620	224.8	1110 0000	3333	00
5640	225.6	1110 0001	2666	01
5660	226.4	1110 0010	1999	10
5680	227.2	1110 0011	0CCC	11
5700	228.0	1110 0100	0000	00
5745	229.8	1110 0101	3333	00
5765	230.6	1110 0110	2666	01
5785	231.4	1110 0111	1999	10
5805	232.2	1110 1000	0CCC	11