DESIGN SPECIFICATION

FOR

SMT318-SX55

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APPROVAL PAGE

Name	Signature	Date

AUTHOR/S

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DOCUMENT HISTORY

Date	Initials	Revision	Description of change
21-Nov-06	AV	0.1	Initial Issue
12-Feb-07	BV	0.2	Cleanup sections, for public release

TABLE OF CONTENTS

1 SCOPE

This document describes the design of the SMT318-SX55 module. It is intended as a guide to the schematic designer, the layout engineer, the firmware developer, and the manufacturing test developer. All aspects of the system are described, in sufficient detail, so as to allow engineering trade-offs to be made during the course of the module's production.

1.1 INTRODUCTION

The SMT318-SX55 is a single width TIM module. It provides the following:

- 2 Xilinx XC4VSX55-12 FPGAs
- 6 external SHBs
- 4 Inter-FPGA SHBs
- 4 Comports
- Global Bus interface
- JTAG interface

1.2 PURPOSE

The SMT318-SX55 provides effective communication links between interfaces.

The module has the following functions:

- Interface to Sundance High-Speed Bus at up to 200MHz (16- and 32-bit).
- Allow FPGA reprogramming via JTAG, Comport and stand-alone FLASH.
- Support partial-reprogramming of the FPGA.
- Support access to FLASH memory via JTAG and Comport.

2 APPLICABLE DOCUMENTS AND REFERENCES

2.1 APPLICABLE DOCUMENTS

2.1.1 External Documents

TI TIM specification & user's guide.

Xilinx Virtex 4 FPGA XC4VFX60.

Xilinx Virtex 4 PCB Designers Guide (ug072)

Xilinx Virtex 4 Memory Interfaces User Guide (ug079)

2.1.2 Internal documents

SUNDANCE SHB specification

2.1.3 Project Documents

N.A

2.2 REFERENCES

2.2.1 External documents

2.2.2 Internal documents

SUNDANCE SMT318-SX55 User Guide

2.2.3 Project documents

N.A

2.3 PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

3 ACRONYMS, ABBREVIATIONS AND DEFINITIONS

3.1 ACRONYMS AND ABBREVIATIONS

DMA	Direct Memory Access
JTAG	Joint Test Action Group (IEEE 1149.1 test access port)
FIFO	First-In First-Out
FPGA	Field Programmable Gate Array
TCXO	Temperature Compensated Crystal Oscillator
PCB	Printed Circuit Board
CPLD	Complex Programmable Logic Device
SHB	Sundance High Speed Bus
TIM	Texas Instruments Module
GPIO	General Purpose I/O
LED	Light Emitting Diode

3.2 DEFINITIONS

TIM carrier	A circuit board which contains TIM site(s). Typically these also contain an interface to a host (PCI, VME), or various interfaces for standalone operation.
MMCX	Trade name for a micro-mini RF connector interface.

4 DESIGN

4.1 GENERAL DESCRIPTION

The SMT318-SX55 module has two Xilinx XC4VSX55 FPGA to provide high-speed interfaces between the devices fitted to the module.

4.2 BLOCK DIAGRAM

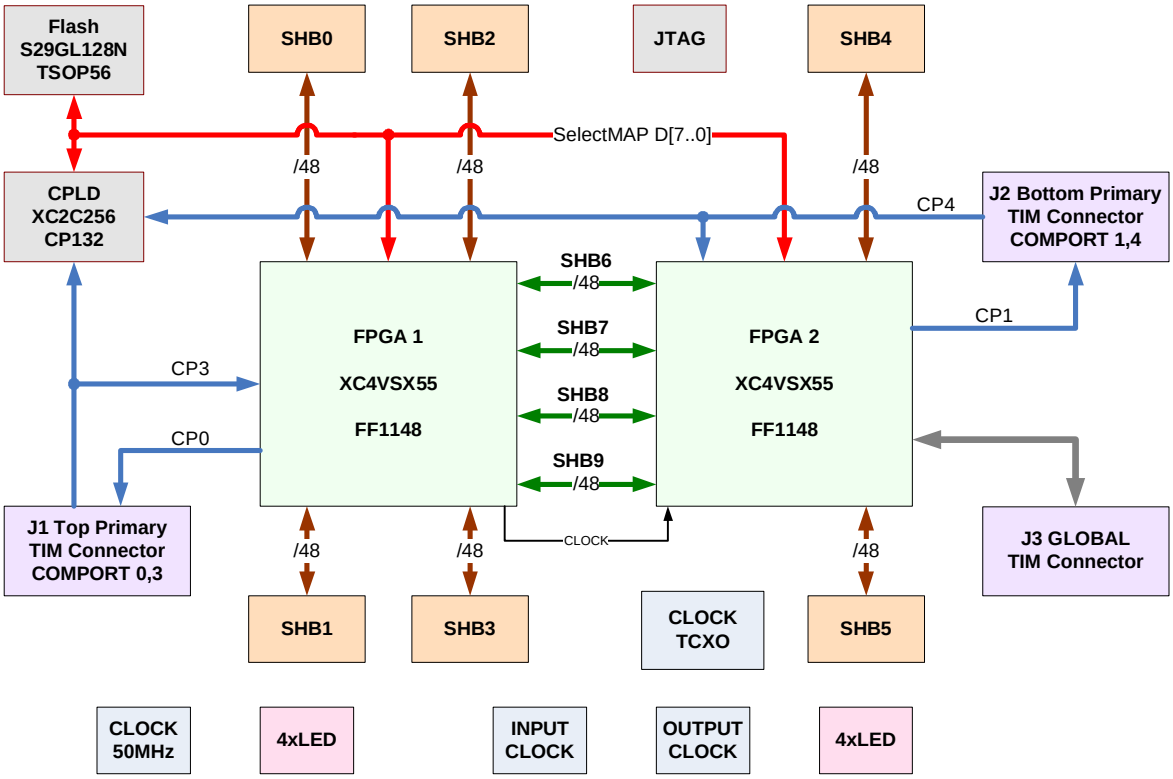

Figure 1 – Block Diagram of SMT318-SX55 module

4.3 CHARACERTISTICS

The SMT318-SX55 module shall conform to the following characteristics:

- Provide 6 SHB connectors with full support for 16/32-bit operation and user defined pins.
    - Two of these shall be PCB routed for LVDS signalling levels
- Provide 4 TIM COMPORT
    - COMPORT 3 shall configure FPGA1 according to Sundance Specification.
    - COMPORT 4 shall configure FPGA2 according to Sundance Specification.
- Enable FPGA to be configured by JTAG, FLASH or COMPORT
- Provide a high-stability clock source oscillator
- Provide conduction cooling via PCB design and thermal interface on the underside of the module.

4.4 POWER SUPPLY

On board power supply provides all necessary voltages for the module.

Power		V	A
VCCINT_1	Internal CORE supply voltage for FPGA 1	1.2	10
VCCINT_2	Internal CORE supply voltage for FPGA 2	1.2	10
VCCAUX	Auxiliary supply voltage for both FPGAs	2.5	3.0
VCCO_EXT	Output drivers supply voltage for external SHBs	3.3	
VCCO_INT	Output drivers supply voltage for internal SHBs	1.5, 1.8, 2.5	1.5 x 2
VBATT	Key memory battery backup supply	0.5 to 4.05	-
VREF	Input reference voltage	0.3 to 3.75	-

VCCINT_1 and VCCINT_2 are controlled by two non-isolated low-voltage input synchronous buck regulators TPS40009. These regulators drive an N-channel MOSFET for the primary buck switch, and an N-channel MOSFET for the synchronous rectifier switch, thereby achieving very high-efficiency power conversion. With using appropriate MOSFETs drivers a 20-A converter can be achieved. In addition soft-start and overcurrent fault shutdown times are set by charging and discharging a capacitor connected to the pin SS/SD of these regulators. This allows for a smooth start-up with no overshoot of the output voltage. VCCAUX voltage is provided with Micrel MIC37300 a

3.0A low-dropout linear voltage regulator with high-current output and a minimum number of external components. It offers high precision, ultra low-dropout (500mV over temperature), and low ground current. VCCO_EXT is used for powering external SHBs and provides from 3.3V Mounting holes. VCCO_INT is used for the power supply of Inter-FPGAs SHBs links. Input voltage for internal SHBs is provided with 1.5A low noise LDO regulators LT1963A series and may be chosen as 1.5V, 1.8V, 2.5V or 3.3V. For each of the FPGAs are used its own LDO regulator.

Total amount of the internal SHB links are 48 * 4 = 192. With 1.5A output current for each regulator it allows to have 7mA for every pin.

The module is provided with a 2 pin connector for VBATT.

The SMT318-SX55 conforms to the TIM standard for single width modules. The TIM connectors supply +5V to the module. The +3.3V supply is provided by the two diagonally opposite mounting holes. This +3.3V is present on all Sundance TIM carrier boards. From these two power rails, filtered +3.3V as well as the remaining voltages are provided to the components on the module.

A green LED is placed on the board to report the state of the power supplies.

4.5 CLOCKS

The module has two internal oscillators: 50MHz and TCXO.

- 50MHz oscillator is used during the FPGAs configuration and is connected to the CPLD.
- TCXO oscillator is connected to both FPGAs and is used for reference clock.

The SMT318-SX55 module has two MMCX 50ohm connectors. One connector is an input for an external oscillator, and the second connector is a clock output. Also it is possible to configure a differential clock (input or output), by using both connectors. The TCXO used for user logic should have frequency stability of better than 10ppm. The systems which are using the SMT318-SX55 are likely to fluctuate in temperature.

Some possible choices might be: http://www.euroquartz.co.uk/tcxo.htm (EM57T)

4.6 CONFIGURATION AND INITIALIZATION

On power-up sequence, the configuration bit-stream is being loaded into the FPGAs using SelectMAP Mode, as it is shown on figure 2:

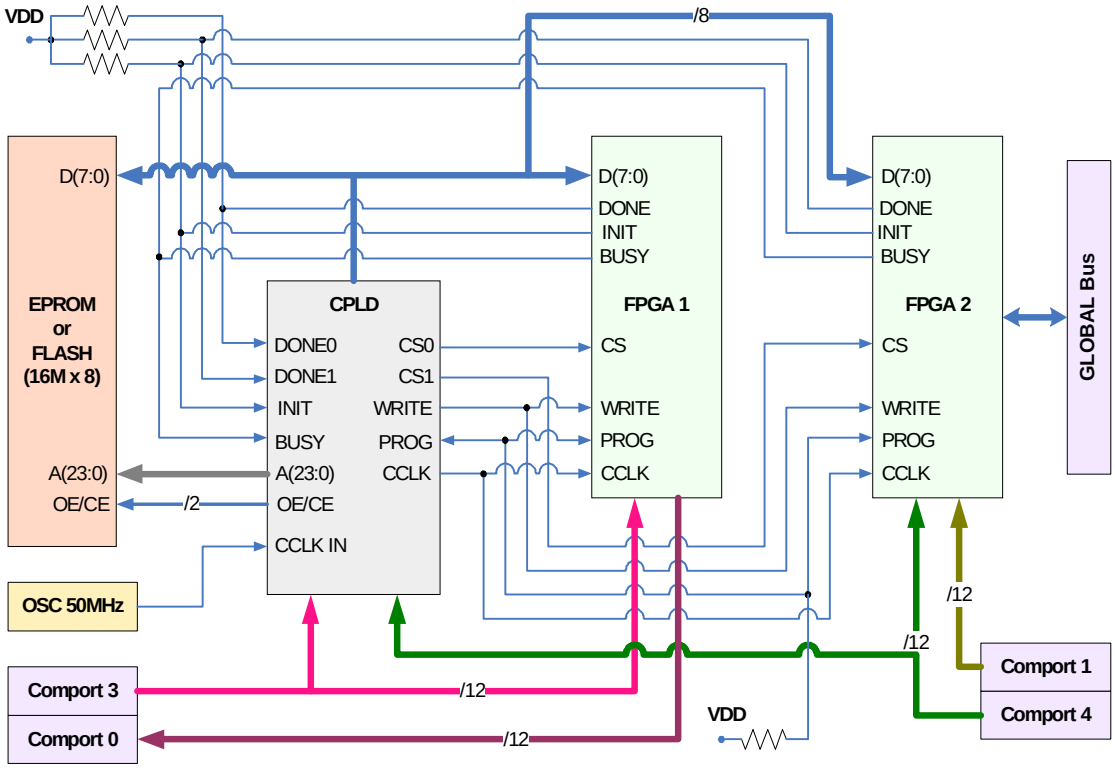

Figure 2 - Configuration Block Diagram

SelectMAP configuration does not support a standard daisy-chain configuration like the bit-serial modes do. However, in an application, where there are multiple FPGAs to be configured, the PromMAP design may be altered to accommodate a parallel daisy-chain so that multiple interface chips are not necessary.

For each FPGA the DONE and CS signals must be connected to the interface design separately. The BUSY and WRITE signals can be a common line between the FPGAs. When the first FPGA raises its DONE signal the interface should disable that FPGA's CS input and enable the next one in the chain, and so on until all DONEs are high.

Using this method will cause each FPGA to become active after its DONE transitions High. Therefore, it is important that none of the configuration pins used for SelectMAP configuration to be used as IOs in the FPGA designs. Otherwise contention could result when one or more FPGAs are configured and active, but others are not yet configured.

To configure the Virtex FPGAs from a parallel PROM, a small interface is needed to generate the PROM addresses and load the data into the FPGAs. This is provided by the CPLD.

4.7 DIGITAL DATA I/O INTERFACE

4.7.1 Sundance High Speed Bus Interface

The SHB interface consists of 60 I/O connections between the FPGA and the SHB connector. The Sundance SHB interface definition allows for two independent 16-bit SDB links or a single 32-bit link to be implemented over one SHB connector.

The interface will be implemented such that it will support a minimum of 100MHz operation, allowing interfacing to other Sundance modules. A maximum user frequency of 180MHz will be possible when interfacing to other Sundance modules, or Sundance modules utilizing Virtex-4 devices.

In addition, external devices and protocols can be implemented by using a custom interface block in the FPGA. Note that certain signals of the SHB connector have special treatment as follows from Table 1:

Signal	P10 Pin	Resistor (ohms)
SHB_HW0_ACK	24	4.7K pulldn
SHB_HW0_CLK	1	150 pulldn
SHB_HW0_REQ	23	4.7K pulldn
SHB_HW0_WEN	22	4.7K pullup
SHB_HW1_ACK	60	4.7K pulldn
SHB_HW1_CLK	37	150 pulldn
SHB_HW1_REQ	59	4.7K pulldn
SHB_HW1_WEN	58	4.7K pullup

Table 1 - SHB Pullup/Pulldown Values (Referenced to +3.3V)

4x SHB interfaces are implemented for FPGA1, with two of them supporting LVDS signalling by differential pair routing on the PCB and flexible I/O termination voltage on the FPGA. 2x SHB interfaces are implemented for FPGA2. 4x Inter-FPGA SHB interfaces provide high-speed communication links between the FPGAs.

External SHB interfaces are powered using VCCO = 3.3V. (2.5V for LVDS option).

Internal SHB interfaces are powered using VCCO = 1.8V.

4.7.2 CPLD

Xilinx CoolRunnerII CPLD XC2C256-CP132 is used to configure the FPGAs on power-up. The CPLD is in the JTAG chain along with the FPGA allowing for field upgrade of the firmware.

4.7.3 FLASH

A single SG29GL128N FLASH is used to hold the configuration bit-streams for both FPGAs. The flash has the capacity to store two configurations at a time. The configuration loaded into the FPGAs at power up is determined by the setting of a DIP switch.

4.7.4 GPIO

The module has 4x GPIO on a 6-pin 1.25mm header to enable digital control signals.

4.8 MEMORY

There is no external memory on the board.

4.9 TIM CONNECTORS

TIM connectors provide 4 communication links (Comports 0, 1, 3, 4) to the FPGA. Comports 0 and 3 go to FPGA1. Comports 1 and 4 go to FPGA2. Comport 1 and Comport 4 are routed to the CPLD to enable uploading the flash and respectively loading the bit stream to the FPGA. The Comport interface is available in Sundance SMT6500 Support Package. The FPGA I/O banks hosting the Comport signals are powered using VCCO = 3.3V. The TIM connectors also provide Power/Ground, reset and various control signals.

References and specifications for these connectors are available on Sundance Web site

4.10 GLOBAL BUS INTERFACE

Global Bus is routed to the FPGA2. Newer Sundance carrier boards employ a design in which 16-bit or 32-bit SHB interfaces are routed to the carrier board FPGA (such as the SMT148-FX, SMT150Q and SMT329) for connections to the I/O resources on those carriers (Gigabit Ethernet/USB2.0, PCI-Express and VME64, respectively).

4.11 DIP SWITCHES

A four pole DIP-switch is connected to the CPLD I/O to provide configuration selection.

4.12 TEMPERATURE SENSOR

The module has temperature sensor LM83 from National Semiconductor that monitors the temperatures of both FPGAs. The digital temperature sensor accurately senses its own

temperature as well as the temperature of the Virtex-4 with a 1 °C resolution. Coupled with the CPLD it flashes a red LED above a high threshold and de-configures the FPGAs. The threshold temperature is fixed by the CPLD at 85 degrees and the FPGA power is shutdown at 125 degrees (Maximum Junction temperature).

4.13 FAN

The module has a fan connector. The fan coupled with a heat sink can be mounted on the FPGAs to provide heat dissipation. The fan signal is controlled by the CPLD and can be switched on/off depending on the current temperature of the FPGAs.

4.14 CONDUCTION COOLING

The module has a pair of 2oz copper core thermal layers for heat dissipation. The bottom of the module has two thermal interface layers which allow a connection to heat pipes or other heat transfer mediums. Thermal vias throughout the board connect these thermal layers. The layers are electrically connected to the ground plane(s) of the PCB.

5 PERFORMANCE

5.1 CONFIGURATION

5.2 SHB

5.3 ANALOG I/O

6 PHYSICAL CHARACTERISTICS

6.1 MECHANICAL

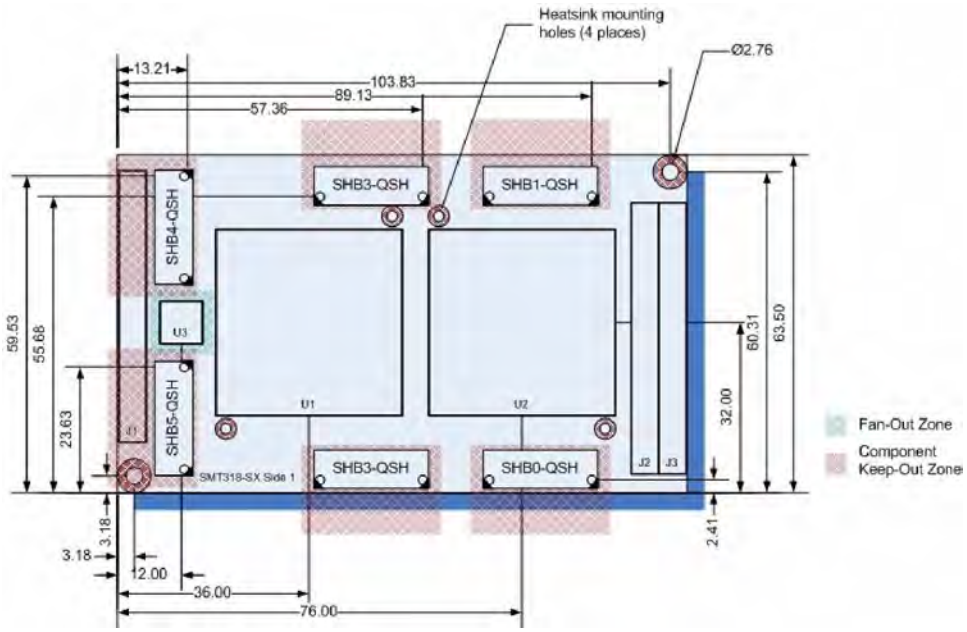

Figure 3 - Top Component Placement

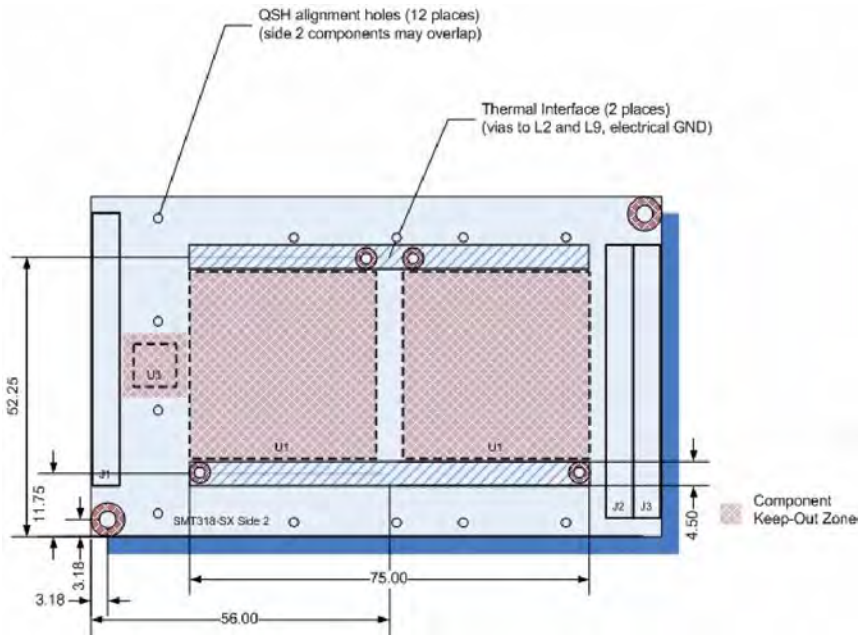

Figure 4 - Bottom Component Placement

7 FOOTPRINT

7.1 TOP VIEW

7.2 BOTTOM VIEW

8 PINOUT

8.1 FPGA

8.2 GPIO

8.3 LED

8.4 SHB

8.5 TIM-40

9 QUALIFICATION REQUIREMENTS

9.1 QUALIFICATION TESTS

9.1.1 Meet Sundance Standard Specifications

- Meet the TIM-40 standard specifications
- Meet SHB specifications
- Allow re-configuration of FPGA(s) via COMPORT protocol

9.1.2 Meet External Specifications

- Meet LVDS specifications

9.1.3 Meet Quality Specifications

- TXCO to provide output at 10ppm across all temperature ranges supported

9.1.4 Speed Qualification

- SHB to operate at 200MHz
- LVDS to operate at 1GHz
- COMPORT to operate at 20MHz

9.1.5 Integration Qualification

- Operate on SMT148-LT, SMT148-FX, SMT310(Q) and SMT300(Q) carriers.
- Operate with SMT361Q, SMT364, SMT368, and SMT374 modules.

10 SAFETY

This module presents no hazard to the user.

11 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

12 ORDERING INFORMATION

Speed grade	-10	-11	-12
	SMT318-SX55	SMT318-SX55-11	SMT318-SX55-12

SMT318-<fpga>-<speed>-<option>

where:

<fpga>= SX55

<speed>= 10, 11, or 12

<option>= none(TXCO=200MHz)