HARDWARE SPECIFICATION
FOR

SMT348

APPROVAL PAGE

Name	Signature	Date

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DOCUMENT HISTORY

Date	Initials	Revision	Description of change
20/10/05	GKP	1.00	First release based on the SMT368.
2/11/05	GKP	1.01	Changed FPGA config mode to slave serial.
8/11/05	GKP	1.02	Changed back to SelectMAP mode. Updated component placements with new QDR2 positions. Updated FPGA bank table.
9/11/05	GKP	1.03	Added comment about SLB and LX device.
1/2/06	GKP	1.04	Added QDR part number.
2/09/06	E.P	1.05	Update of FPGA configuration and DIP switch

TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

1. SCOPE

This document specifies the requirements for The SMT348 FPGA TIM module

1.1. INTRODUCTION

The SMT348 is a TIM module in the range of Sundance's Virtex 4 FPGA modules.

It provides a communications platform between an XC4VSX55 or XC4VLX160 FPGA and

- 4 banks of QDR2 SRAM.

- 2 32-bit SHBs.

- TIM Global Bus.

- LVDS connections for high speed parallel connections

- LVTTL connections and connectors.

This variety of connectors and interfaces provides a wide range of development options for designers to explore the capabilities of the comprehensive Sundance TIM modules family.

1.2. PURPOSE

The SMT348 must:

- Provide high-speed interface to Sundance ADC/DAC modules

- Provide high-speed interface to Sundance DSP modules.

- In any configuration on Sundance carriers, i.e on its own, on a stand-alone carrier or in a Host as part of a system.

1.3. APPLICABILITY

Interface to other FPGA, DSP, ADC/DAC modules and in stand alone systems.

Document No.	Revision	Date	
Smt348 design spec.doc	1.04	02/09/06	Page 7 of 24

2. APPLICABLE DOCUMENTS AND REFERENCES

2.1. APPLICABLE DOCUMENTS

2.1.1. External Documents

TI TIM specification & user's guide.

Samtec QSH Catalogue page

Virtex 4 Datasheet

2.1.2. Internal documents

SUNDANCE SDB specification.

SUNDANCE SHB specification

SUNDANCE SLB specification

2.1.3. Project Documents

Smt348 QCF14.mpp   Project Planning Document.

2.2. REFERENCES

2.2.1. External documents

N.A

2.2.2. Internal documents

N.A

2.2.3. Project documents

N.A

2.3. PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

3. ACRONYMS, ABBREVIATIONS AND DEFINITIONS

3.1. ACRONYMS AND ABBREVIATIONS

TIM   Texas Instruments Module

3.2. DEFINITIONS

TIM carrier   A circuit board which contains TIM site(s). Typically these also contain an interface to a host (PCI, VME), or various interfaces for standalone operation.

4. REQUIREMENTS

4.1. PRIME ITEM DEFINITION

This module conforms to the TIM standard (**T**exas **I**nstrument **M**odule, See TI TIM specification & user's guide) for single width modules.

It sits on a carrier board.

The carrier board provides power (5V, 3.3V, +/-12V), ground, communication links (Comport links) between all the modules fitted and a pathway to the host, for a non stand-alone system.

The SMT348 requires a 3.3V power supply (as present on all Sundance TIM carrier boards), which must be provided by the two diagonally opposite mounting holes.

4.1.1. Prime Item Diagrams

Figure 1 shows a simplified version of the SMT348 module
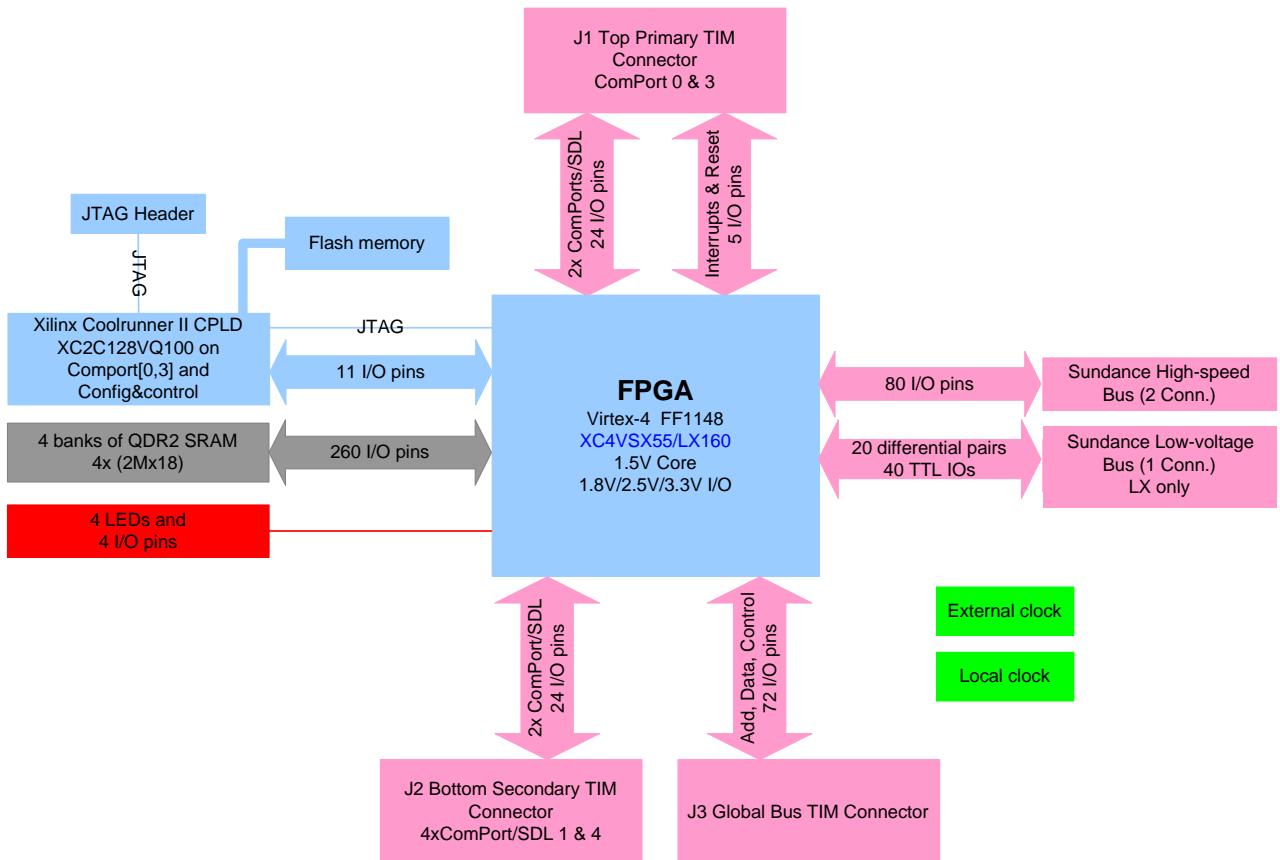
Figure 1: Block Diagram

4.1.2. Interface Definition

For the TIM to carrier board or external world interfacing, see in Sundance Help file (that you can download from this link)

4.1.3. Major Component List

- Block1: Xilinx Virtex 4 XC4VSX55/LX160 and configuration scheme.

- Block2: QDR2 SRAM memory.

- Block3: IO connectors for general purpose or dedicated interfaces.

- Block4: 100MHz local clock, and external clock input.

- Block5: LEDs for development and in-use monitoring and general purpose use.

4.1.4. Prime Item Characteristics

4.1.4.1. FPGA

Xilinx Virtex 4 XC4VSX55FF1148 or XC4VLX160FF1148 FPGA.

This device is packaged in a 1148-pin BGA package.

4.1.4.2. CPLD

Xilinx Coolrunner II device XC2C256-6CP132C This device is packaged in a 132-ball BGA type package with a -6 speed grade.

It can be used to configure the FGPA via Comport 3, or from a configuration stored in flash memory.

The flash memory is programmed using the CPLD and data via the ComPort3 and Comport0.

4.1.4.3. FLASH MEMORY

S29GL256N11TFI01 is a 256Mbit flash from Spansion

It can be used to configure the FPGA at power up.

Slave SelectMAP FPGA configuration interface (up to 50 MHz)

Design revision technology enables storing and accessing multiple design revisions for configuration.

All the flash functionalities are available.

4.1.4.4. JTAG Header

The JTAG header is compatible with Xilinx Parallel-IV cable signals.

It supports code download (for the FPGA), FPGA configuration, Hardware and Software Debugging tools for the Virtex-4.

This cable connects the parallel port of an engineer's Workstation/PC to the JTAG chain of the SMT348 Module.

All the devices from block1 are chained and accessible via this JTAG header.

4.1.4.5. FPGA Configuration schemes

Different schemes are available to provide maximum flexibility in systems where the SMT348 is involved:

The FPGA configuration bitstream source is

- On Comport 3:

The CPLD is connected to 2 Comport links of the SMT348 TIM connector. A switch is used to select the configuration Comport 3 that will be used to receive the bitstream.

The CPLD allows for FPGA configuration in slave SelectMAP mode.

- Using the on-board Flash memory.

The CPLD monitors the configuration data between the Flash and the FPGA. The FPGA configuration is operated in Master SelectMap mode.

A switch is used to select the Flash as the source for the configuration bitstream.

- Using the on-board JTAG header and Xilinx JTAG programming tools.

The JTAG header is a Parallel-IV Header.

4.1.4.6.　QDR2 SRAM

Up to 4 Mbytes of QDR2 SRAM per bank.

The memory is available as 4 independent banks.

The QDR2 memory runs at 250MHz.

Each bank is fully independent with separate address, control and data busses.

The devices used are Samsung K7R321884M. Alternative part numbers, fully compatible can be fitted depending on availability at time of order.

4.1.4.7.   Sundance High speed Bus

2 x 60 pin connectors provide 80 IO connections between the FPGA and the outside word.

They allow interfacing to other Sundance modules providing that you implement an SHB interface in the FPGA. (See 2.1.2.)

The SHB interface is available in Sundance SMT6500 support package. Either two 16-bit, or 1 32-bit interface can be implemented per connector.

They allow interfacing to the outside world by implementing your own interface in the FPGA.

The FPGA IO banks hosting the SHB signals are powered using Vcco = 3.3V.

4.1.4.8.   Sundance Low voltage Bus

This is an LVDS bus comprising data (2 x 16 bit buses, I & Q), clock, and control signals. This bus is present on the LX160 version of the module only.

They allow interfacing to Sundance mezzanine modules providing that you implement an SLB interface in the FPGA. (See 2.1.2.)

They allow interfacing to the outside world by implementing your own LVDS interface in the FPGA.

All LVDS data pins (both I and Q) are connected to a 2.5/3.3V powered FPGA banks (link selectable). The LVDS Clock signals are also in these banks.

All LVTTL signals are connected to a 3.3V powered FPGA bank.

4.1.4.9.   TIM Connectors

TIM connectors provide 4 communication links (Comports) and a Global Bus to the FPGA.

They allow interfacing to Sundance TIM modules or to a Host PC providing that you implement Comport Interface inside the FPGA. (See 2.1.2.)

The Comport interface is available in Sundance SMT6500 support package.

The FPGA io banks hosting the Comport signals are powered using Vcco = 3.3v.

The TIM connectors also provide power/ground, reset and various control signals.

References and specifications for these connectors are available on Sundance Web site

- One four-position DIP switch is connected to the FPGA I/Os for general purpose use in an FPGA design.

- One four-position DIP switch is connected to the CPLD to provide control over the selection of the configuration bitstream source and a special reset feature called "TIM Confign".

JPC 4	TIM Config
ON	ENABLED
OFF	DISABLED

Table 1: DIP switch for special reset feature

JPC 3,2, 1	JPC3	JPC2	JPC1
C3P	OFF	OFF	OFF
Flash	OFF	OFF	ON

Table 2: DIP switch for the selection of the configuration bitstream source

JPC 3,2, 1	JPC3	JPC2	JPC1
Flash accesses	ON	OFF	OFF

Table 3: DIP switch for the selection of the Flash erase & program operations.

The Flash erase & program operations are operated by the CPLD.

Commands are provided via Comport3 and status information from the Flash is given over Comport0.

4.1.4.11. Clocking scheme

The SMT348 module contains a 100MHz LVTTL clock, A QDR2 clock (frequency:tbd) and a connector for an external LVTTL clock input/output.

4.1.4.12. LEDs

- 4 Red LEDs connect to the FPGA and are available to the User.

- 1 Green LED connects to the DONE pin of the FPGA to show FPGA is configured. The LED is turned on when the FPGA is configured.

4.1.5. Performance

The FPGA features like speed grade and density dictate most performances.

The performances achievable by the other components are given in the 4.1.4. Prime Item Characteristics chapter.

Document No.	Revision	Date	
Smt348 design spec.doc	**1.04**	**02/09/06**	Page 16 of 24

4.1.6. Physical Characteristics

4.1.6.1. Power budget

Table 4: Power budget.

Device	Quantity	Voltage(V)	Current(mA)	Power(W)	Source
Samsung QDR2	4	1.8			
100 MHz Clock oscillator	1	3.3	10	0.033	**Jauch VX3 Quartz crystal oscillators datasheet**
LEDs	5	3.3	10	0.165	
DIP Switch	1	2.5	2.1	0.005	Four 4.7 Kohm pullup
XC4VSX55/LX160	1	Must be calculated based on design			
Coolrunner II CPLD (See details)	1	1.8	17mA	0.031	**CPLD power calculator**

Details:

Coolrunner II CPLD power requirement based on design:

During FPGA configuration only, the Coolrunner CPLD power consumption is at its maximum:

- Macrocells used: 202

- Macrocells used as outputs or bidirectional: 26

- Fmax:50MHz

- The average toggle rate of all flip-flops:40%

- Number of product terms:448

5. FOOTPRINT

5.1. TOP VIEW
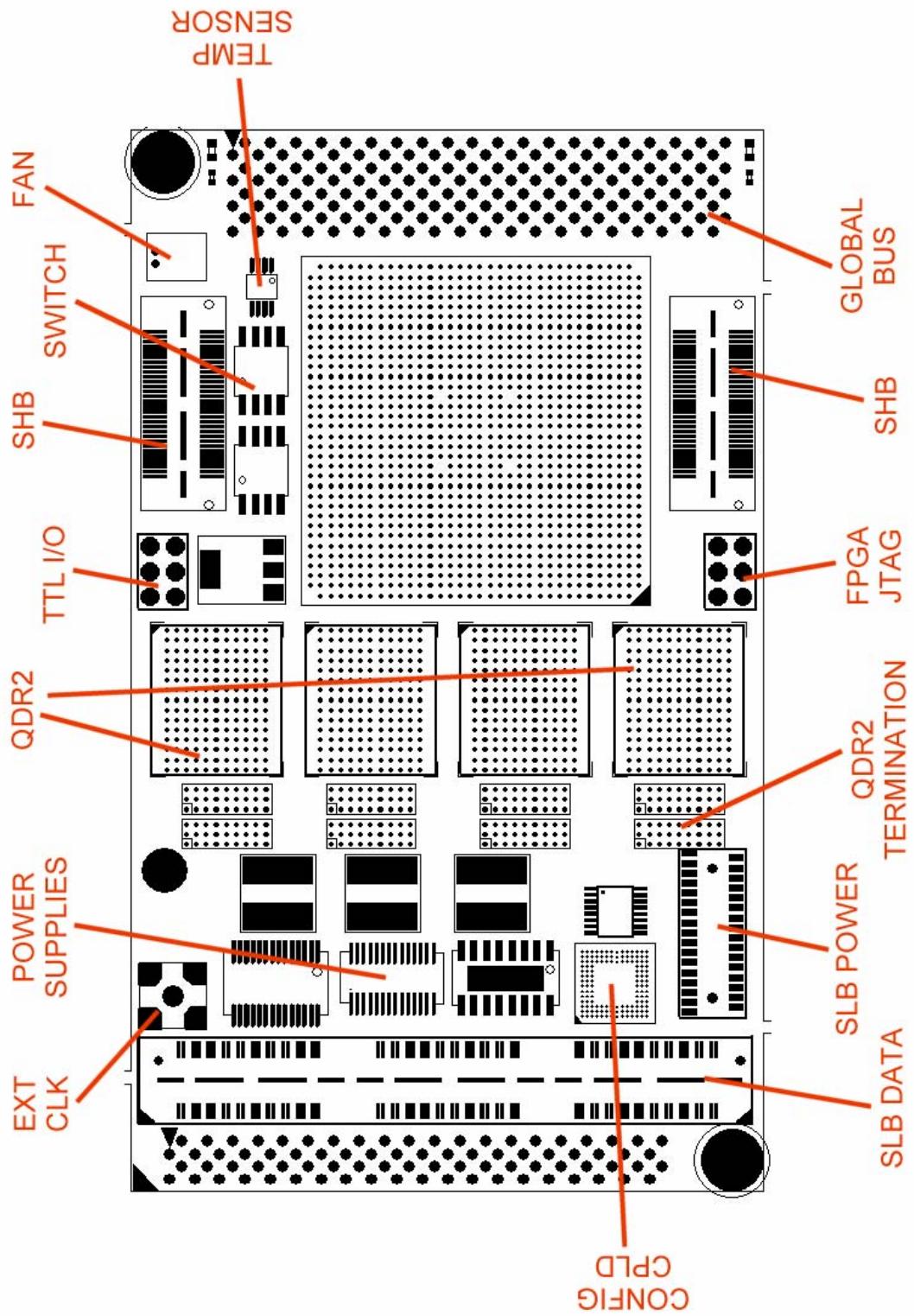
Figure 2: Top View
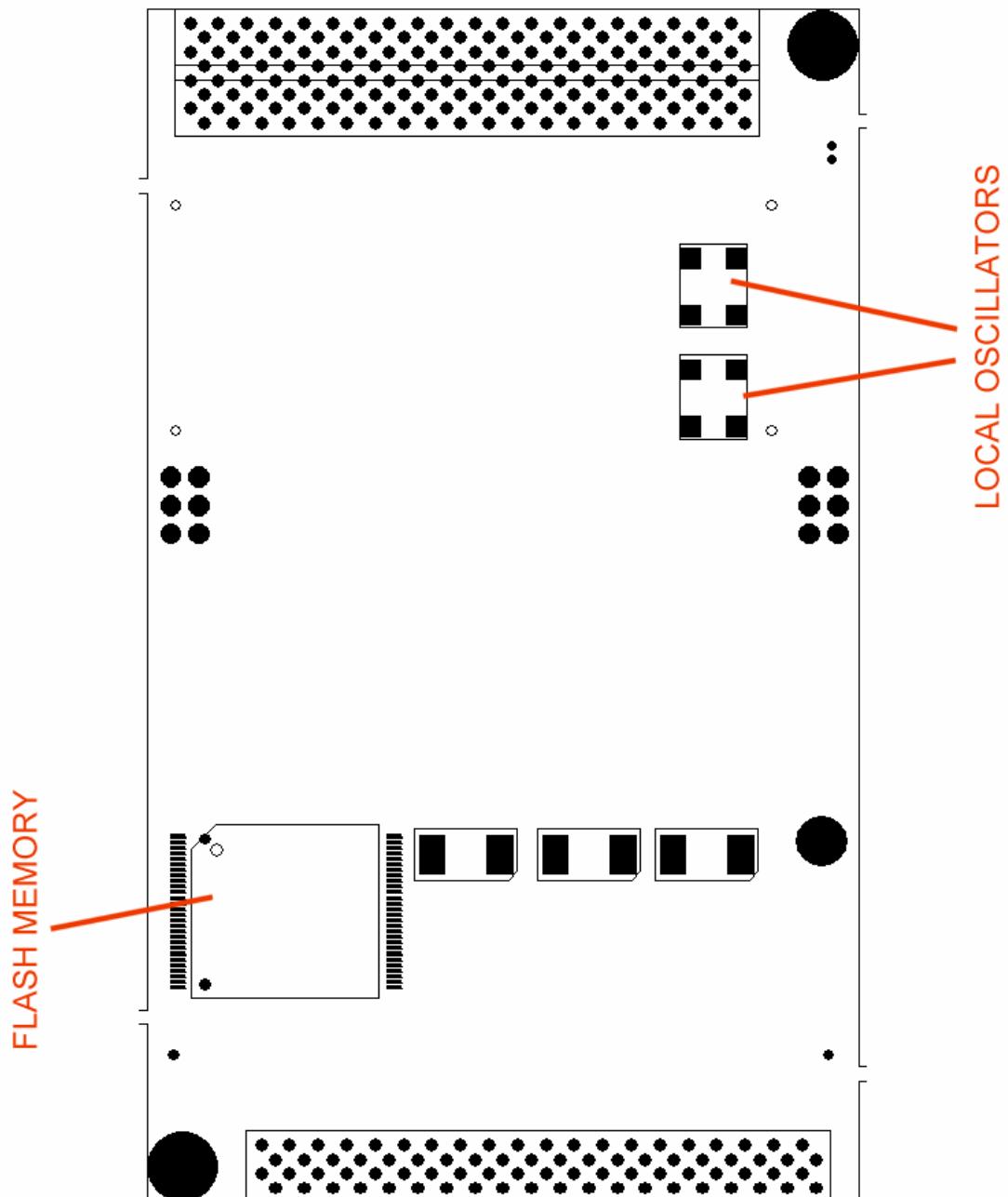
5.2. BOTTOM VIEW

Figure 3: Bottom View

6. PINOUT

6.1. FPGA PIN ALLOCATION BY BANK

Bank	I/O	Vr*	QDR2	SHB	CP	SLB	GB	Other	Total
1	48	0							
2	48	0						8xConfig	8
3	16	0	Clocks & DLL control						2
4	16	0						Clocks & Reset & Switches	13
5	64	4	Bank C Data + Control						64
6	64	4	Bank B Data + Control						64
7	64	6				SLB LVTTL	13 Control	PXI, TTL, INTs, LEDs, Misc.	64
8	64	6					32 Data & 31 Address & 1 Control		64
9	64	4	Bank D Data & Control						64
10	64	4	Bank A Data & Control						64
11	64	6		1xSHB	2xCP				64
12	64	6		1xSHB	2xCP				64
13	64	6				16 Diff Data & 4 Diff Clocks			46
14	64	6				16 Diff Data & 4 Diff Clocks			46

Vr* = Vrp + Vrn + Vref

6.2. SHB

SUNDANCE SHB specification

6.3. SLB

SUNDANCE SLB specification

7. QUALIFICATION REQUIREMENTS

7.1. QUALIFICATION TESTS

7.1.1. Meet Sundance standard specifications

- Meet the TIM standard specifications

- Meet the SLB specifications (LVDS standard).

- Meet the SHB specifications.

7.1.2. Speed qualification tests

- QDR2 memory accesses at 250MHz.

7.1.3. Integration qualification tests

- Must work on ALL Sundance platforms as a root TIM module or as part of a network of TIMs on carriers.

- Must be able to work stand-alone.