# SMT361Q

User Manual


Certificate Number FM 55022

## Revision History

| Date | Comments | Engineer | Version |
|---|---|---|---|
| 22/04/04 | First rev, based on 365 | J.V. | 1.0.0 |
| 01/06/04 | FPGA clock rate compared with DSP clock rate added | J.V. | 1.0.1 |
| 03/03/06 | Minor changes, and ComPorts architecture | SM | 1.0.2 |
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## Contacting Sundance

You can contact Sundance for additional information by login onto the Sundance support forum.

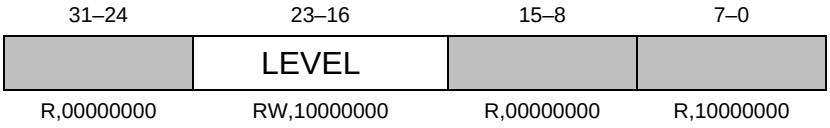
# Notational Conventions

### *C60*

The terms C60, C64xx and TMS320C64xx will be used interchangeably throughout this document.

### *Register Descriptions*

The format of registers is described using diagrams of the following form:




The digits at the top of the diagram indicate bit positions within the register and the central section names bits or bit fields. The bottom row describes what may be done to the field and its value after reset. Shaded fields are reserved and should only ever be written with zeroes.

| | |
|---|---|
| R | Readable by the CPU |
| W | Writeable by the CPU |
| RW | Readable and writeable by the CPU |

Binary digits indicate the value of the field after reset.

## Outline Description

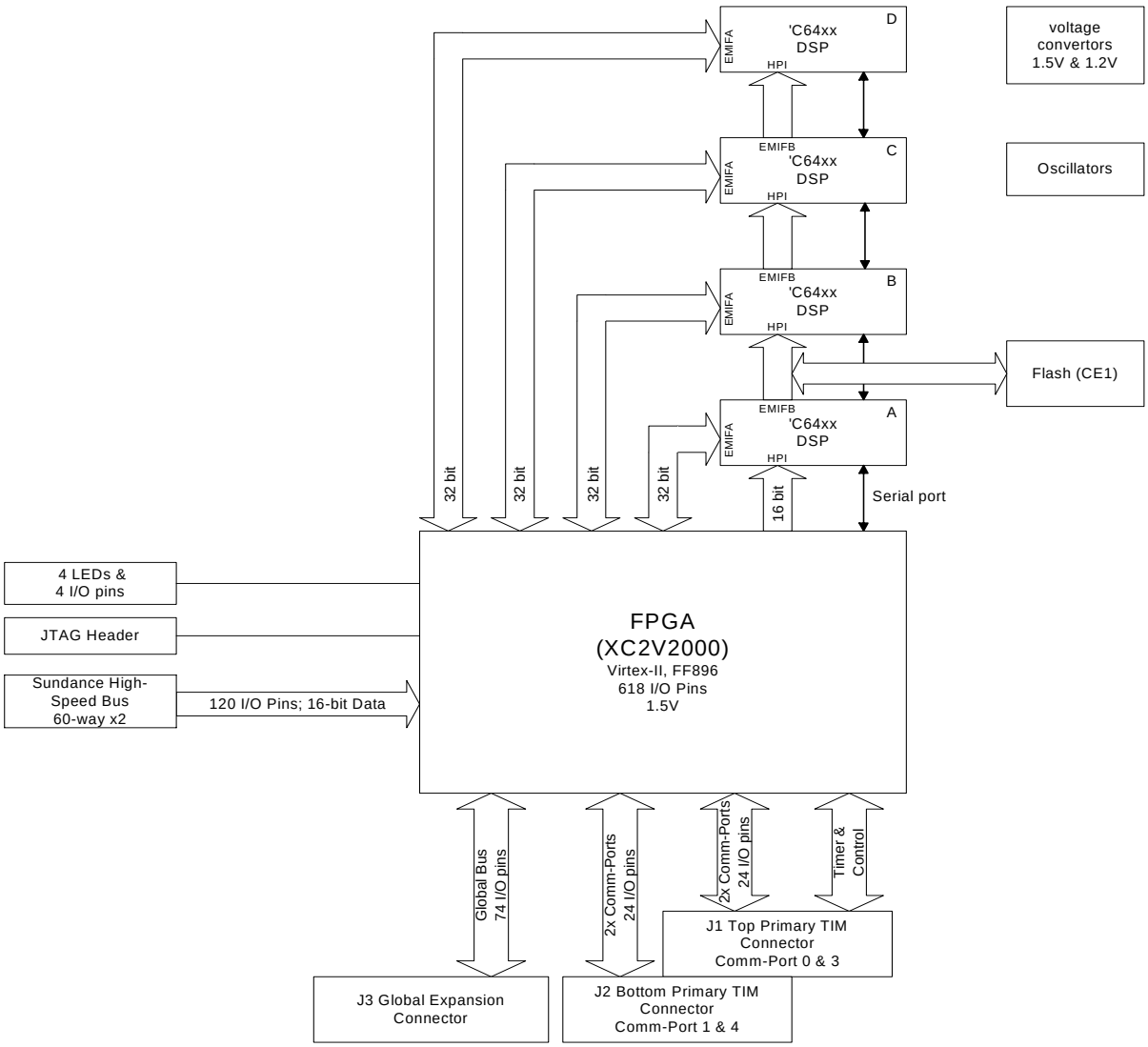
The SMT361Q is Sundance's 3rd generation of Texas Instruments 'C6x DSP TIM (Texas Instruments Module). This module uses 4 TMS320C6416 DSPs which have clock speeds of up to 720MHz.

The module also includes a Xilinx Virtex-II (XC2V2000FF896) FPGA which is configured to provide 'C4x style ComPorts, a TIM compatible enhanced global bus, two Sundance High-Speed Busses (SHBs) and other control functions.

The SMT361Q is, from the user's perspective, a multi-DSP version of the SMT361A Module and a system can be designed with a mixture of SMT361s and SMT361Qs on the same Module Carrier.

The SMT361Q is supported by the TI Code Composer Studio and 3L Diamond RTOS to enable full MultiDSP systems with minimum efforts by the programmers.

# Block Diagram




# Architecture Description

The SMT361Q TIM consists of a Texas Instruments TMS320C6416 running at 600MHz.

A Field Programmable Gate Array (FPGA) is used to manage Global bus accesses and implement four ComPorts and two Sundance High Speed Busses. This is a Xilinx Virtex-II device.

## TMS320C6416

The processor will run with zero wait states from internal SRAM.

The following table shows the main DSP characteristics.

| Feature | C6416 |
|---|---|
| DMA / McBSP / Timer | 64/3/3 |
| On-chip memory | 1056k bytes |
| Speed | 1GHz |
| Others | UTOPIA<br>Viterbi and Turbo decoders |

The SMT361Q implementation using this DSP provides interfaces using the EMIFs (External Memory Interfaces A & B), timers and JTAG.

The JTAG interface is provided to enable application debugging via a suitable JTAG controller and software. Typically, this will be a SMT310 and TI Code Composer Studio. This is an invaluable interface that enables the application programmer to quickly debug a 'chain' of processors in single or multi-processor situations.

Each DSP's EMIFA is used to connect to the Virtex-II FPGA.

The Flash ROM is connected via DSP_A, EMIFB as a 16-bit device.

### DSP resources and control

The DSP resources available to each DSP are the following:

| Ressource | DSP_A | DSP_B | DSP_C | DSP_D |
|---|---|---|---|---|
| External ComPort | 1 | 1 | 1 | 1 |
| Internal ComPort | 5 | 5 | 5 | 5 |
| External SHB | 2 | 0 | 0 | 0 |
| Global bus | 1 | 0 | 0 | 0 |
| Flash | 1 | 0 | 0 | 0 |

## Clock settings

An on-board crystal oscillator (X2) provides the clock used for the C60, which is then multiplied by 12 internally. (50MHz x 12 = 600MHz).

As the clock mode is set to "10" the EMIF clock is running at CPU clock/6 i.e. 100MHz.

## Boot Mode

The SMT361Q is configured to boot from flash after a reset

### *Flash Boot*

1. The DSP_A copies a bootstrap program from the first part of the flash memory into internal program RAM starting at address 0.
2. Execution starts at address 0.

The standard bootstrap supplied with the SMT361Q then performs the following operations:

1. All relevant C60 internal registers are set to default values;
2. The FPGA is configured from data held in flash memory and sets up the communication ports, the global bus and the Sundance High-speed Buses. This step must have been completed before data can be sent to the ComPorts from external sources such as the host or other TIMs;
3. The configuration for DSP_B is sent with HPI. DSP_B then passes it on the same way to DSP_C which pass it on the same way to DSP_D. All DSPs are configured and waiting to boot over their ComPorts (see after).
4. A C4x-style boot loader is executed. This will continually examine the ComPorts until data appears on one of them. The bootstrap will then load a program in boot format from that port; the loader will not read data arriving on other ports.
5. Finally, control is passed to the loaded program.

The delay between the release of the board reset and the FPGA configuration is around 1s for a SMT361Q.

A typical time to wait after releasing the board reset should be in excess of this delay, but no damage will result if any of I/Os are used before they are fully configured. In fact, the ComPorts will just produce a not ready signal when data is attempted to be transferred during this time, and then continue normally after the FPGA is configured.

### EMIF Control Registers

The C6416 has two external memory interfaces (EMIFs). One of these is 64 bits wide (EMIF_A), the other 16 bits (EMIF_B).

The C60 contains several registers that control the external memory interfaces (EMIFs). A full description of these registers can be found in the *C6000 Peripherals Reference Guide*.

The standard bootstrap will initialise these registers to use the following resources:

| Memory space (EMIFA) | Resource | Address range |
|---|---|---|
| | Internal program memory (1M) | 0x00000000 - 0x000FFFFF |
| CE3 | Virtex | 0xB0000000 - 0xB00FFFFF |

| Memory space (EMIFB) | Resource | Address range |
|---|---|---|
| CE0 | HPI of adjacent DSP | 0x60000000 - 0x600000FF |
| CE1 | 8MB Flash in 4 pages<br>Page is selected with GPIO9 and GPIO10 | 0x64000000 – 0x641FFFFF |
| CE2 | Any access asserts FPGA PROG line | 0x68000000 – 0x641FFFFF |
| CE3 | A write programs data bit D0 serially in the FPGA and make a CCLK edge. | 0x68000000 – 0x641FFFFF |

## *FLASH*

An 8MByte flash memory is provided with direct access by the DSP_A. This device contains boot code for the DSPs and the configuration data for the FPGA.

This is a 16-bit wide device.

The first few KBytes are used for DSP boot code.

The flash device can be re-programmed by the DSP at any time. There is a software protection mechanism to stop most errant applications from destroying the device's contents.

Note that the flash memory is connected as a 16-bit device, but during a C6x boot (internal function of the C6x) only the bottom 8 bits are used.

As the C60 only provides 20 address lines on its EMIFB, two GPIO lines (9 and 10) are used to access this device. So the device should be seen as divided in 4x 2MBytes pages.

### *FLASH Paging*

Selecting the visible flash memory page (4 pages of 2MBytes) involves setting up the GPIO registers bit 9 and 10. Make sure that the setup of the other GPIO is kept untouched as they are used for external interrupt and leds.

## Virtex-II FPGA

This device, a Xilinx XC2V2000, is responsible for the provision of the SHBs, ComPorts and the Global bus. On power-up, this device is un-configured (SRAM based FPGA technology). During the DSP boot process, the FPGA is configured for normal operation.

The FPGA operates at EMIF speed (100MHz).

The standard configuration for the primary FPGA uses approximately 4000 slices and 24 Block rams. The remainder can be used for additional functionality.

This FPGA provides for 4 external ComPorts.

Each DSP has 6 ComPorts. One of these is external, and the other 5 are for inter-DSP communications.

Note that the I/Os of the FPGA are not 5V tolerant.

All of the external interfaces provided by the FPGA are fully described in the SMT6400 help file.

The Sundance High-speed BUS (SHB) specification can be found here.

The SDL specification can be found here.

The FPGA configuration is done in two steps:

First asserting the prog line clears the FPGA configuration. This is simply done by an access in EMIFB CE2.

Then after the FPGA configuration has cleared the FPGA configuration is programmed serially by writing the data from the flash in EMIFB CE3.

At the end of the programming a register is polled to wait until the FPGA is configured and proceed with the application loading process.

## External Clock

An external clock input is provided to the FPGA. This signal is directly connected to the secondary TIM connector user defined pin 12.

## Version control

Version number for FPGA firmware and boot code is stored in the Flash ROM during programming as zero-terminated ASCII strings. These are displayed when using the SMT6001 utility.

## Reprogramming the firmware and boot code

The reprogramming of the module is done using the SMT6001.

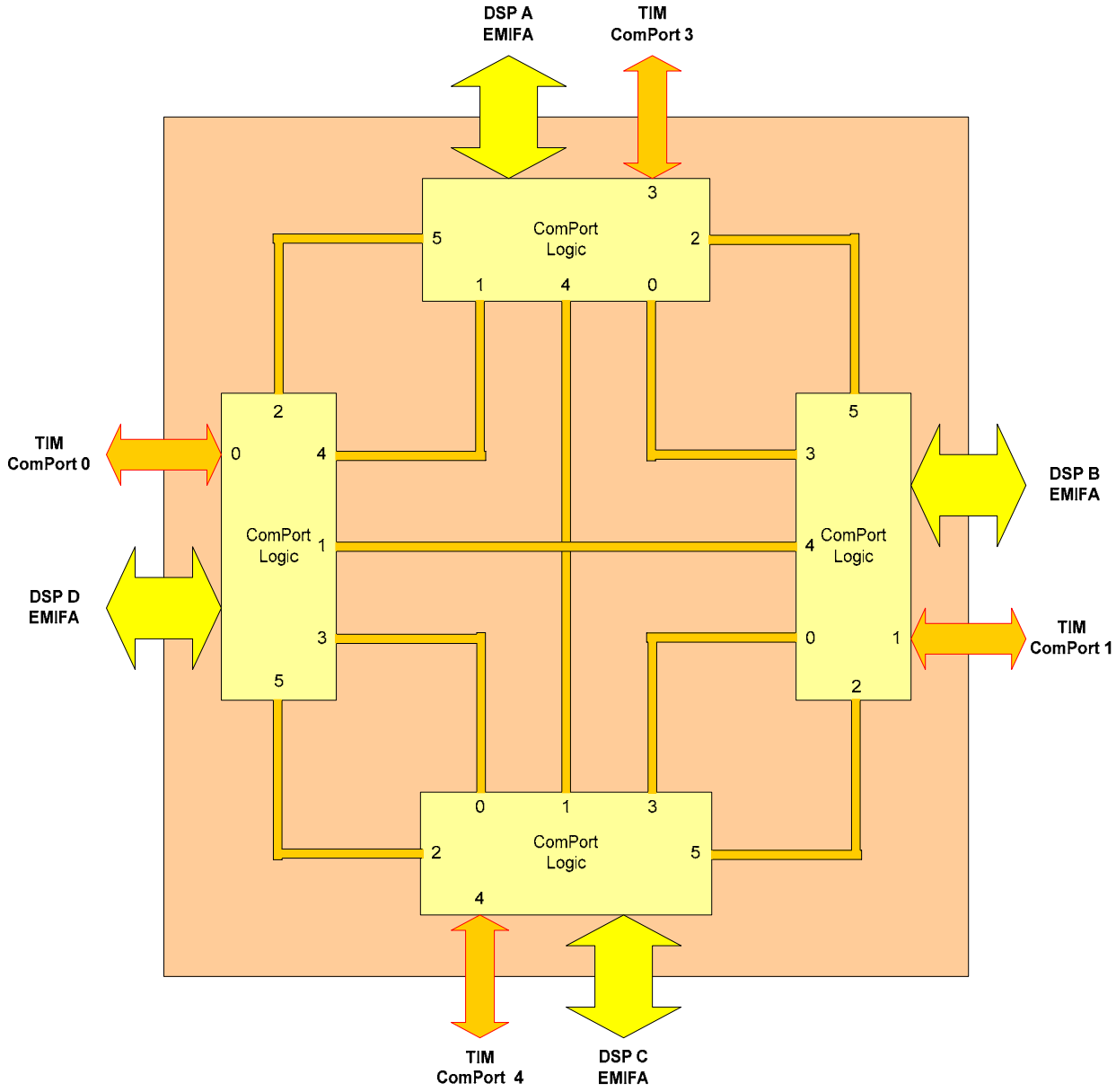
It contains the latest boot code and FPGA firmware for it and allows storing a user application in it.

# FPGA ressources

## *ComPorts*

The SMT361Q provides 6 ComPorts (0, 1, 2, 3, 4 and 5) for each DSP among which one of them is external.

The ComPort architecture is as follows:




See *SMT6400 help file*

### Interrupts

See *SMT6400 help file*

### *SDB*

The SMT361Q provides two SHB available to DSP_A that are 32-bit SDB.

They are numbered SDB_0 for SHB_A, SDB_1 for SHB_B.

See *SMT6400 help file*

SDB Clock selection

The SDB clock selection is not implemented. The clock is running at the EMIF speed i.e. 100MHz.

### *Global bus*

The SMT361Q provides one global bus interface available to DSP_A.

See *SMT6400 help file*

### *CONFIG & NMI*

Only DSP_A has control over these bits.

See *SMT6400 help file*

### *Timer*

Only DSP_A has control over the timer pins.

See *SMT6400 help file*

### *IIOF interrupt*

The firmware allows DSP_A to generate pulses on the external interrupt lines of the TIM.

See *SMT6400 help file*

### *LED*

The SMT361Q has 21 LEDs.

The LED D14 on the top right corner of the module always displays the state of the FPGA DONE pin. This LED is off when the FPGA is configured (DONE=1) and on when it is not configured (DONE=0).

This LED should go on when the board is first powered up and go off when the FPGA has been successfully programmed (this is the standard operation of the boot code resident in the flash memory device). If the LED does not light at power-on, check that you have the mounting pillars and screws fitted properly. If it stays on, the DSP is not booting correctly, or is set to boot in a non-standard way.

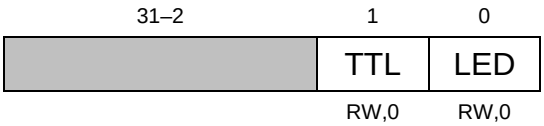
Each DSP can directly control the state of 4 LEDs connected to the GPIO pins 12 to 15.

Each DSP can control the state of 1 LEDs and one TTL pins through the FPGA.

Writing 1 will illuminate the LED; writing 0 will turn it off.

LED Register

**LED 0x900D0000**




### *TTL pins*

The SMT361Q has 4 TTL signals available (one from each DSP) available on connector JP3.

## Code Composer Studio

This module is fully compatible with the Code Composer Studio (CCS) debug environment (version 2.21 or later). This extends to both the software and JTAG debugging hardware.

The name of the C64xx CCS device driver is tixds64xx_11.dvr, and should be obtained from Texas Instruments.

In case of difficulty please contact the Sundance support team.

## Operating Conditions

### *Safety*

The module presents no hazard to the user.

### *EMC*

The module is designed to operate within an enclosed host system that provides adequate EMC shielding. Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system.

The module is protected from damage by fast voltage transients introduced along output cables from outside the host system.

Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.

### *General Requirements*

The module must be fixed to a TIM40-compliant carrier board.

The SMT361Q TIM is in a range of modules that must be supplied with a 3.3V power source. In addition to the 5 V supply specified in the TIM specification, these new generation modules require an additional 3.3 V supply to be presented on the two diagonally-opposite TIM mounting holes. The lack of this 3.3 V power supply should not damage the module, although it will obviously be inoperable; prolonged operation under these circumstances is not recommended.

The SMT361Q is compatible with all Sundance TIM carrier boards. It is a 5V tolerant module, and as such, it may be used in mixed systems with older TIM modules, carrier boards and I/O modules.

Use of the TIM on SMT327 (cPCI) motherboards may require a firmware upgrade. If LED D6 on the SMT361Q remains illuminated once the TIM is plugged in and powered up, the SMT327 needs the upgrade. The latest firmware is supplied with all new boards shipped. Please contact Sundance directly if you have an older board and need the upgrade.

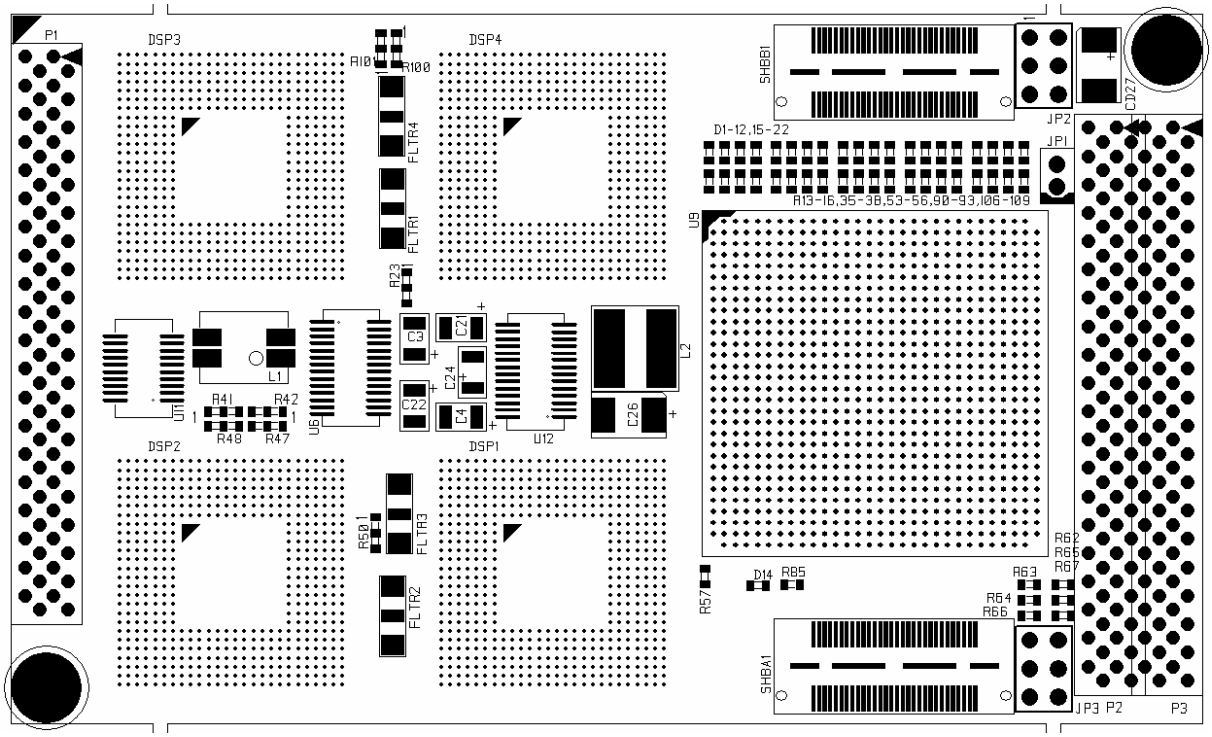
The external ambient temperature must remain between 0°C and 40°C, and the relative humidity must not exceed 95% (non-condensing).

### *Power Consumption*

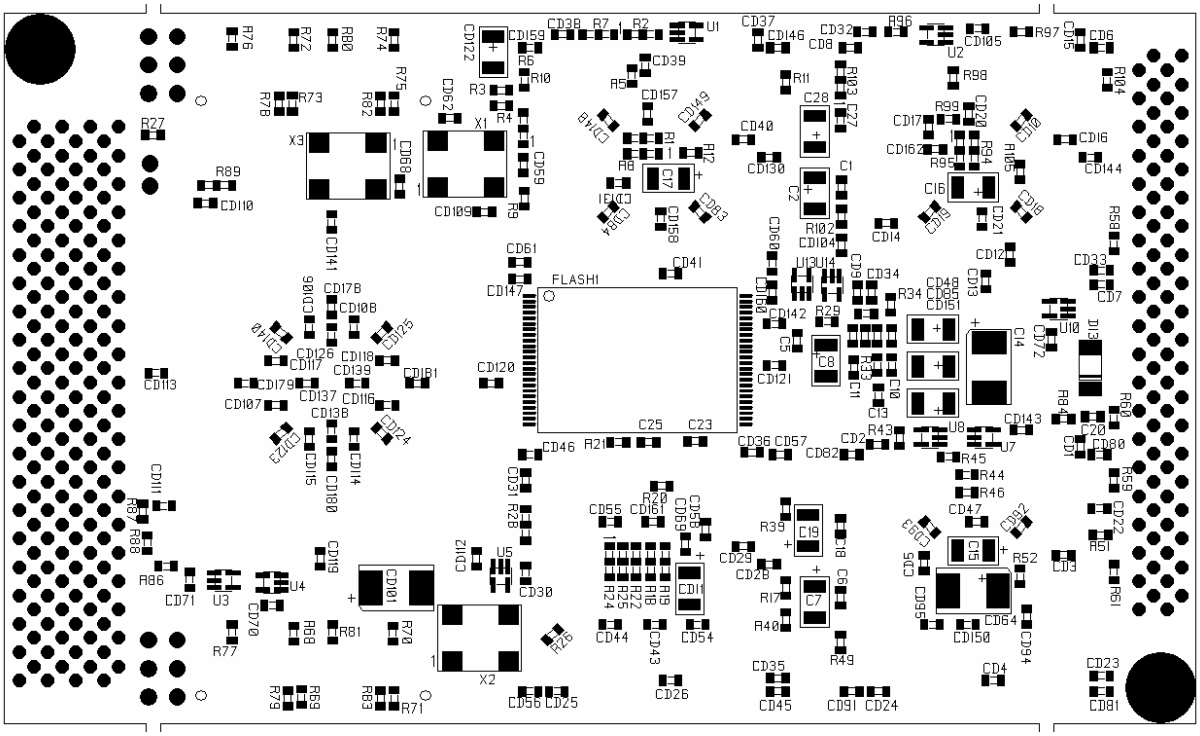
The power consumption of this TIM is dependent on the operating conditions in terms of core activity and I/O activity. The maximum power consumption is 10W.

## PCB description

### *Component Side*



## Solder Side


FLASH1
X1
X2
X3
U1
U2
U3
U4
U5
U7
U8
U10
U13
U14
C1
C2
C3
C7
C8
C13
C14
C15
C16
C17
C19
C28
R1
R2
R3
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R89
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R94
R95
R96
R97
R98
R99
R102
R104
R105
D13

# Connector Pinouts

### *FPGA PROG Pin Control (JP1)*

The FPGA PROG pin is used to clear the FPGA configuration.

It is to be used as a safety in case the FPGA has been programmed with a bad bitstream that corrupts the dsp external bus and prevents which any further programming. Removing the jumper allows the user to clear the FPGA configuration and reprogram the FPGA. A jumper must always be fitted for proper operation.

### *FPGA JTAG (JP2)*

The following shows the pin-outs for JP2 (FPGA) JTAG connector:

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| V33 | 1 | 2 | TCK |
| GND | 3 | 4 | TMS |
| TDO | 5 | 6 | TDI |

### *TTL (JP3)*

The following shows the pin-outs for JP3 TTL connector:

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| V33 | 1 | 2 | TTL DSP_A |
| TTL DSP_D | 3 | 4 | TTL DSP_C |
| TTL DSP_B | 5 | 6 | GND |

### *SHB pinout*

| Pin | Signal | Signal | Pin |
|---|---|---|---|
| 1 | SHB_CLK | SHB_D0 | 2 |
| 3 | SHB_D1 | SHB_D2 | 4 |
| 5 | SHB_D3 | SHB_D4 | 6 |
| 7 | SHB_D5 | SHB_D6 | 8 |
| 9 | SHB_D7 | SHB_D8 | 10 |
| 11 | SHB_D9 | SHB_D10 | 12 |
| 13 | SHB_D11 | SHB_D12 | 14 |
| 15 | SHB_D13 | SH_D14 | 16 |
| 17 | SHB_D15 | SHB_U0 | 18 |
| 19 | SHB_U1 | - | 20 |
| 21 | - | SHB_WEN | 22 |
| 23 | SHB_REQ | SHB_ACK | 24 |
| 25 | - | - | 26 |
| 27 | - | - | 28 |
| 29 | - | - | 30 |
| 31 | - | - | 32 |
| 33 | - | - | 34 |
| 35 | - | - | 36 |
| 37 | SHB_CLK | SHB_D16 | 38 |
| 39 | SHB_D17 | SHB_D18 | 40 |
| 41 | SHB_D19 | SHB_D20 | 42 |
| 43 | SHB_D21 | SHB_D22 | 44 |
| 45 | SHB_D23 | SHB_D24 | 46 |
| 47 | SHB_D25 | SHB_D26 | 48 |
| 49 | SHB_D27 | SHB_D28 | 50 |
| 51 | SHB_D29 | SHB_D30 | 52 |
| 53 | SHB_D31 | SHB_U0 | 54 |
| 55 | SHB_U1 | - | 56 |
| 57 | - | SHB_WEN | 58 |
| 59 | SHB_REQ | SHB_ACK | 60 |

 Not implemented

FPGA Memory Map

See *SMT6400 help file*

The memory mapping is as follows:

DSP_A memory map:

```
#define CP0                     (volatile unsigned int *)0xB0000000
#define CP1                     (volatile unsigned int *)0xB0008000
#define CP3                     (volatile unsigned int *)0xB0018000
#define CP4                     (volatile unsigned int *)0xB0020000
#define CP0_STAT                (volatile unsigned int *)0xB0004000
#define CP1_STAT                (volatile unsigned int *)0xB000C000
#define CP3_STAT                (volatile unsigned int *)0xB001C000
#define CP4_STAT                (volatile unsigned int *)0xB0024000
#define GB_STAT                 (volatile unsigned int *)0xB0034000
#define SDB_STAT                (volatile unsigned int *)0xB0038000
#define STAT                    (volatile unsigned int *)0xB003C000
#define SDB_A                   (volatile unsigned int *)0xB0040000
#define SDB_B                   (volatile unsigned int *)0xB0050000
#define SDB_A_STAT              (volatile unsigned int *)0xB0048000
#define SDB_B_STAT              (volatile unsigned int *)0xB0058000
#define SDB_A_INPUTFLAG         (volatile unsigned int *)0xB0044000
#define SDB_B_INPUTFLAG         (volatile unsigned int *)0xB0054000
#define SDB_A_OUTPUTFLAG        (volatile unsigned int *)0xB004C000
#define SDB_B_OUTPUTFLAG        (volatile unsigned int *)0xB005C000
#define GLOBAL_BUS              (volatile unsigned int *)0xB00A0000
#define GLOBAL_BUS_CTRL         (volatile unsigned int *)0xB0080000
#define GLOBAL_BUS_START        (volatile unsigned int *)0xB0088000
#define GLOBAL_BUS_LENGTH       (volatile unsigned int *)0xB0090000
#define TCLK                    (volatile unsigned int *)0xB00C0000
#define TIMCONFIG               (volatile unsigned int *)0xB00C8000
#define LED                     (volatile unsigned int *)0xB00D0000
#define INTCTRL4                (volatile unsigned int *)0xB00E0000
#define INTCTRL4_EXT            (volatile unsigned int *)0xB00E4000
#define INTCTRL5                (volatile unsigned int *)0xB00E8000
#define INTCTRL5_EXT            (volatile unsigned int *)0xB00EC000
#define INTCTRL6                (volatile unsigned int *)0xB00F0000
```

```
#define INTCTRL6_EXT                (volatile unsigned int *)0xB00F4000
#define INTCTRL7                    (volatile unsigned int *)0xB00F8000
#define INTCTRL7_EXT                (volatile unsigned int *)0xB00FC000
```

DSP_B, DSP_C, DSP_D memory map:

```
#define CP0                         (volatile unsigned int *)0xB0000000
#define CP1                         (volatile unsigned int *)0xB0008000
#define CP3                         (volatile unsigned int *)0xB0018000
#define CP4                         (volatile unsigned int *)0xB0020000
#define CP0_STAT                    (volatile unsigned int *)0xB0004000
#define CP1_STAT                    (volatile unsigned int *)0xB000C000
#define CP3_STAT                    (volatile unsigned int *)0xB001C000
#define CP4_STAT                    (volatile unsigned int *)0xB0024000
#define GB_STAT                     (volatile unsigned int *)0xB0034000
#define LED                         (volatile unsigned int *)0xB00D0000
#define INTCTRL4                    (volatile unsigned int *)0xB00E0000
#define INTCTRL5                    (volatile unsigned int *)0xB00E8000
#define INTCTRL6                    (volatile unsigned int *)0xB00F0000
#define INTCTRL7                    (volatile unsigned int *)0xB00F8000
```

## FPGA Pinout

See board schematics.

## Bibliography

1. C6000 Peripherals Reference Guide (literature number SPRU190)
   Describes common peripherals available on the TMS320C6x digital signal processors. This book includes information on the internal data and program memories, the external memory interface (EMIF), the host port, multichannel-buffered serial ports, direct memory access (DMA), clocking and phase-locked loop (PLL), and the power-down modes.

2. TIM-40 MODULE SPECIFICATION Including TMS320C44 Addendum

3. SHB Technical Specification

4. SDB Technical Specification

5. TMS320C4x User's Guide (literature number SPRU063)
   Describes the C4x 32-bit floating-point processor, developed for digital signal processing as well as parallel processing applications. Covered are its architecture, internal register structure, instruction set, pipeline, specifications, and operation of its six DMA channels and six communication ports. Software and hardware applications are included.

6. Xilinx Virtex-II datasheet and application notes

7. SMT6400 help file

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