APPLICATION NOTE 1

Application note detailing the differences between the SMT363V and SMT363XC2

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This document describes the differences between the SMT363XC2 and the SMT363V.

1) The NET+50 runs at 44.3MHz (the older modules have a clock of 33MHz). The consequence of this is that all internal timers including the baud rate generators will run faster and so the BRG divisor will need to be changed.

The memory access timings to the DPRAM are also altered. The minimum external memory access for the NET+50 is two clock cycles. On the 363V this equates to 60ns (33MHz = 30ns cycle time). On the 363XC2 this cycle time has been extended by setting the CS0 Control register wait field to 2 (which equates to a cycle time of 67ns). This register is at address 0xFFC00014, and has the value 0xFFFC0200 stored within it.

2) There should no longer be any flash memory race condition. This is prevented with the addition of the DSP's ARE signal into the CPLD (XC9536XL). It is still good practice, however, to perform a flash reset command prior to issuing erase (or other) commands.

3) The FPGA is an XC2V1000. The default configuration for this is a simple confidence check which flashes two LEDs. Note that the bitstream size is different. The DSP's boot code should use the value 255194 (words) as the configuration length. The 363V used the erroneous value 234457 (twice the actual required value).

4) The FPGA is now in the JTAG chain together with the XC9536XL CPLD. Access to this chain is via JP3 (pin-out in the design spec).

5) Connection to the Ethernet and RS232 signals is via a latching pin header. The pin-out is given in the design spec.

6) The Ethernet PHY is an Intel part (older modules used the now obsolete Lucent device).

7) There are 8 LEDs.

LED #	Function
1	Connected to the FPGA DONE pin. This LED is illuminated when the FPGA does NOT contain a valid configuration.
2	Connected the the FPGA pin V5
3	Connected the the FPGA pin V4
4	Connected to the NET+50 PORTA0 pin 45
5	Connected to the NET+50 PORTA1 pin 44
6	Connect to the Intel PHY pin CFG3 (shows activity on the Ethernet connection)
7	Connect to the Intel PHY pin CFG2
8	Connect to the Intel PHY pin CFG1

8) The addition of jumper JP5 allows for the continuous assertion of the FPGA's PROG pin. This can be useful to stop the FPGA from being configured during the boot process (which can be necessary if a non-working configuration has been loaded into flash).

9) The 363V's SDB connector (40 pin ODU type) has been replaced by an SHB connector (60 pin Samtec QSE series). All 60 pins are connected directly to the FPGA.