HARDWARE SPECIFICATION

FOR

SMT368

Note:

If this copy is no longer in use, return to sender.

APPROVAL PAGE

Name	Signature	Date

AUTHOR/S

Name	Signature	Date
G Parker		7/2/2005

DOCUMENT HISTORY

Date	Initials	Revision	Description of change
7/2/05	GKP	1.0	First release
8/2/05	GKP	1.01	Added FPGA bank/pin table
8/2/05	GKP	1.02	Added PCB layout
15/2/05	GKP	1.03	Detailed SLB and LVDS pins.
22/9/05	GKP	1.04	Minor typos corrected.

TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

1. SCOPE

This document specifies the requirements for The SMT368VP FPGA Tim module

1.1. INTRODUCTION

The SMT368 is a TIM module in the range of Sundance Virtex 4 FPGA modules.

It provides a communications platform between a XC4VSX35 FPGA and

- On-board 166MHz ZBT memory.
- SHBs.
- LVDS connections for high speed parallel connections
- LVTTL connections and connectors.

This variety of connectors and interfaces provides a wide range of development options for designers to explore the capabilities of the comprehensive Sundance TIM modules family.

1.2. PURPOSE

The SMT368 must:

- Provide high-speed interface to Sundance ADC/DAC modules
- Provide high-speed interface to Sundance DSP modules.
- In any configuration on Sundance carriers, i.e on its own, on a stand-alone carrier or in a Host as part of a system.

1.3. APPLICABILITY

Interface to other FPGA, DSP, ADC/DAC modules and in stand alone systems.

2. APPLICABLE DOCUMENTS AND REFERENCES

2.1. APPLICABLE DOCUMENTS

2.1.1. External Documents

TI TIM specification & user's guide.

Samtec QSH Catalogue page

Virtex 4 Datasheet

2.1.2. Internal documents

SUNDANCE SDB specification.

SUNDANCE SHB specification

SUNDANCE SLB specification

2.1.3. Project Documents

Smt368 QCF14.mpp Project Planning Document.

2.2. REFERENCES

2.2.1. External documents

N.A

2.2.2. Internal documents

N.A

2.2.3. Project documents

N.A

2.3. PRECEDENCE

In the event of conflict between the text of this document, and the applicable documents cited herein, the text of this document takes precedence. Nothing in this document however, supersedes applicable laws and regulations unless a specific exemption has been obtained and is identified in the text of this document.

3. ACRONYMS, ABBREVIATIONS AND DEFINITIONS

3.1. ACRONYMS AND ABBREVIATIONS

TIM	Texas Instruments Module

3.2. DEFINITIONS

TIM carrier	A circuit board which contains TIM site(s). Typically these also contain an interface to a host (PCI, VME), or various interfaces for standalone operation.

4. REQUIREMENTS

4.1. PRIME ITEM DEFINITION

This module conforms to the TIM standard (**T**exas **I**nstrument **M**odule, See TI TIM specification & user's guide) for single width modules.

It sits on a carrier board.

The carrier board provides power, Ground, communication links (Comport links) between all the modules fitted and a pathway to the host, for a non stand-alone system.

The SMT368 requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards), which must be provided by the two diagonally opposite mounting holes.

4.1.1. Prime Item Diagrams

Figure 1 shows a simplified version of the SMT368 module

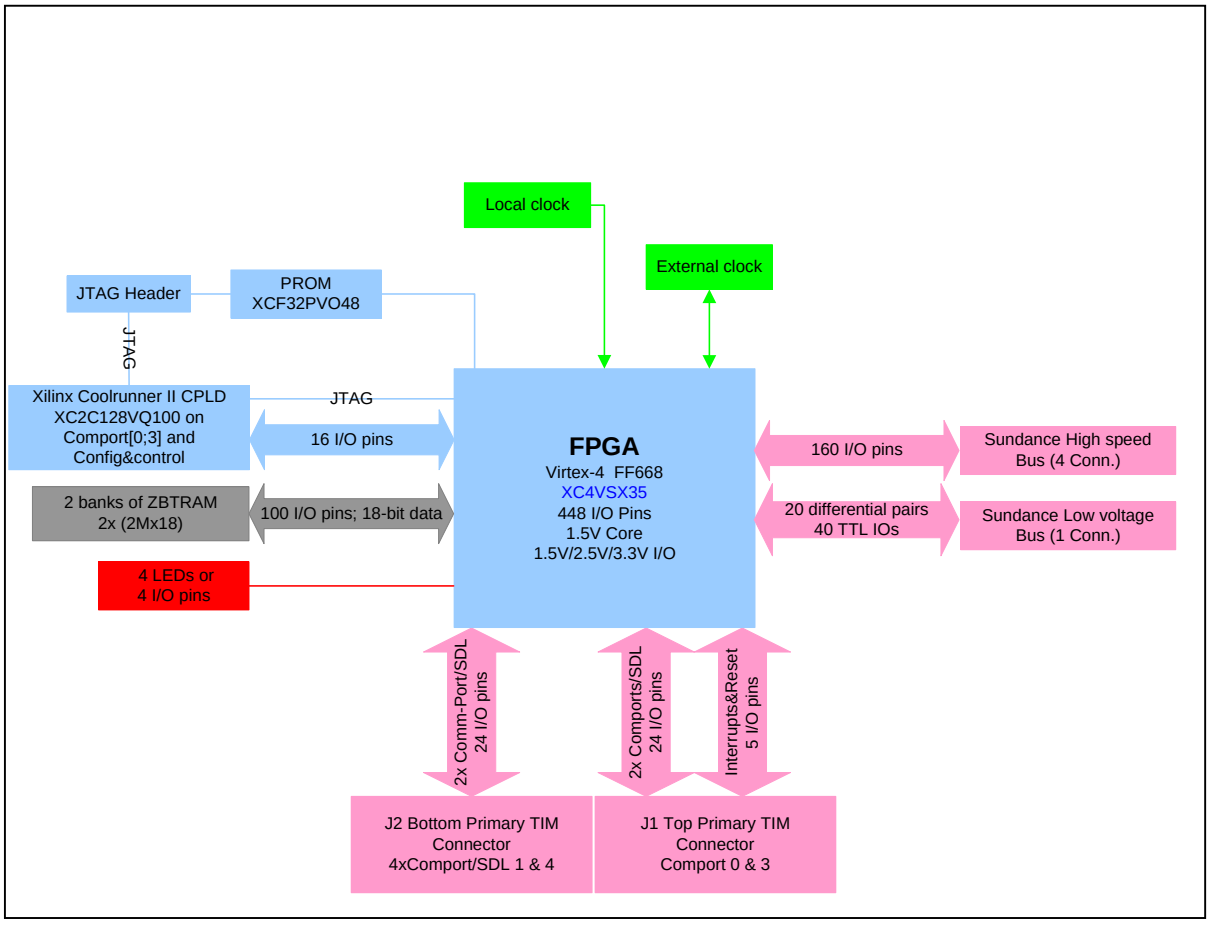

Figure 1: Block Diagram

4.1.2. Interface Definition

For the TIM to carrier board or external world interfacing, see in Sundance Help file (that you can download from this link)

4.1.3. Major Component List

- Block1: Xilinx Virtex 4 XC4VSX35 and configuration scheme.
- Block2: ZBT SRAM memory.
- Block3: IO connectors for general purpose or dedicated interfaces.
- Block4: 100MHz local clock, and external clock input.
- Block5: Leds for development and in-use monitoring and general purpose use.

4.1.4. Prime Item Characteristics

4.1.4.1. FPGA

Xilinx Virtex 4 XC4VSX35FF668 FPGA.

This device is packaged in a 668-pin BGA package.

4.1.4.2. CPLD

Xilinx Coolrunner II device XC2C128-6VQ100C This device is packaged in a 100-pin very Thin QFP package with a -6 speed grade.

It can be used to configure the FGPA via Comport 0 or 3.

4.1.4.3. PROM

Xilinx Flash PROM device XCF32PVO48.

Accessed via JTAG to load an FPGA configuration bitstream.

Then, it can be used to configure the FPGA at power up.

Parallel FPGA configuration interface (up to 33 MHz)

Design revision technology enables storing and accessing multiple design revisions for configuration.

Built-in data decompressor compatible with Xilinx advanced compression technology.

4.1.4.4. JTAG Header

The JTAG header is compatible with Xilinx Parallel-IV cable signals.

It supports code download (for the FPGA Power PC), FPGA configuration, Hardware and Software Debugging tools for the Virtex-II Pro.

This cable connects the parallel port of an engineer's Workstation/PC to the JTAG chain of the SMT368 Module.

All the devices from block1 are chained and accessible via this JTAG header.

4.1.4.5. FPGA Configuration schemes

Different schemes are available to provide maximum flexibility in systems where the SMT368 is involved:

The FPGA configuration bitstream source is

- one of the 2 Comports:

The CPLD is connected to 2 Comport links of the SMT368 TIM connector. A switch is used to select the configuration Comport that will be used to receive the bitstream.

The CPLD allows for FPGA configuration in slave SelectMap mode.

- Using the on-board Flash PROM.

The CPLD monitors the configuration data between the Xilinx Flash PROM and the FPGA. The FPGA configuration is operated in Master SelectMap mode.

- Using the on-board JTAG header and Xilinx JTAG programming tools.

The JTAG header is a Parallel-IV Header.

4.1.4.6. ZBT SRAM

Up to 8 Mbytes of ZBT SRAM

The memory is available as 2 independent banks of ZBT.

The ZBT memory runs at 166MHz. This particular type of memory allows completely random addressing on each clock cycle, which is ideal for many DSP oriented functions.

Each bank is fully independent with separate address, control and data busses.

The 2 devices used are Samsung ??????. Alternative part numbers, fully compatible can be fitted depending on availability at time of order.

4.1.4.7. Sundance High speed Bus

4 x 60 pins connectors provide 160 IO connections between the FPGA and the outside word.

They allow interfacing to other Sundance modules providing that you implement an SHB interface in the FPGA. (See 2.1.2.)

The SHB interface is available in Sundance SMT6500 support package. Either two 16-bit, or 1 32-bit interface can be implemented per connector.

They allow interfacing to the outside world by implementing your own interface in the FPGA.

The FPGA IO banks hosting the SHB signals are powered using Vcco = 3.3v.

4.1.4.8. Sundance Low voltage Bus

This is an LVDS bus comprising data (2 x 16 bit buses, I & Q), clock, and control signals.

They allow interfacing to Sundance mezzanine modules providing that you implement an SLB interface in the FPGA. (See 2.1.2.)

They allow interfacing to the outside world by implementing your own LVDS interface in the FPGA.

14 LVDS data pins (both I and Q) are connected to a 2.5V powered FPGA bank. The LVDS Clock signal is also on this bank. A 2.5V bank has the ability to use the LVDS_25_DCI inputs. All other LVDS signals are input to a 3.3V powered FPGA bank. This bank cannot use LVDS_25_DCI and cannot output LVDS signals, but these signals are unimportant for 14-bit ADC and DAC operations.

4.1.4.9. TIM Connectors

TIM connectors provide 4 communication links (Comports) to the FPGA.

They allow interfacing to Sundance TIM modules or to a Host PC providing that you implement Comport Interface inside the FPGA. (See 2.1.2.)

The Comport interface is available in Sundance SMT6500 support package.

The FPGA io banks hosting the Comport signals are powered using Vcco = 3.3v.

The TIM connectors also provide power/ground, reset and various control signals.

References and specifications for these connectors are available on Sundance Web site

4.1.4.10. DIP Switches

- One four-position DIP switch is connected to the FPGA I/Os for general purpose use in an FPGA design.
- One four-position DIP switch is connected to the CPLD to provide control over the selection of the configuration bitstream source and a special reset feature called “TIM Confign”.

JPC 4	TIM Config
ON	ENABLED
OFF	DISABLED

Table 1: DIP switch for special reset feature

JPC 3,2, 1	JPC3	JPC2	JPC1
C0P	ON	ON	ON
C3P	OFF	OFF	OFF
PROM	ON	ON	OFF

Table 2: DIP switch for the selection of the configuration bitstream source

4.1.4.11. Clocking scheme

The SMT368 module contains a 100MHz LVTTL clock, and a connector for external LVTTL clock input/output.

- 100 MHz LVTTL oscillator: Main system clock. Can be input in a DC

4.1.4.12. LEDs

- 4 Red LEDs connect to the FPGA and are available to the User.
- 1 Green LED connects to the DONE pin of the FPGA to show FPGA is configured. The LED is turned on when the FPGA is configured.

4.1.5. Performance

The FPGA features like speed grade and density dictate most performances.

The performances achievable by the other components are given in the 4.1.4. Prime Item Characteristics chapter.

4.1.6. Physical Characteristics

4.1.6.1. Power budget

Table 3: Power budget.

Device	Quantity	Voltage(V)	Current(mA)	Power(W)	Source
Samsung ZBT	2	3.3			
25 MHz Clock oscillator	1	3.3	10	0.033	Jauch VX3 Quartz crystal oscillators datasheet
LEDs	5	3.3	10	0.165	
DIP Switch	1	2.5	2.1	0.005	Four 4.7 Kohm pullup
XC4VSX35	1	Must be calculated based on design			
Coolrunner II CPLD (See details)	1	1.8	17mA	0.031	CPLD power calculator

Details:

Coolrunner II CPLD power requirement based on design:

During FPGA configuration only, the Coolrunner CPLD power consumption is at its maximum:

- Macrocells used: 40
- Macrocells used as outputs or bidirectional: 26
- Fmax:100MHz
- The average toggle rate of all flip-flops:40%
- Number of product terms:69

5. FOOTPRINT

5.1. TOP VIEW

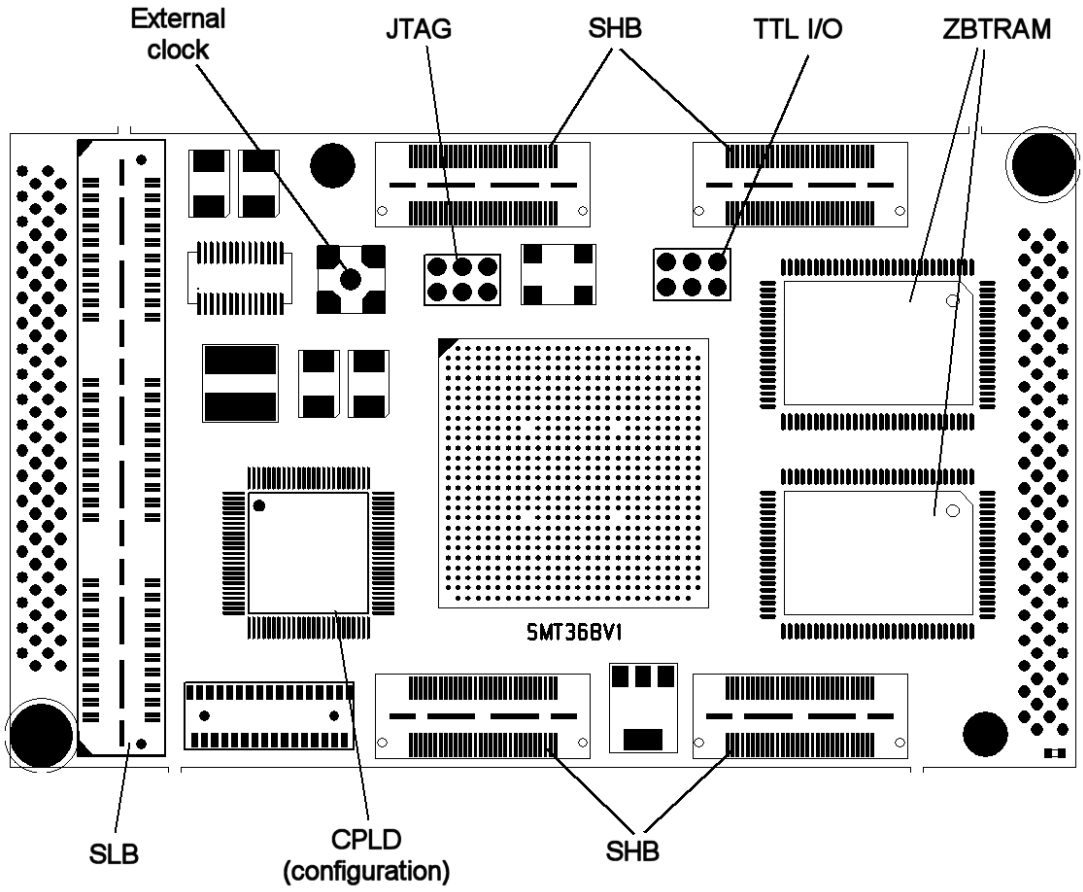

Figure 2: Top View

5.2. BOTTOM VIEW

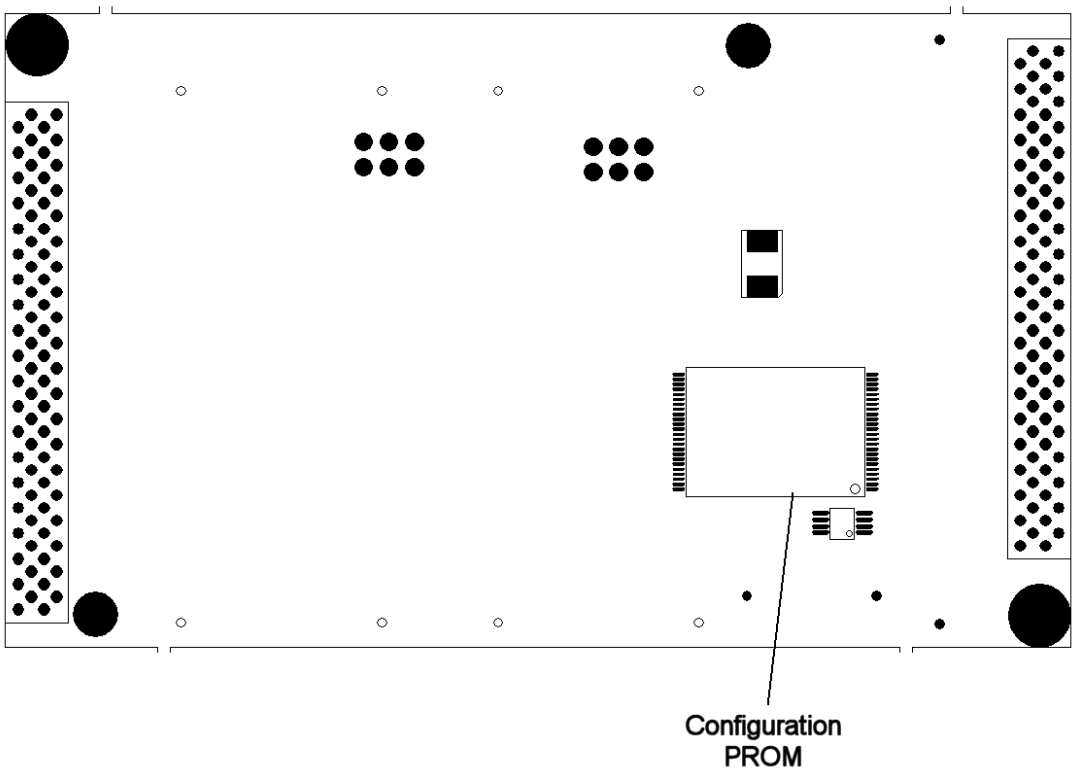

Figure 3: Bottom View

6. PINOUT

6.1. FPGA PIN ALLOCATION BY BANK

Bank	I/O	Vrp/Vrn	ZBT	SHB	CP	SLB	Other	Total
1	16	0		16				16
2	16	0		8			8	16
3	16	0		16				16
4	16	0		8			8	16
5	64	0	49		12		2	63
6	64	0		48	12		4	64
7	64	0		64				64
8	64	0			12	47	5	64
9	64	0	49		12		3	64
10	64	2				62		64

Total pin count **447**

6.2. SHB

SUNDANCE SHB specification

6.3. SLB

SUNDANCE SLB specification

7. QUALIFICATION REQUIREMENTS

7.1. QUALIFICATION TESTS

7.1.1. Meet Sundance standard specifications

- Meet the TIM standard specifications
- Meet the SLB specifications (LVDS standard).
- Meet the SHB specifications.

7.1.2. Speed qualification tests

- ZBT memory accesses at 166MHz.

7.1.3. Integration qualification tests

- Must work on ALL Sundance platforms as a root TIM module or as part of a network of TIMs on carriers.
- Must be able to work stand-alone.