iUnit / Module Description:	Dual C6472 EVM
Unit / Module Number:	SMT372T
Document Issue Number:	2.0
Issue Date:	24th June 2013
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Product Specification for SMT372T

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Certificate Number FM 55022

Revision History

Issue	Changes Made	Date	Initials
1.0	First release.	12th May 2009	GKP
1.1	Update.	14th May 2009	GKP
1.2	Added top RSL connector.	14th May 2009	GKP
1.3	Added FPGA I/O table.	19th May 2009	GKP
1.4	Corrected number of McBSPs, and their connectivity. Changed the Ethernet PHY model. Commented that the DSPs' GPIO driver LEDs.	26th May 2009	GKP
1.5	Removed reference to 16 GTX on FX70.	16th July 2009	GKP
1.6	Updated board layout drawing.	8th Sept 2009	GKP
1.7	Corrected McBSP references to UTOPIA	11th March 2010	GKP
1.8	Added JP4 detail	4th May 2010	GKP
1.9	Added DSP GPIO section	7th July 2010	GKP
1.10	Added RJ45 pin-out detail and link the SMT562E. Corrected part number typo.	20th January 2011	GKP
1.11	Added max FPGA power details.	30th Nov 2011	GKP
2.0	Major update: Added FPGA pin out. Update DIP switch description.	24th June 2013	GKP

Table of Contents

1 Introduction / Description

The SMT372T is a dual C6472 single width TIM comprising:

- 2 TI C6472 6-core DSPs
- Xilinx Virtex5 FXxxT FPGA
- Two x16 DDR2 devices per DSP
- 10/100/1000 Ethernet PHY
- RSL connectors
- 64MByte flash memory

2 Related Documents

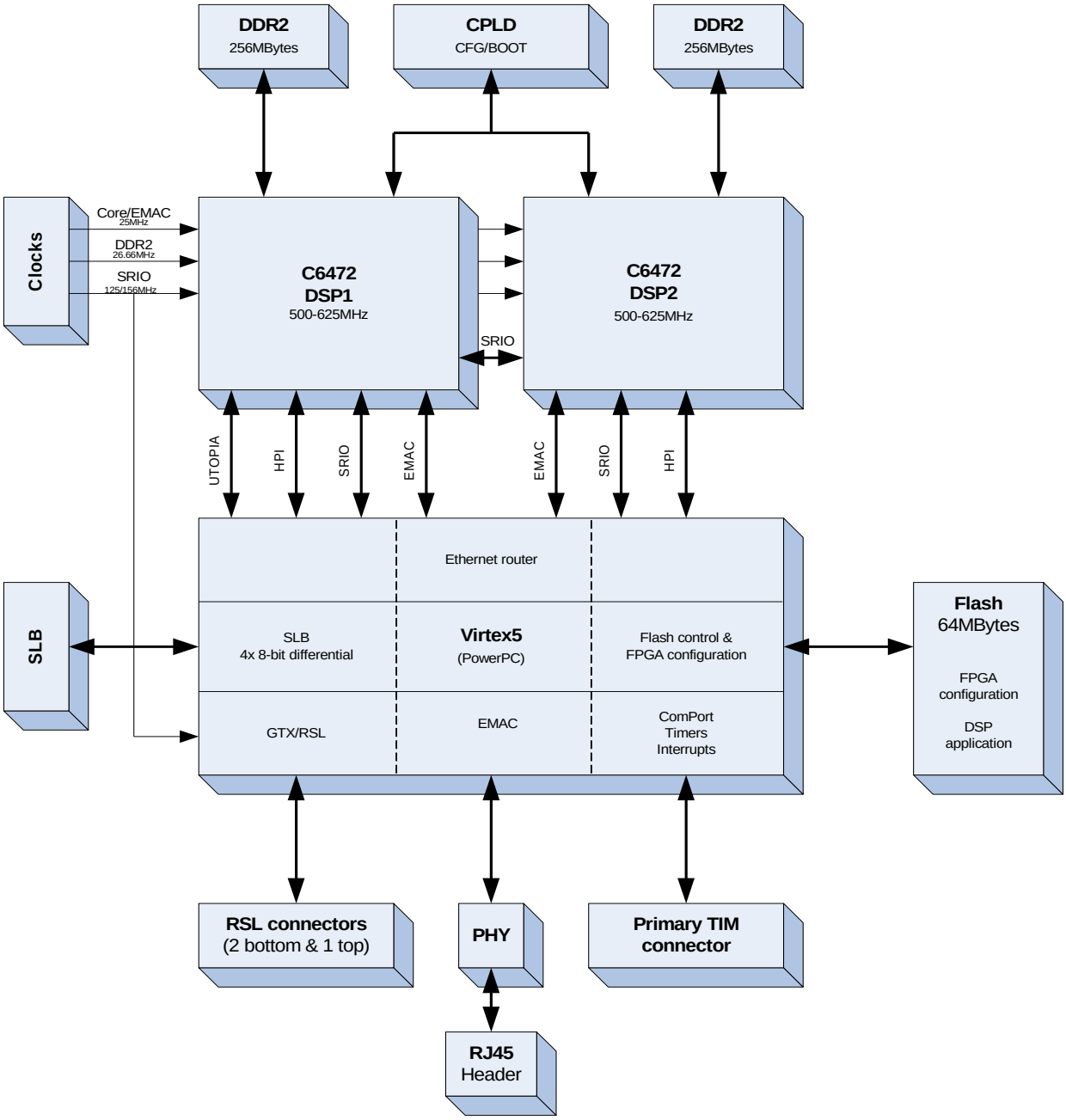
Xilinx Virtex5 documentation:
http://www.xilinx.com/support/documentation/virtex-5.htm

A wiki for the SMT372T can be found here:
http://wiki.sundance.com/index.php/SMT372T

3 Acronyms, Abbreviations and Definitions

A list of acronyms etc: http://www.sundance.com/web/files/static.asp?pagename=acc

4 Block Diagram



5 Module Description

5.1 TI C6472 DSP

The SMT372T module includes two TI C6472 DSP devices.
Each C6472 incorporates 6 cores running at 500-625MHz.

5.1.1 DSP Clock

A 25MHz oscillator is buffered and routed to the DSPs' PLL1 and PLL2 inputs. These are used to generate the core and EMAC clocks.
The core clock multiplier can be selected to operate the device at 500-625MHz.
The EMAC always runs with a x20 PLL multiplier.

5.1.2 DSP Boot

Upon power-up or soft reset, the FPGA will configure itself from the byte-wide flash memory.
After configuration, the FPGA will load the DSPs' megamodules' boot code using HPI.
The megamodules will then be released from reset and further application loading can be either from flash or from an interface provided by the FPGA (RSL, ComPort).

5.1.3 GPIO

DSP1 has a single GPIO connection made available on the TIM connector. GP04 is connected to UDP1 (TIM pin 1).
DSP2 has two GPIO connections to the TIM connector. GP04 is connected to UDP2 (TIM pin 3), and GP03 is connected to UDP6 (TIM pin 9).

5.1.4 SRIO

Each DSP has 2 SRIO interfaces.
One SRIO from each DSP is connected together.
The second SRIO from each DSP is connected to the FPGA.
The SRIO external clock speed is 125MHz allowing operation at 1.25 and 2.5Gbps.
This is the same speed as the Sundance RSL implementation.

5.1.5 I2C

Each DSP has an I2C connection to the FPGA.
This is a slow serial interface running at up to 400kHz.
This is the simplest mechanism for the DSP to access the FPGA.

5.1.6 UTOPIA

Each DSP has a single 16-bit UTOPIA port.
The UTOPIA from DSP1 is connected to the FPGA. The remaining UTOPIA is un-connected.

A total of 50 FPGA I/O pins are needed for this interface.

5.1.7 HPI

A 16-bit interface exists from the DSPs to the FPGA using 26 I/O pins.
This is a DSP slave interface with the FPGA as the master. This interface is the mechanism by which the DSPs' boot code is loaded.
Access to all of the DSPs' resources can be made through the HPI.
The HPIs to the DSPs are independent.

5.1.8 DDR2 Memory (DDR533)

Two 16-bit wide devices are used for each DSP. Using 2G bit devices provides for 256Mbytes of memory per DSP.
The memory clock speed is 266MHz.

5.2 FPGA

A Xilinx Virtex-5 FXT device interfaces to both DSPs, the Ethernet PHY, flash memory, external GTX/RSL connectors, and other TIM resources.

The FPGA is set to master slave map configuration. Upon reset or power-up, the FPGA will configure itself from the flash memory.

See Physical Properties section for power consumption details.

5.2.1 JTAG

A 6-pin header is provided to enable programming and debugging of the CPLD and FPGA. The location of this header, JP4, is shown on the board layout drawing.

The pin-out is as follows;

TMS	TDI	TDO
4	5	6
1	2	3
VCC (3.3V)	GND	TCK

5.2.2 SLB (Sundance Local Bus)

A full implementation of the SLB is provided.
This interface incorporates 4 8-bit differential LVDS buses, general purpose LVTTL I/O, differential clocks and triggers. This interface uses 109 FPGA I/O pins.
The LVDS ports of this bus can operate at 2.5V or 3.3V; determined by jumper positions. JP1 selects the I/O voltage for the main data signals, and JP2 selects the I/O voltage for the control signals. Positions 1-2 is for 3.3V, position -3 for 2.5V.

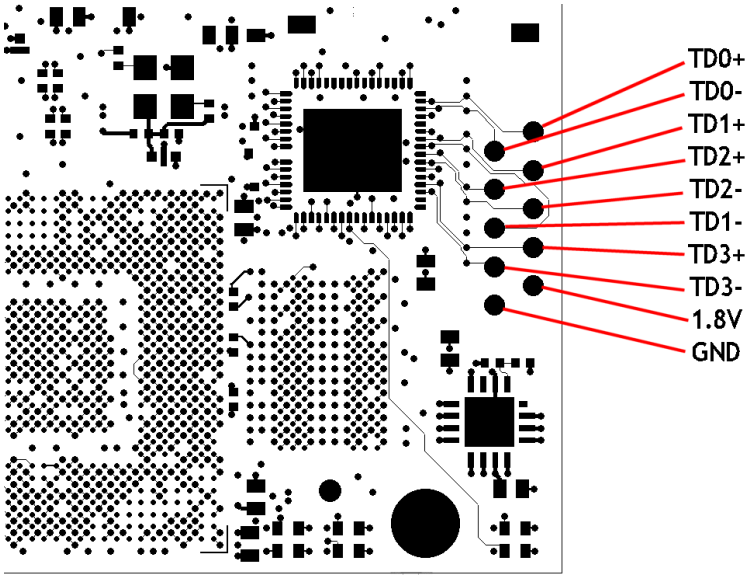
5.2.3 ComPort

A single byte-wide ComPorts is be provided through the primary TIM connector.
An interface within the FPGA translates ComPort traffic into SRIO data. This interface requires 12 FPGA I/O pins.

5.3 Ethernet PHY

A single Ethernet PHY (Marvell 88E1116) is connected to an FPGA MAC.
The DSPs' EMAC interfaces connect directly to the FPGA, and a soft router provides connectivity to the PHY and RJ45 connector/header. [Note: That a full RJ45 connector is not provided, but the signals are presented on a header.]

The pin-out of the Ethernet header is shown here:



There are three EMAC interfaces to the FPGA which requires 39 I/O pins, and a further 2 for the MDC/MDCIO interface.

It is recommended that the SMT562E be used for Ethernet connectivity (http://www.sundance.com/web/files/productpage.asp?STRFilter=SMT562E).

5.4 CPLD

A small Xilinx CPLD is provided which determines the DSPs' configuration after reset.

5.5 DIP Switch

A 4-way DIP switch is used to select module operating modes.

The DIP switch is connected directly to the FPGA. The status of the switch is visible in a read-only register by the DSPs.

Hence the functions set by the DIP switch is determined by the FPGA firmware. The default firmware results in the following:

DIP switch slider number				Mode
4	3	2	1	
On	On	On	On	DSPs boot from flash.
On	On	On	Off	Allow flash re-programming (using SMT6002).
On	On	Off	On	User defined.
On	On	Off	Off	3L Diamond mode.

5.6 DSP JTAG

For debugging the DSP using Code Composer Studio, the JTAG connection is made on the TIM carrier board via the TIM connector. Refer to the relevant carrier board information.

5.7 LEDs

Each DSP has direct connection to two LEDs. These are for general purpose use and are driven by the GP(11:10)/CFGGP(1:0) pins.

The FPGA has direct connection to 4 LEDs. These are for general purpose use.

5.8 RSL

The Virtex5FXT device in the FF665 package provides 8 lanes of GTX high-speed serial interfaces. Two are used to connect to the DSPs. The remaining 6 lanes are routed to the RSL connectors. Two lanes to each of the 3 connectors.

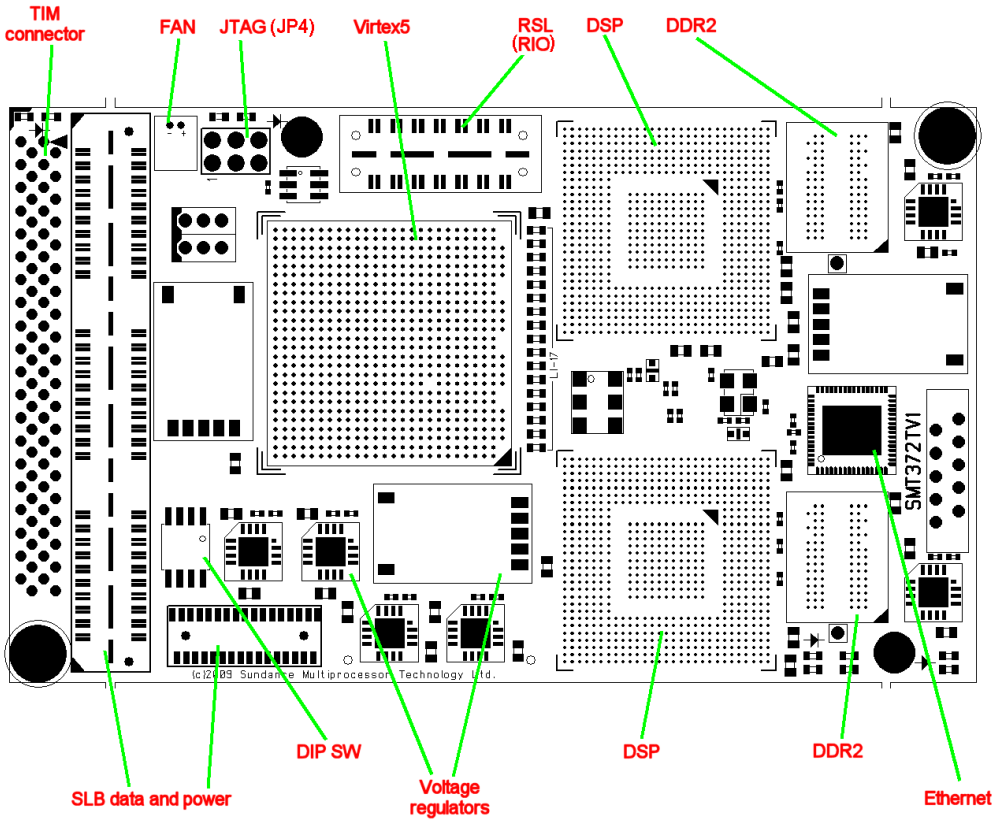
RSL communication can be routed to the DSPs' SRIO, or HPI interfaces.

5.9 Flash

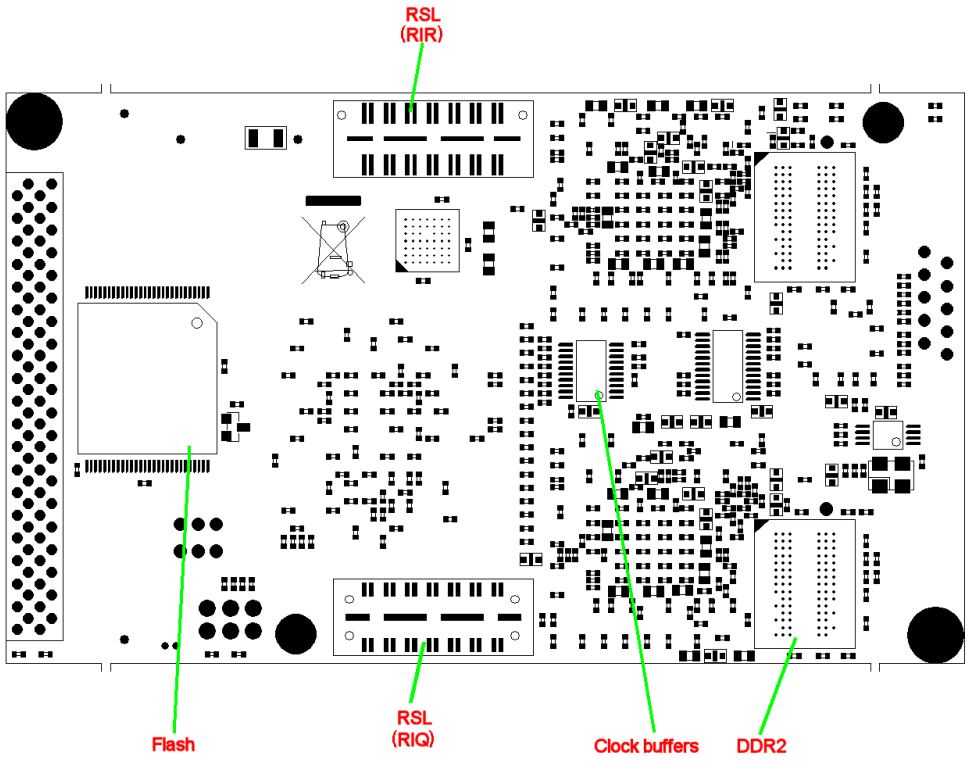
A byte-wide flash of 64M bytes provides storage for the FPGA configuration and DSP application.
The flash cannot be accessed directly from the DSP as the DSP does not have an external parallel memory interface.
Flash access by the DSP is implemented using SRIO or I2C cores within the FPGA.
It is suggested that an area of flash can be reserved to store a default FPGA configuration. This area should not be modified by the user.
[Alternatively, a slow I2C command sequence could be initiated to the FPGA that signals the start of an HPI transfer of data to flash.]

This parallel flash requires 39 FPGA I/O pins.

6 Board Layout



Top view



Bottom view

7 FPGA I/O Allocation

Sub-system	Pin name	Pin count	Instances	Sub-total	Total
SLB	Data	64	1		109
	Control	21			
	Clocks	16			
	Misc	8			
Comm ports	Data	8	1	8	12
	Control	4		4	
Clock	All	3		3	3
Flash	Add	26	1	26	38
	Data	8		8	
	Ctrl	4		4	
UTOPIA	All	25	2	50	50
HPI	All	26	2	52	52
TTL & LEDs	All	8		8	8
TIM Interrupts	NMI/IACK/IIOF/RST	7		7	7
TIM timers	TCLK	2		2	2
DSP Timers	All	3	2	6	6
TIM reset	RESET	1		1	1
DSP reset	RESET	2		2	2
TIM C4x	CONFIG	1		1	1
EMAC	All	13	3	39	39
	Other	2		2	2
DIP Switch	All	4		4	4

7.1 FPGA Pin Out

Signal	BGA	Comment

Clock, reset, interrupts, etc:

FPGA_CLK25	AB10	25MHz clock input
FPGARSTN	AB12	Reset input. Active low.
1WIRE	AD24	Interface to 1-wire device.
NMIN1	AB11	NMI input to DSP1. Active low.
NMIN2	AC11	NMI input to DSP2. Active low.
LRESETN1	E26	LRESET to DSP1.
LRESETN2	G24	LRESET to DSP2.
LRESETNMIENN1	E25	LRESETNMIEN to DSP1.
LRESETNMIENN2	E23	LRESETNMIEN to DSP2.
CRESEL1_0 CRESEL1_1 CRESEL1_2	F24 G25 G26	CORESEL bus for DSP1.
CRESEL2_0 CRESEL2_1 CRESEL2_2	G22 F22 F23	CORESEL bus for DSP2.
TIMA0 TIMA1 TIMA2	AD9 AD8 AC8	TIMI0 DSP1. TIMI1 DSP1. TIMO2 DSP1.
TIMB0 TIMB1 TIMB2	AA9 AB9 AC9	TIMI0 DSP2. TIMI1 DSP2. TIMO2 DSP2.
SCL1	AC13	I2C bus clock for DSP1.
SCL2	AC14	I2C bus clock for DSP2.
SDA1	AC12	I2C bus data for DSP1.
SDA2	AB14	I2C bus data for DSP2.

TIM interface:

NMI CONFIG IACK IIOF0 IIOF1 IIOF2 PXITRIG1 PXITRIG2 PXITRIG3 TCLK0 TCLK1	AF24 AD23 AF25 AF23 AE23 AE22 AC26 AD26 AD25 AE25 AE26	Signals direct to TIM connector.

TIM ComPort connection:

C3D0 C3D1 C3D2 C3D3 C3D4 C3D5 C3D6 C3D7	AB16 AC19 AB21 AB20 AB17 AB19 AC16 AB15	ComPort data bus.
C3D8 C3D9 C3D10 C3D11	AA20 Y21 AC17 AC18	ComPort STROBE. ComPort RDY. ComPort REQ. ComPort ACK.

Sundance Local Bus interface (SLB):

CLOCKOUTIN CLOCKOUTIP CLOCKOUTQN CLOCKOUTQP	W25 W26 B20 A20	SLB Differential Clocks.
DATAOFRANGEIN DATAOFRANGEIP DATAOFRANGEQN DATAOFRANGEQP	R26 P26 A13 B14	SLB Data Out Of Range.
EXTTRIGERIN EXTTRIGERIP EXTTRIGERQN EXTTRIGERQP	R25 P25 A19 A18	SLB External Trigger.
FPGARSCLOCKN FPGARSCLOCKP FPGASYSCLOCKN FPGASYSCLOCKP	D19 C19 V23 W24	SLB Auxiliary Clocks.
MODE0 MODE1 PSENABLE0 PSENABLE1 SERIALNUMBER SMBCLK SMBDATA SMBNALERT	M21 L25 M24 M22 N23 F25 N26 N24	Various LVTTL signals. See SLB spec.

SIGNAL0 SIGNAL1 SIGNAL2 SIGNAL3 SIGNAL4 SIGNAL5 SIGNAL6 SIGNAL7 SIGNAL8 SIGNAL9 SIGNAL10 SIGNAL11	L24 L22 K25 K22 J26 J24 L23 K26 K23 K21 J25 J23	SLB general purpose logic signals.
CNTRL0 CNTRL1 CNTRL2 CNTRL3 CNTRL4 CNTRL5 CNTRL6 CNTRL7 CNTRL8	N22 M26 N21 M25 J21 H24 H22 H26 H23	SLB general purpose logic signals.

SLB_DAIN0 SLB_DAIN1 SLB_DAIN2 SLB_DAIN3 SLB_DAIN4 SLB_DAIN5 SLB_DAIN6 SLB_DAIN7	AA24 Y22 W23 P23 V24 V22 U22 R22	SLB data bus ch. AI –ve component.
SLB_DAIP0 SLB_DAIP1 SLB_DAIP2 SLB_DAIP3 SLB_DAIP4 SLB_DAIP5 SLB_DAIP6 SLB_DAIP7	AB25 AA22 Y23 P24 U24 U21 T22 R23	SLB data bus ch. AI +ve component.
SLB_DAQN0 SLB_DAQN1 SLB_DAQN2 SLB_DAQN3 SLB_DAQN4 SLB_DAQN5 SLB_DAQN6 SLB_DAQN7	C24 D20 C26 C21 A22 A15 C17 C14	SLB data bus ch. AQ –ve component.

SLB_DAQP0 SLB_DAQP1 SLB_DAQP2 SLB_DAQP3 SLB_DAQP4 SLB_DAQP5 SLB_DAQP6 SLB_DAQP7	D24 D21 B26 B21 B22 A14 B16 C13	SLB data bus ch. AQ +ve component.
SLB_DBIN0 SLB_DBIN1 SLB_DBIN2 SLB_DBIN3 SLB_DBIN4 SLB_DBIN5 SLB_DBIN6 SLB_DBIN7	AB26 AA23 Y25 R21 V26 W21 T25 T23	SLB data bus ch. BI –ve component.
SLB_DBIP0 SLB_DBIP1 SLB_DBIP2 SLB_DBIP3 SLB_DBIP4 SLB_DBIP5 SLB_DBIP6 SLB_DBIP7	AA25 AB24 Y26 P21 U26 V21 U25 T24	SLB data bus ch. BI +ve component.
SLB_DBQN0 SLB_DBQN1 SLB_DBQN2 SLB_DBQN3 SLB_DBQN4 SLB_DBQN5 SLB_DBQN6 SLB_DBQN7	D25 C22 A17 C23 A25 A24 C18 C16	SLB data bus ch. BQ –ve component.
SLB_DBQP0 SLB_DBQP1 SLB_DBQP2 SLB_DBQP3 SLB_DBQP4 SLB_DBQP5 SLB_DBQP6 SLB_DBQP7	D26 D23 B17 B24 B25 A23 B19 B15	SLB data bus ch. BQ +ve component.

Flash memory interface:

FLASH_A<0>	H9	
FLASH_A<1>	G10	
FLASH_A<2>	H21	
FLASH_A<3>	G20	
FLASH_A<4>	H11	
FLASH_A<5>	G11	
FLASH_A<6>	H19	
FLASH_A<7>	H18	
FLASH_A<8>	G12	
FLASH_A<9>	F13	
FLASH_A<10>	G19	
FLASH_A<11>	F18	
FLASH_A<12>	F14	Flash address bus.
FLASH_A<13>	F15	
FLASH_A<14>	F17	
FLASH_A<15>	G17	
FLASH_A<16>	G14	
FLASH_A<17>	H13	
FLASH_A<18>	G16	
FLASH_A<19>	G15	
FLASH_A<20>	Y18	
FLASH_A<21>	AA18	
FLASH_A<22>	Y11	
FLASH_A<23>	AA10	
FLASH_A<24>	AA19	
FLASH_A<25>	Y20	
FLASH_D<0>	AA15	
FLASH_D<1>	Y15	
FLASH_D<2>	W14	
FLASH_D<3>	Y13	Flash data bus.
FLASH_D<4>	W16	
FLASH_D<5>	Y16	
FLASH_D<6>	AA14	
FLASH_D<7>	AA13	
FLASH_CE	Y12	Flash Chip Enable.
FLASH_OE	AA12	Flash Output Enable.
FLASH_RST	W11	Flash RESET.
FLASH_WE	AA17	Flash Write Enable.

Host Port Interface (HPI):

HASA HCNTL0A HCNTL1A HCSA HDS1A HDS2A HHWILA HINTA HRDYA HRWA	V6 T8 U6 W6 U5 U7 V7 T7 T5 W5	DSP1 HPI Control.
HDA<0> HDA<1> HDA<2> HDA<3> HDA<4> HDA<5> HDA<6> HDA<7> HDA<8> HDA<9> HDA<10> HDA<11> HDA<12> HDA<13> HDA<14> HDA<15>	W4 Y4 Y5 Y6 AF3 AF4 AD4 AE5 AF5 AD5 AA5 AB5 AD6 AC6 AE6 AB6	DSP1 HPI Data.

HASB HCNTL0B HCNTL1B HCSB HDS1B HDS2B HHWILB HINTB HRDYB HRWB	G4 J5 J6 F5 H4 H6 G6 K6 K5 G5	DSP2 HPI Control.
HDB<0> HDB<1> HDB<2> HDB<3> HDB<4> HDB<5> HDB<6> HDB<7> HDB<8> HDB<9> HDB<10> HDB<11> HDB<12> HDB<13> HDB<14> HDB<15>	R5 R7 R8 R6 P8 P6 N8 N6 N7 M6 M7 L8 L7 L5 K8 K7	DSP2 HPI Data.

Ethernet PHY interface:

PHYRST PHYCOMA PHYMDC PHYMDIO PHYRXC PHYRXCT PHYRXD0 PHYRXD1 PHYRXD2 PHYRXD3 PHYTXC PHYTXCT PHYTXD0 PHYTXD1 PHYTXD2 PHYTXD3	H7 G7 F12 E11 A9 E8 E7 B9 C8 E6 F7 F8 F9 G9 H8 J8	FPGA Ethernet PHY Interface.

DSP Ethernet PHY interfaces:

RGMDCLKA RGMDIOA RGRDA0 RGRDA1 RGRDA2 RGRDA3 RGRXC0A RGRXTL0A RGTDA0 RGTDA1 RGTDA2 RGTDA3 RGTXC0A RGTXCTL0A	E21 E10 A7 C6 C7 D8 D6 C9 B10 A5 B6 D10 B7 D9	DSP1 Ethernet PHY interface.
RGMDCLKA RGMDIOA RGRDA0 RGRDA1 RGRDA2 RGRDA3 RGRXC0A RGRXTL0A RGTDA0 RGTDA1 RGTDA2 RGTDA3 RGTXC0A RGTXCTL0A	F20 G21 B5 B4 A12 B11 A10 A4 D11 C11 E5 D5 B12 C12	DSP2 Ethernet PHY interface.

RSL/MGT/GTX Interfaces:

RIORX_POS13 RIORX_NEG13 RIORX_POS12 RIORX_NEG12 RIORX_POS2 RIORX_NEG2 RIORX_POS3 RIORX_NEG3 RIORX_POS8 RIORX_NEG8 RIORX_POS9 RIORX_NEG9	R1 T1 V1 U1 C1 D1 F1 E1 AD1 AC1 AA1 AB1	RIO 1st Link RIO 2nd Link RIR 2nd Link RIR 1st Link RIQ 2nd Link RIQ 1st Link
RIOTX_POS13 RIOTX_NEG13 RIOTX_POS12 RIOTX_NEG12 RIOTX_POS2 RIOTX_NEG2 RIOTX_POS3 RIOTX_NEG3 RIOTX_POS8 RIOTX_NEG8 RIOTX_POS9 RIOTX_NEG9	P2 R2 W2 V2 B2 C2 G2 F2 AE2 AD2 Y2 AA2	As above but TX.

SRIO Interfaces:

SRIORXP1 SRIORXN1 SRIORXP2 SRIORXN2	H2 J2 N2 M2	Connection to DSP2.
SRIOTXP1 SRIOTXN1 SRIOTXP2 SRIOTXN2	J1 K1 M1 L1	Connection to DSP1.

RSL/MGT/GTX Clocks:

REFCLKP_114 REFCLKN_114	T4 T3	125MHz clock.
REFCLKP_116 REFCLKN_116	D4 D3	125MHz clock.

Miscellaneous:

SW0 SW1 SW2 SW3	E16 D16 E15 D15	DIP Switch.
LED0 LED1 LED2 LED3	E18 F19 E20 F10	LEDs.

URA0	AF22	
URA1	AB22	
URA2	AC22	
URA3	AC23	
URA4	AC24	
URCLAV	AC7	
URCLK	AF7	
URD0	AD15	
URD1	AD16	
URD2	AE16	
URD3	AF17	
URD4	AE17	
URD5	AD18	
URD6	AE18	
URD7	AF18	
URD8	AF19	UTOPIA Interface to DSP1.
URD9	AD21	
URD10	AC21	
URD11	AD20	
URD12	AD19	
URD13	AE20	
URD14	AF20	
URD15	AE21	
URENB	AB7	
URSOC	AE7	
UXA0	AD14	
UXA1	AF13	
UXA2	AF14	
UXA3	AF15	
UXA4	AE15	
UXCLAV	AA7	
UXCLK	AE8	

UXD0	AF8	
UXD1	AA8	
UXD2	W9	
UXD3	AD11	
UXD4	AE11	
UXD5	V9	
UXD6	AF10	
UXD7	AF9	
UXD8	AE10	
UXD9	AD10	UTOPIA Interface to DSP1 (cont'd).
UXD10	W8	
UXD11	V8	
UXD12	AE12	
UXD13	AF12	
UXD14	AD13	
UXD15	AE13	
UXENB	Y8	
UXSOC	Y7	

8 Support Packages

TBA.

9 Physical Properties

Dimensions (approx.)	4.2”	2.5”

Weight	

Voltage	Current
+12V	TBD
+5V	TBD
+3.3V	TBD
-12V	0

FPGA core power	8W max*

MTBF	

*The core power will vary within custom FPGA applications. For all envisaged FX30T based designs, the core power is not expected to exceed 5W. For modules incorporating the FX70T, a power requirement in excess of 8W is possible and must be managed during the FPGA design cycle. A 10W version of the SMT372T is available but not recommended for analog applications (where an SLB mezzanine is also used).

10 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

11 Safety

This module presents no hazard to the user when in normal use.

12 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.
This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.
Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

13 Ordering Information

SMT372T-30	Virtex5 FX30T.
SMT372T-70	Virtex5 FX70T.